

# SN74ALVC162268

## 12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS

SCES051 – AUGUST 1995

- **B-Port Outputs Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required**
- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Member of the Texas Instruments Widebus™ Family**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

### description

The SN74ALVC162268 is a 12-bit to 24-bit registered bus exchanger, which is intended for use in applications where data must be transferred from a narrow high-speed bus to a wide, lower-frequency bus. This device is designed specifically for low-voltage (3.3-V)  $V_{CC}$  operation; it is tested at 2.5-V, 2.7-V, and 3.3-V  $V_{CC}$ .

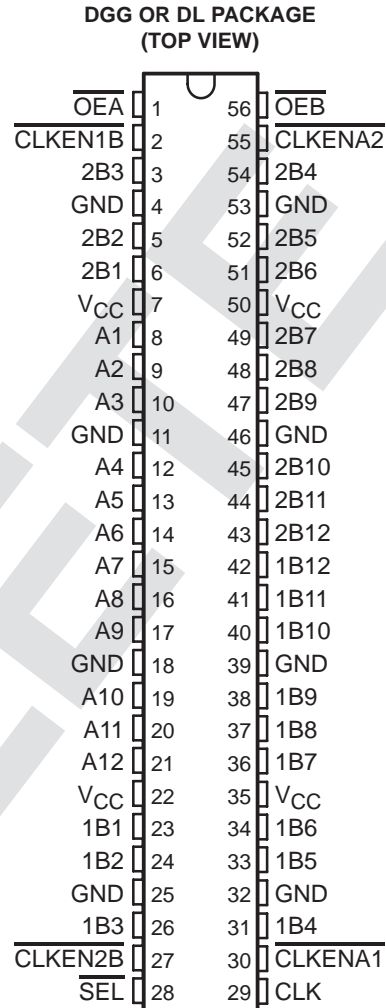
The device provides synchronous data exchange between the two ports. Data is stored in the internal registers on the low-to-high transition of the clock (CLK) input when the appropriate clock-enable (CLKEN) inputs are low. The select (SEL) line is synchronous with CLK and selects 1B or 2B input data for the A outputs.

For data transfer in the A-to-B direction, a two-stage pipeline is provided in the A-to-1B path with a single storage register in the A-to-2B path. Proper control of these inputs allows two sequential 12-bit words to be presented synchronously as a 24-bit word on the B port. Data flow is controlled by the active-low output enables (OEA, OEB). These control terminals are registered so bus direction changes are synchronous with CLK.

The B outputs, which are designed to sink up to 12 mA, include 26-Ω resistors to reduce overshoot and undershoot.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVC162268 is characterized for operation from -40°C to 85°C.



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**Function Tables**

**OUTPUT ENABLE**

INPUTS			OUTPUTS	
CLK	$\overline{OEA}$	$\overline{OEB}$	A	1B, 2B
↑	H	H	Z	Z
↑	H	L	Z	Active
↑	L	H	Active	Z
↑	L	L	Active	Active

**A-TO-B STORAGE ( $\overline{OEB} = L$ )**

INPUTS				OUTPUTS	
$\overline{CLKENA1}$	$\overline{CLKENA2}$	CLK	A	1B	2B
H	H	X	X	1B <sub>0</sub> <sup>‡</sup>	2B <sub>0</sub> <sup>‡</sup>
L	X	↑	L	L <sup>†</sup>	X
L	X	↑	H	H <sup>†</sup>	X
X	L	↑	L	X	L
X	L	↑	H	X	H

† Two CLK edges are needed to propagate data.

‡ Output level before the indicated steady-state input conditions were established

**B-TO-A STORAGE ( $\overline{OEA} = L$ )**

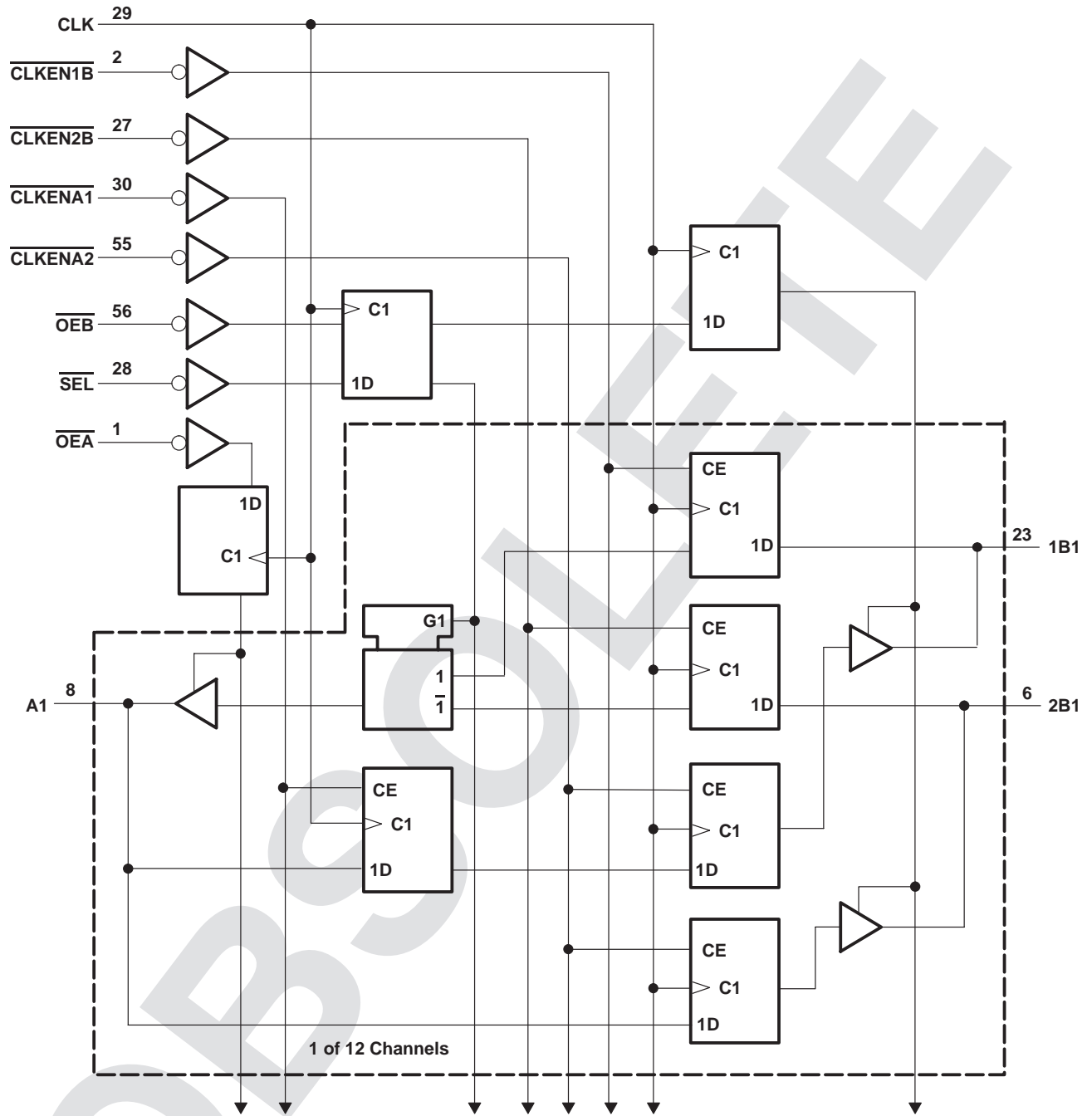
INPUTS						OUTPUT
$\overline{CLKEN1B}$	$\overline{CLKEN2B}$	CLK	$\overline{SEL}$	1B	2B	A
H	X	X	H	X	X	A <sub>0</sub> <sup>‡</sup>
X	H	X	L	X	X	A <sub>0</sub> <sup>‡</sup>
L	X	↑	H	L	X	L
L	X	↑	H	H	X	H
X	L	↑	L	X	L	L
X	L	↑	L	X	H	H

‡ Output level before the indicated steady-state input conditions were established

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logic diagram (positive logic)



# SN74ALVC162268

## 12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS

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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	-0.5 V to 4.6 V
Input voltage range, $V_I$ : Except I/O ports (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
I/O ports (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	$\pm 50$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	$\pm 50$ mA
Continuous current through $V_{CC}$ or GND	$\pm 100$ mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 3): DGG package	1 W
DL package	1.4 W
Storage temperature range, $T_{stg}$	$-65^\circ\text{C}$ to $150^\circ\text{C}$

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. The input and output positive-voltage ratings may be exceeded up to 4.6 V if the input and output clamp-current ratings are observed.  
 3. The maximum package power dissipation is calculated using a junction temperature of  $150^\circ\text{C}$  and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

### recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	2.3	3.6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2.3$ V to 2.7 V	1.7	V
		$V_{CC} = 2.7$ V to 3.6 V	2	
$V_{IL}$	Low-level input voltage	$V_{CC} = 2.3$ V to 2.7 V	0.7	V
		$V_{CC} = 2.7$ V to 3.6 V	0.8	
$V_I$	Input voltage	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	V
$I_{OH}$	High-level output current on the B port	$V_{CC} = 2.3$ V	-6	mA
		$V_{CC} = 2.7$ V	-8	
		$V_{CC} = 3$ V	-12	
$I_{OL}$	Low-level output current on the B port	$V_{CC} = 2.3$ V	6	mA
		$V_{CC} = 2.7$ V	8	
		$V_{CC} = 3$ V	12	
$I_{OH}$	High-level output current on the A port	$V_{CC} = 2.3$ V	-12	mA
		$V_{CC} = 2.7$ V	-12	
		$V_{CC} = 3$ V	-24	
$I_{OL}$	Low-level output current on the A port	$V_{CC} = 2.3$ V	12	mA
		$V_{CC} = 2.7$ V	12	
		$V_{CC} = 3$ V	24	
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
$T_A$	Operating free-air temperature	-40	85	$^\circ\text{C}$

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub> <sup>†</sup>	T <sub>A</sub> = -40°C to 85°C			UNIT	
			MIN	TYP <sup>‡</sup>	MAX		
V <sub>OH</sub> (B port)	I <sub>OH</sub> = -100 μA	MIN to MAX	V <sub>CC</sub> -0.2			V	
	I <sub>OH</sub> = -4 mA, V <sub>IH</sub> = 1.7 V	2.3 V	1.9				
	I <sub>OH</sub> = -6 mA	V <sub>IH</sub> = 1.7 V	2.3 V	1.7			
		V <sub>IH</sub> = 2 V	3 V	2.4			
	I <sub>OH</sub> = -8 mA, V <sub>IH</sub> = 2 V	2.7 V	2				
I <sub>OH</sub> = -12 mA, V <sub>IH</sub> = 2 V	3 V	2					
V <sub>OL</sub> (B port)	I <sub>OL</sub> = 100 μA	MIN to MAX	0.2			V	
	I <sub>OL</sub> = 4 mA, V <sub>IL</sub> = 0.7 V	2.3 V	0.4				
	I <sub>OL</sub> = 6 mA	V <sub>IL</sub> = 0.7 V	2.3 V	0.55			
		V <sub>IL</sub> = 0.8 V	3 V	0.55			
	I <sub>OL</sub> = 8 mA, V <sub>IL</sub> = 0.8 V	2.7 V	0.6				
I <sub>OL</sub> = 12 mA, V <sub>IL</sub> = 0.8 V	3 V	0.8					
V <sub>OH</sub> (A port)	I <sub>OH</sub> = -100 μA	MIN to MAX	V <sub>CC</sub> -0.2			V	
	I <sub>OH</sub> = -6 mA, V <sub>IH</sub> = 1.7 V	2.3 V	2				
	I <sub>OH</sub> = -12 mA	V <sub>IH</sub> = 1.7 V	2.3 V	1.7			
		V <sub>IH</sub> = 2 V	2.7 V	2.2			
		V <sub>IH</sub> = 2 V	3 V	2.4			
I <sub>OH</sub> = -24 mA, V <sub>IH</sub> = 2 V	3 V	2					
V <sub>OL</sub> (A port)	I <sub>OL</sub> = 100 μA	MIN to MAX	0.2			V	
	I <sub>OL</sub> = 6 mA, V <sub>IL</sub> = 0.7 V	2.3 V	0.4				
	I <sub>OL</sub> = 12 mA	V <sub>IL</sub> = 0.7 V	2.3 V	0.7			
		V <sub>IL</sub> = 0.8 V	2.7 V	0.4			
	I <sub>OL</sub> = 24 mA, V <sub>IL</sub> = 0.8 V	3 V	0.55				
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.6 V	±5			μA	
I <sub>I</sub> (hold)	V <sub>I</sub> = 0.7 V	2.3 V	45			μA	
	V <sub>I</sub> = 1.7 V		-45				
	V <sub>I</sub> = 0.8 V	3 V	75				
	V <sub>I</sub> = 2 V		-75				
	V <sub>I</sub> = 0 to 3.6 V		±500				
I <sub>OZ</sub> <sup>§</sup>	V <sub>O</sub> = V <sub>CC</sub> or GND	3.6 V	±10			μA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	3.6 V	40			μA	
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND	3 V to 3.6 V	750			μA	
C <sub>i</sub>	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V	3.5			pF
C <sub>io</sub>	A or B ports	V <sub>O</sub> = V <sub>CC</sub> or GND	3.3 V	9			pF

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

<sup>‡</sup> All typical values are at V<sub>CC</sub> = 3.3 V.

<sup>§</sup> For I/O ports, the parameter I<sub>OZ</sub> includes the input-leakage current.



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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

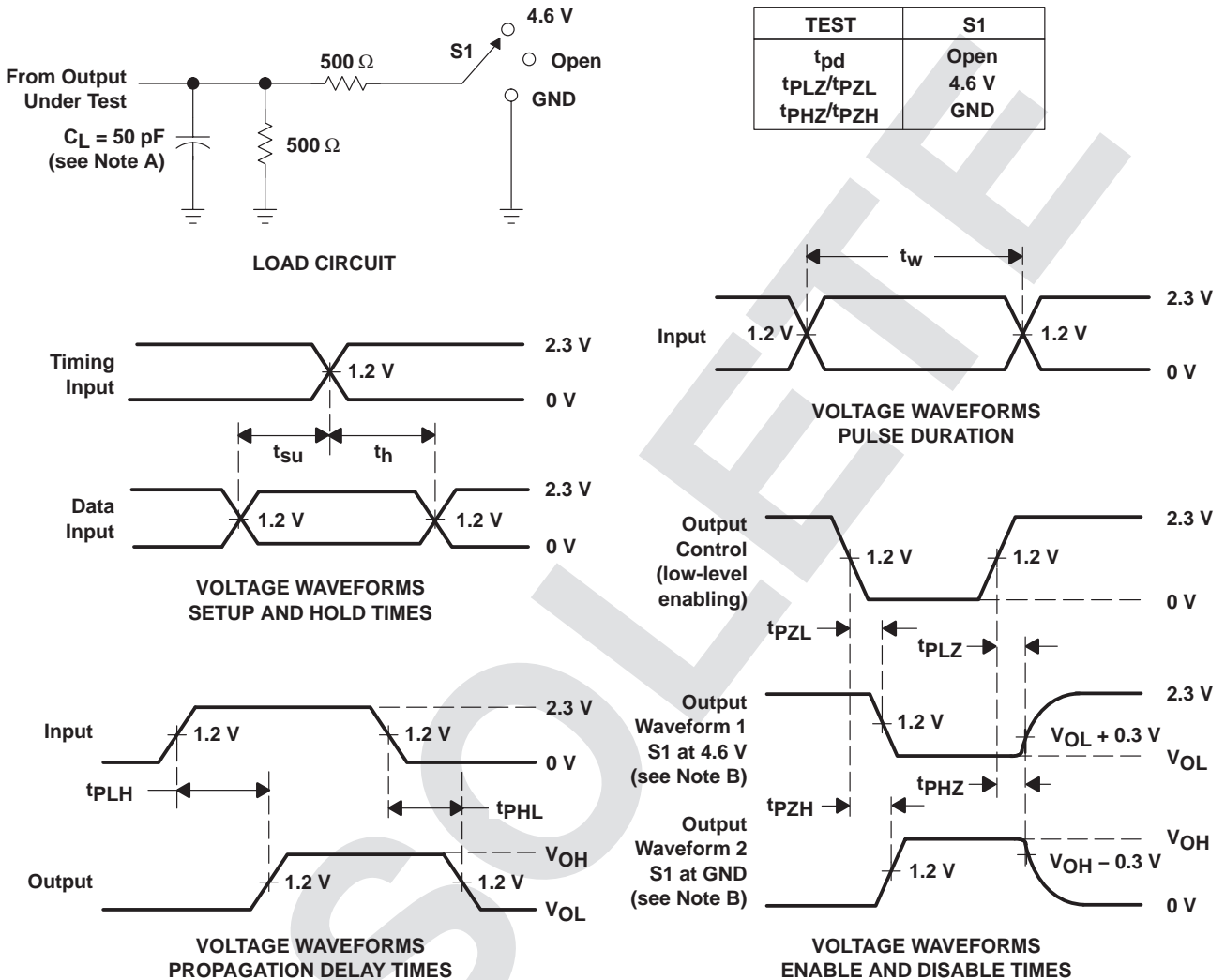
			V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT	
			MIN	MAX	MIN	MAX	MIN	MAX		
f <sub>clock</sub>	Clock frequency		120		125		150		MHz	
t <sub>w</sub>	Pulse duration, CLK High or low		3.3		3.3		3.3		ns	
t <sub>su</sub>	Setup time	A data before CLK↑	High or low		4.5		4		3.4	
		B data before CLK↑	High or low		0.8		1.2		1	
		SEL before CLK↑	High or low		1.4		1.6		1.3	
		CLKENA1 or CLKENA2 before CLK↑	High or low		3.6		3.4		2.8	
		CLKENB1 or CLKENB2 before CLK↑	High or low		3.2		3		2.5	
		OE before CLK↑	High or low		4.2		3.9		3.2	
t <sub>th</sub>	Hold time	A data after CLK↑	High or low		0		0		0.2	
		B data after CLK↑	High or low		1.3		1.2		1.3	
		SEL after CLK↑	High or low		1		1		1	
		CLKENA1 or CLKENA2 after CLK↑	High or low		0.1		0.1		0.4	
		CLKENB1 or CLKENB2 after CLK↑	High or low		0.1		0		0.5	
		OE after CLK↑	High or low		0		0		0.2	

switching characteristics over recommended operating free-air temperature range, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			120		125		150		ns
t <sub>pd</sub>	CLK	B	2.1	6.7	5.9		1.8	5.4	ns
t <sub>pd</sub>	CLK	A (1B)	2.1	6.4	5.4		1.7	4.8	ns
t <sub>pd</sub>	CLK	A (2B)	2.1	6.4	5.3		1.8	4.8	ns
t <sub>pd</sub>	CLK	A (SEL)	3	7.9	6.5		2.4	5.8	ns
t <sub>en</sub>	CLK	B	2.8	7.7	6.8		2.6	6.1	ns
t <sub>dis</sub>	CLK	B	3.5	7.4	6.1		2.5	5.9	ns
t <sub>en</sub>	CLK	A	2.1	6.7	5.6		1.8	5.1	ns
t <sub>dis</sub>	CLK	A	2.7	6.7	5.4		2.1	5	ns



**PARAMETER MEASUREMENT INFORMATION**  
 $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$



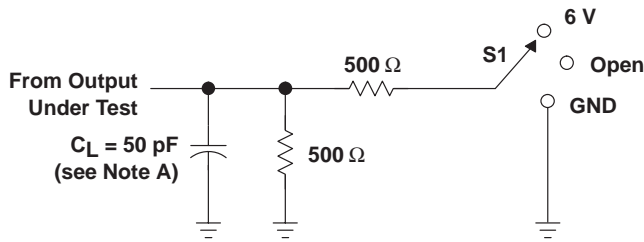
- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .
  - D. The outputs are measured one at a time with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**Figure 1. Load Circuit and Voltage Waveforms**

# SN74ALVC162268 12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS

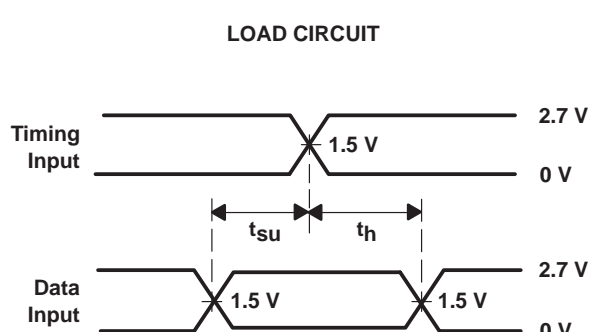
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## PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$

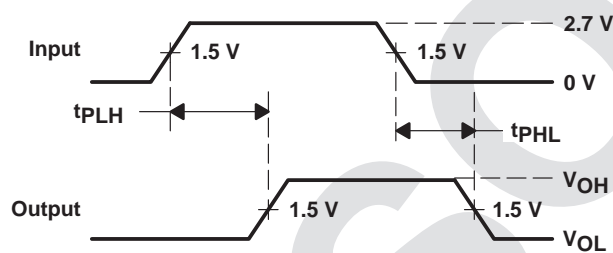


LOAD CIRCUIT

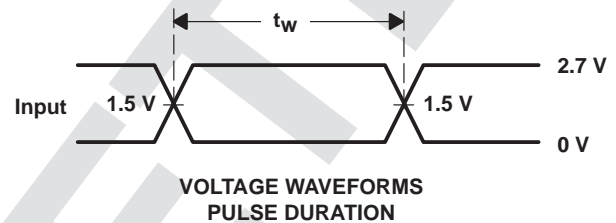
TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



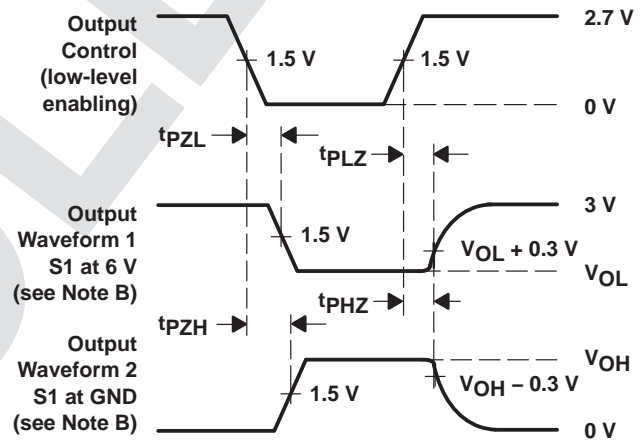
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .  
 D. The outputs are measured one at a time with one transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 2. Load Circuit and Voltage Waveforms



**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74ALVC162268DL	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI
SN74ALVC162268DLR	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

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<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DL (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MO-118

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