

SN54ABT533, SN74ABT533A OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCBS186D – JANUARY 1991 – REVISED JANUARY 1997

- State-of-the-Art *EPIC-IIB™* BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- High-Drive Outputs ($-32\text{-mA } I_{OH}$, $64\text{-mA } I_{OL}$)
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Plastic (N) and Ceramic (J) DIPs, and Ceramic Flat (W) Package

description

These octal transparent D-type latches with 3-state outputs are designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

When the latch-enable (LE) input is high, the \bar{Q} outputs follow the complements of the data (D) inputs. When LE is taken low, the \bar{Q} outputs are latched at the inverse of the levels at the D inputs.

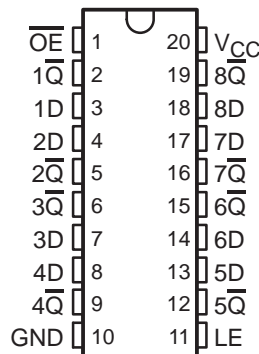
A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

\overline{OE} does not affect the internal operations of the latches. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

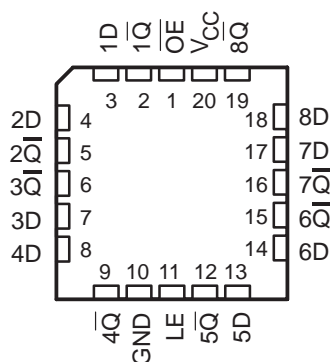
To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT533 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT533A is characterized for operation from -40°C to 85°C .

SN54ABT533 . . . J OR W PACKAGE
SN74ABT533A . . . DB, DW, N, OR PW PACKAGE
(TOP VIEW)



SN54ABT533 . . . FK PACKAGE
(TOP VIEW)



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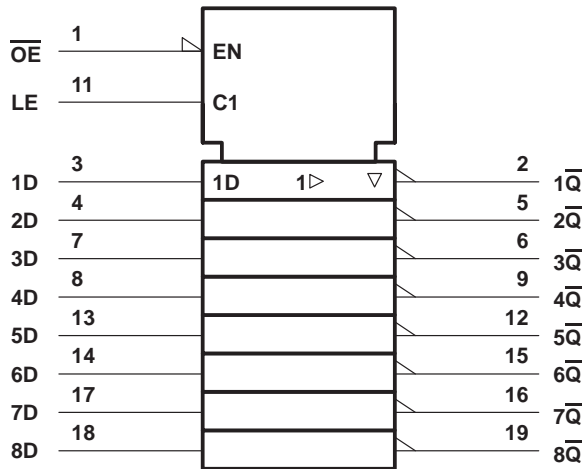
SN54ABT533, SN74ABT533A OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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FUNCTION TABLE
(each latch)

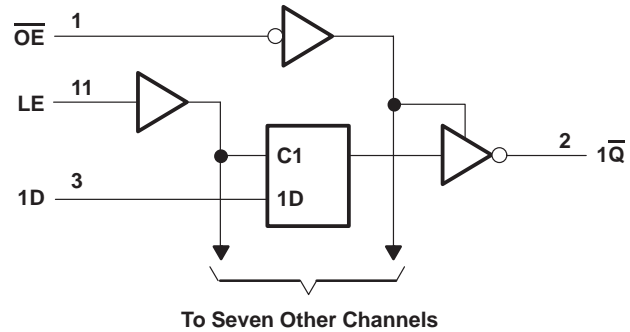
| INPUTS | | | OUTPUT |
|-----------------|----|---|------------------|
| \overline{OE} | LE | D | \overline{Q} |
| L | H | H | L |
| L | H | L | H |
| L | L | X | \overline{Q}_0 |
| H | X | X | Z |

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

| | |
|---------------------------------------------------------------------------------|-----------------|
| Supply voltage range, V_{CC} | -0.5 V to 7 V |
| Input voltage range, V_I (see Note 1) | -0.5 V to 7 V |
| Voltage range applied to any output in the high or power-off state, V_O | -0.5 V to 5.5 V |
| Current into any output in the low state, I_O : SN54ABT533 | 96 mA |
| SN74ABT533A | 128 mA |
| Input clamp current, I_{IK} ($V_I < 0$) | -18 mA |
| Output clamp current, I_{OK} ($V_O < 0$) | -50 mA |
| Package thermal impedance, θ_{JA} (see Note 2): DB package | 115°C/W |
| DW package | 97°C/W |
| N package | 67°C/W |
| PW package | 128°C/W |
| Storage temperature range, T_{stg} | -65°C to 150°C |

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for through-hole packages, which use a trace length of zero.

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recommended operating conditions (see Note 3)

| | | SN54ABT533 | | SN74ABT533A | | UNIT |
|-----------------|------------------------------------|------------|-----------------|-------------|-----------------|------|
| | | MIN | MAX | MIN | MAX | |
| V _{CC} | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| V _{IH} | High-level input voltage | 2 | | 2 | | V |
| V _{IL} | Low-level input voltage | | 0.8 | | 0.8 | V |
| V _I | Input voltage | 0 | V _{CC} | 0 | V _{CC} | V |
| I _{OH} | High-level output current | | -24 | | -32 | mA |
| I _{OL} | Low-level output current | | 48 | | 64 | mA |
| Δt/Δv | Input transition rise or fall rate | | 10 | | 10 | ns/V |
| T _A | Operating free-air temperature | -55 | 125 | -40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | T _A = 25°C | | | SN54ABT533 | | SN74ABT533A | | UNIT |
|--------------------------|--------------------------------------------------------------------------------------|--------------------------|------|-------|------------|------|-------------|------|------|
| | | MIN | TYP† | MAX | MIN | MAX | MIN | MAX | |
| V _{IK} | V _{CC} = 4.5 V, I _I = -18 mA | | | -1.2 | | -1.2 | | -1.2 | V |
| V _{OH} | V _{CC} = 4.5 V, I _{OH} = -3 mA | 2.5 | | | 2.5 | | | 2.5 | V |
| | V _{CC} = 5 V, I _{OH} = -3 mA | 3 | | | 3 | | | 3 | |
| | V _{CC} = 4.5 V | I _{OH} = -24 mA | 2 | | | 2 | | | |
| I _{OH} = -32 mA | | 2* | | | | | | 2 | |
| V _{OL} | V _{CC} = 4.5 V | I _{OL} = 48 mA | | 0.55 | | 0.55 | | | V |
| | | I _{OL} = 64 mA | | 0.55* | | | 0.55 | | |
| V _{hys} | | | 100 | | | | | | mV |
| I _I | V _{CC} = 5.5 V, V _I = V _{CC} or GND | | | ±1 | | ±1 | | ±1 | μA |
| I _{OZH} | V _{CC} = 5.5 V, V _O = 2.7 V | | | 10 | | 10 | | 10 | μA |
| I _{OZL} | V _{CC} = 5.5 V, V _O = 0.5 V | | | -10 | | -10 | | -10 | μA |
| I _{off} | V _{CC} = 0, V _I or V _O ≤ 4.5 V | | | ±150 | | | | ±150 | μA |
| I _{CEX} | V _{CC} = 5.5 V, V _O = 5.5 V | Outputs high | | 50 | | 50 | | 50 | μA |
| I _{O‡} | V _{CC} = 5.5 V, V _O = 2.5 V | -50 | -140 | -180 | -50 | -180 | -50 | -180 | mA |
| I _{CC} | V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND | Outputs high | | 1 | 250 | 250 | 250 | 250 | μA |
| | | Outputs low | | 24 | 30 | 30 | 30 | 30 | mA |
| | | Outputs disabled | | 0.5 | 250 | 250 | 250 | 250 | μA |
| ΔI _{CC} § | V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND | Outputs high | | 1.5 | | 1.5 | | 1.5 | mA |
| | | Outputs low | | 1.5 | | 1.5 | | 1.5 | |
| | | Outputs disabled | | 1.5 | | 1.5 | | 1.5 | |
| C _i | V _I = 2.5 V or 0.5 V | | 3.5 | | | | | | pF |
| C _o | V _O = 2.5 V or 0.5 V | | 6.5 | | | | | | pF |

* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V_{CC} = 5 V.

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.



SN54ABT533, SN74ABT533A
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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

| | | SN54ABT533 | | | | UNIT | |
|-----------------|-----------------------------|-------------------------------------------------|-----|--|-----|------|-----|
| | | V _{CC} = 5 V, T _A = 25°C | | | MIN | | MAX |
| | | MIN | MAX | | | | |
| t _w | Pulse duration, LE high | | 3.3 | | 3.3 | ns | |
| t _{su} | Setup time, data before LE↓ | High or low | 2.1 | | 2.1 | ns | |
| t _h | Hold time, data after LE↓ | High or low | 1.5 | | 1.5 | ns | |

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

| | | SN74ABT533A | | | | UNIT | |
|-----------------|-----------------------------|-------------------------------------------------|-----|--|-----|------|-----|
| | | V _{CC} = 5 V, T _A = 25°C | | | MIN | | MAX |
| | | MIN | MAX | | | | |
| t _w | Pulse duration, LE high | | 3.3 | | 3.3 | ns | |
| t _{su} | Setup time, data before LE↓ | High or low | 2.1 | | 2.1 | ns | |
| t _h | Hold time, data after LE↓ | High or low | 2.1 | | 2.1 | ns | |

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54ABT533 | | | | | UNIT |
|------------------|-----------------|----------------|-------------------------------------------------|-----|-----|-----|-----|------|
| | | | V _{CC} = 5 V, T _A = 25°C | | | MIN | MAX | |
| | | | MIN | TYP | MAX | | | |
| t _{PLH} | D | Q̄ | 1.9 | 4.2 | 5.4 | 1.9 | 6.7 | ns |
| t _{PHL} | | | 3.1 | 4.9 | 6.3 | | | |
| t _{PLH} | LE | Q̄ | 2.7 | 4.9 | 6.2 | 2.7 | 7.6 | ns |
| t _{PHL} | | | 3.5 | 5.4 | 6.8 | | | |
| t _{PZH} | OĒ | Q̄ | 1.6 | 3.7 | 4.8 | 1.6 | 5.8 | ns |
| t _{PZL} | | | 2.4 | 4.2 | 6.2 | | | |
| t _{PHZ} | OĒ | Q̄ | 2.8 | 5.1 | 6.2 | 2.8 | 7.2 | ns |
| t _{PLZ} | | | 2 | 4.1 | 6 | | | |



SN54ABT533, SN74ABT533A
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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN74ABT533A | | | | UNIT | |
|-----------|-----------------|----------------|---------------------------------------------|-----|-----|-----|------|-----|
| | | | $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$ | | | MIN | | MAX |
| | | | MIN | TYP | MAX | | | |
| t_{PLH} | D | \bar{Q} | 1.7 | 4.2 | 5.4 | 1.7 | 6.4 | ns |
| t_{PHL} | | | 2.6 | 4.9 | 6.3 | 2.6 | 6.6 | |
| t_{PLH} | LE | \bar{Q} | 2.7 | 4.9 | 6.2 | 2.7 | 7.3 | ns |
| t_{PHL} | | | 3.5 | 5.4 | 6.8 | 3.5 | 7.3 | |
| t_{PZH} | \overline{OE} | \bar{Q} | 1.6 | 3.7 | 4.8 | 1.6 | 5.7 | ns |
| t_{PZL} | | | 2.4 | 4.2 | 6.2 | 2.4 | 6.7 | |
| t_{PHZ} | \overline{OE} | \bar{Q} | 1.6 | 5.1 | 6.2 | 1.6 | 6.9 | ns |
| t_{PLZ} | | | 2 | 4.1 | 6 | 2 | 6.5 | |

SN54ABT533, SN74ABT533A OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

| TEST | S1 |
|-------------------|------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | 7 V |
| t_{PHZ}/t_{PZH} | Open |



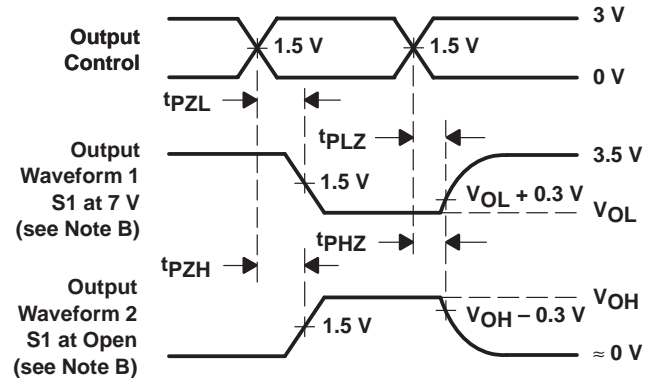
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/ Ball Finish | MSL Peak Temp ⁽³⁾ | Samples (Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|----------------------------|----------------------|------------------------------|-----------------------------|
| 5962-9584301Q2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | Call TI | Call TI | |
| 5962-9584301QRA | ACTIVE | CDIP | J | 20 | 1 | TBD | Call TI | Call TI | |
| 5962-9584301QSA | ACTIVE | CFP | W | 20 | 1 | TBD | Call TI | Call TI | |
| SN74ABT533ADBLE | OBSOLETE | SSOP | DB | 20 | | TBD | Call TI | Call TI | |
| SN74ABT533ADBR | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74ABT533ADBRE4 | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74ABT533ADBRG4 | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74ABT533ADW | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74ABT533ADWE4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74ABT533ADWG4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74ABT533AN | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | |
| SN74ABT533ANE4 | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | |
| SN74ABT533APWLE | OBSOLETE | TSSOP | PW | 20 | | TBD | Call TI | Call TI | |
| SN74ABT533APWR | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74ABT533APWRE4 | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74ABT533APWRG4 | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SNJ54ABT533FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | |
| SNJ54ABT533J | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 | N / A for Pkg Type | |
| SNJ54ABT533W | ACTIVE | CFP | W | 20 | 1 | TBD | Call TI | N / A for Pkg Type | |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN54ABT533 :

- Catalog: [SN74ABT533](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


| | |
|----|-----------------------------------------------------------|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

TAPE AND REEL INFORMATION

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74ABT533ADBR | SSOP | DB | 20 | 2000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74ABT533APWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74ABT533ADBR | SSOP | DB | 20 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74ABT533APWR | TSSOP | PW | 20 | 2000 | 367.0 | 367.0 | 38.0 |

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within Mil-Std 1835 GDFP2-F20

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF TERMINALS ** | A | | B | |
|---------------------|------------------|------------------|------------------|------------------|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.740 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AC.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - \triangle Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - \triangle Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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