

EMC-OPTIMIZED HIGH SPEED CAN TRANSCEIVER

 Check for Samples: [SN65HVD1040A-Q1](#)

FEATURES

- Qualified for Automotive Applications
- Improved Drop-In Replacement for TJA1040
- Meets or Exceeds the Requirements of ISO 11898-5
- GIFT/ICT Compliant
- ESD Protection up to ± 12 kV (Human-Body Model) on Bus Pins
- Low-Current Standby Mode With Bus Wake-Up, <12 μ A Max
- High Electromagnetic Compliance (EMC)
- Bus-Fault Protection of -27 V to 40 V
- Dominant Time-Out Function
- Thermal Shutdown Protection
- Power-Up/Down Glitch-Free Bus Inputs and Outputs
 - High Input Impedance With Low V_{CC}
 - Monotonic Outputs During Power Cycling

APPLICATIONS

- GMW3122 Dual-Wire CAN Physical Layer
- SAE J2284 High-Speed CAN for Automotive Applications
- SAE J1939 Standard Data Bus Interface
- ISO 11783 Standard Data Bus Interface
- NMEA 2000 Standard Data Bus Interface

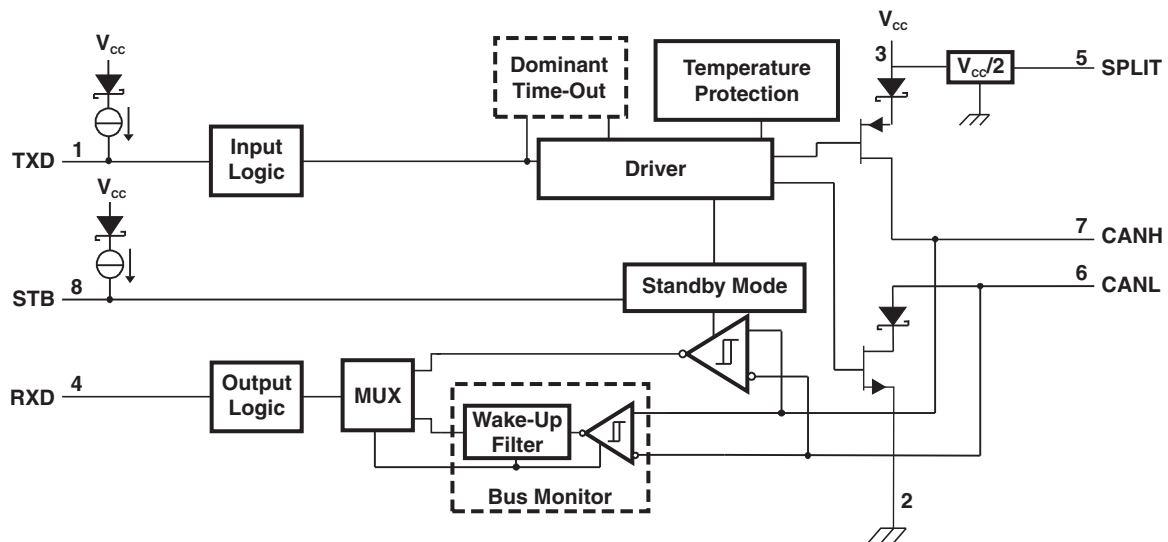
DESCRIPTION

The SN65HVD1040A meets or exceeds the specifications of the ISO 11898 standard for use in applications employing a Controller Area Network (CAN). The device is qualified for use in automotive applications.

As a CAN transceiver, this device provides differential transmit capability to the bus and differential receive capability to a CAN controller at signaling rates up to 1 megabit per second (Mbps)⁽¹⁾.

- (1) The signaling rate of a line is the number of voltage transitions that are made per second, expressed in the units bps (bits per second).

FUNCTIONAL BLOCK DIAGRAM



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

Designed for operation in especially harsh environments, the SN65HVD1040A features cross-wire, over-voltage, and loss of ground protection from -27 V to 40 V , over-temperature protection, a -12-V to 12-V common-mode range, and withstands voltage transients according to ISO 7637.

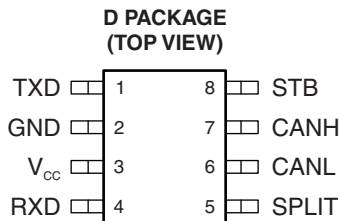
STB (pin 8) provides two different modes of operation: high-speed mode or low-current standby mode. The high-speed mode of operation is selected by connecting STB (pin 8) to ground.

If a high logic level is applied to the STB pin of the SN65HVD1040A, the device enters a low-current standby mode, while the receiver remains active in a low-power bus-monitor standby mode.

In the low-current standby mode, a dominant bit greater than $5\text{ }\mu\text{s}$ on the bus is passed by the bus-monitor circuit to the receiver output. The local protocol controller may then reactivate the device when it needs to transmit to the bus.

A dominant time-out circuit in the SN65HVD1040A prevents the driver from blocking network communication with a hardware or software failure. The time-out circuit is triggered by a falling edge on TXD (pin 1). If no rising edge is seen before the time-out constant of the circuit expires, the driver is disabled. The circuit is then reset by the next rising edge on TXD.

SPLIT (pin 5) is available as a $V_{CC}/2$ common-mode bus voltage bias for a split-termination network (see application information).



ORDERING INFORMATION⁽¹⁾

| PART NUMBER | PACKAGE ⁽²⁾ | MARKED AS | ORDERING NUMBER |
|-----------------|------------------------|-----------|--------------------------|
| SN65HVD1040A-Q1 | SOIC-8 | 1040AQ | SN65HVD1040AQDRQ1 (reel) |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

ABSOLUTE MAXIMUM RATINGS^{(1) (2)}

| | | VALUE |
|----------|---|-----------------|
| V_{CC} | Supply voltage range | –0.3 V to 6 V |
| | Voltage range at bus terminals (CANH, CANL, SPLIT) | –27 V to 40 V |
| I_O | Receiver output current | 20 mA |
| V_I | Voltage input range, ISO 7637 transient pulse ⁽³⁾ (CANH, CANL) | –150 V to 100 V |
| V_I | Voltage input range (TXD, STB) | –0.3 V to 6 V |
| T_J | Junction temperature range | –40°C to 150°C |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
- (3) Tested in accordance with ISO 7637 test pulses 1, 2, 3a, 3b per IBEE system level test (Pulse 1 = –100 V, Pulse 2 = 100 V, Pulse 3a = –150 V, Pulse 3b = 100 V). If dc may be coupled with ac transients, externally protect the bus pins within the absolute maximum voltage range at any bus terminal. This device has been tested with dc bus shorts to +40 V with leading common-mode chokes. If common-mode chokes are used in the system and the bus lines may be shorted to dc, ensure that the choke type and value in combination with the node termination and shorting voltage either will not create inductive flyback outside of voltage maximum specification or use an external transient-suppression circuit to protect the transceiver from the inductive transients.

ELECTROSTATIC DISCHARGE PROTECTION

| PARAMETER | TEST CONDITIONS | VALUE | |
|--|-------------------------------------|------------------------------|---------|
| Electrostatic discharge ⁽¹⁾ | Human-Body Model ⁽²⁾ | CANH and CANL ⁽³⁾ | ±12 kV |
| | | SPLIT ⁽⁴⁾ | ±10 kV |
| | | All pins | ±4 kV |
| | Charged-Device Model ⁽⁵⁾ | All pins | ±1.5 kV |
| | Machine Model ⁽⁶⁾ | | ±200 V |

- (1) All typical values at 25°C.
- (2) Tested in accordance JEDEC Standard 22, Test Method A114E.
- (3) Test method based upon JEDEC Standard 22 Test Method A114E, CANH and CANL bus pins stressed with respect to each other and GND.
- (4) Test method based upon JEDEC Standard 22 Test Method A114E, SPLIT pin stressed with respect to GND.
- (5) Tested in accordance JEDEC Standard 22, Test Method C101C.
- (6) Tested in accordance JEDEC Standard 22, Test Method A115A.

RECOMMENDED OPERATING CONDITIONS

| | | | MIN | MAX | UNIT |
|-------------------|---|-----------------------------------|------|------|------|
| V_{CC} | Supply voltage | | 4.75 | 5.25 | V |
| V_I or V_{IC} | Voltage at any bus terminal (separately or common mode) | | –12 | 12 | V |
| V_{IH} | High-level input voltage | TXD, STB | 2 | 5.25 | V |
| V_{IL} | Low-level input voltage | TXD, STB | 0 | 0.8 | V |
| V_{ID} | Differential input voltage | | –6 | 6 | V |
| I_{OH} | High-level output current | Driver | –70 | | mA |
| | | Receiver | –2 | | |
| I_{OL} | Low-level output current | Driver | | 70 | mA |
| | | Receiver | | 2 | |
| T_A | Operating free-air temperature range | See Thermal Characteristics table | –40 | 125 | °C |

SUPPLY CURRENT

over recommended operating conditions including operating free-air temperature range (unless otherwise noted)

| | PARAMETER | TEST CONDITIONS | MIN | TYP ⁽¹⁾ | MAX | UNIT | |
|----------|--------------------|-----------------|--------------------------------------|--------------------|-----|------|----|
| I_{CC} | 5-V supply current | Standby mode | | 6 | 12 | μA | |
| | | Dominant | $V_I = 0$ V, 60-Ω load, STB at 0 V | | 50 | 70 | mA |
| | | Recessive | $V_I = V_{CC}$, No load, STB at 0 V | | 6 | 10 | |

- (1) All typical values are at 25°C with a 5-V supply.

DEVICE SWITCHING CHARACTERISTICS

over recommended operating conditions, $T_A = -40^\circ\text{C}$ to 125°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|-----------------------|--|--------------------------|-----|-----|------|
| $t_{d(\text{LOOP1})}$ | Total loop delay, driver input to receiver output, recessive to dominant | STB at 0 V, See Figure 9 | 90 | 230 | ns |
| $t_{d(\text{LOOP2})}$ | Total loop delay, driver input to receiver output, dominant to recessive | | 90 | 230 | ns |

DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions, $T_A = -40^\circ\text{C}$ to 125°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|---------------------|---|--|--------------|--------------------|--------------|---------------|
| $V_{O(D)}$ | Bus output voltage (dominant) | CANH | 2.9 | 3.4 | 4.5 | V |
| | | CANL | | | | |
| $V_{O(R)}$ | Bus output voltage (recessive) | $V_I = 3\text{ V}$, STB at 0 V, $R_L = 60\ \Omega$, See Figure 1 and Figure 2 | 2 | 2.5 | 3 | V |
| V_O | Bus output voltage (standby mode) | STB at V_{CC} , $R_L = 60\ \Omega$, See Figure 1 and Figure 2 | -0.1 | | 0.1 | V |
| $V_{OD(D)}$ | Differential output voltage (dominant) | $V_I = 0\text{ V}$, $R_L = 60\ \Omega$, STB at 0 V, See Figure 1, Figure 2, and Figure 3 | 1.5 | | 3 | V |
| | | $V_I = 0\text{ V}$, $R_L = 45\ \Omega$, STB at 0 V, See Figure 1, Figure 2, and Figure 3 | 1.4 | | 3 | |
| $V_{OD(R)}$ | Differential output voltage (recessive) | $V_I = 3\text{ V}$, STB at 0 V, $R_L = 60\ \Omega$, See Figure 1 and Figure 2 | -0.012 | | 0.012 | V |
| | | $V_I = 3\text{ V}$, STB at 0 V, No load | -0.5 | | 0.05 | |
| V_{SYM} | Output symmetry (dominant or recessive) ($V_{O(\text{CANH})} + V_{O(\text{CANL})}$) | STB at 0 V, $R_L = 60\ \Omega$, See Figure 13 | $0.9 V_{CC}$ | V_{CC} | $1.1 V_{CC}$ | V |
| $V_{OC(ss)}$ | Steady-state common-mode output voltage | STB at 0 V, $R_L = 60\ \Omega$, See Figure 8 | 2 | 2.5 | 3 | V |
| $\Delta V_{OC(ss)}$ | Change in steady-state common-mode output voltage | STB at 0 V, $R_L = 60\ \Omega$, See Figure 8 | | 30 | | mV |
| I_{IH} | High-level input current, TXD input | V_I at V_{CC} | -2 | | 2 | μA |
| I_{IL} | Low-level input current, TXD input | V_I at 0 V | -50 | | -10 | μA |
| $I_{O(off)}$ | Power-off TXD output current | V_{CC} at 0 V, TXD at 5 V | | | 1 | μA |
| $I_{OS(ss)}$ | Short-circuit steady-state output current | $V_{\text{CANH}} = -12\text{ V}$, CANL open, See Figure 11 | -120 | -85 | | mA |
| | | $V_{\text{CANH}} = 12\text{ V}$, CANL open, See Figure 11 | | 0.4 | 1 | |
| | | $V_{\text{CANL}} = -12\text{ V}$, CANH open, See Figure 11 | -1 | -0.6 | | |
| | | $V_{\text{CANL}} = 12\text{ V}$, CANH open, See Figure 11 | | 75 | 120 | |
| C_O | Output capacitance | See receiver input capacitance | | | | |

(1) All typical values are at 25°C with a 5-V supply.

DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions, $T_A = -40^\circ\text{C}$ to 125°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|-------------|--|--|-----|--------------------|-----|---------------|
| t_{PLH} | Propagation delay time, low-to-high level output | STB at 0 V, See Figure 4 | 25 | 65 | 120 | ns |
| t_{PHL} | Propagation delay time, high-to-low level output | STB at 0 V, See Figure 4 | 25 | 45 | 120 | ns |
| t_r | Differential output signal rise time | STB at 0 V, See Figure 4 | | 25 | | ns |
| t_f | Differential output signal fall time | STB at 0 V, See Figure 4 | | 45 | | ns |
| t_{en} | Enable time from standby mode to dominant | See Figure 7 | | | 10 | μs |
| $t_{(dom)}$ | Dominant time out ⁽²⁾ | $\downarrow V_I$, See Figure 10 | 300 | 450 | 700 | μs |

(1) All typical values are at 25°C with a 5-V supply.

(2) The TXD dominant time out ($t_{(dom)}$) disables the driver of the transceiver once the TXD has been dominant longer than $t_{(dom)}$, which releases the bus lines to recessive, preventing a local failure from locking the bus dominant. The driver may only transmit dominant again after TXD has been returned HIGH (recessive). While this protects the bus from local faults, locking the bus dominant, it limits the minimum data rate possible. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. This, along with the $t_{(dom)}$ minimum, limits the minimum bit rate. The minimum bit rate may be calculated by:

$$\text{Minimum Bit Rate} = 11 / t_{(dom)} = 11 \text{ bits} / 300 \mu\text{s} = 37 \text{ kbps}$$

RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions, $T_A = -40^\circ\text{C}$ to 125°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|--------------|--|--|-----|--------------------|------|---------------|
| V_{IT+} | Positive-going input threshold voltage, high-speed mode | STB at 0 V, See Table 3 | | 800 | 900 | mV |
| V_{IT-} | Negative-going input threshold voltage, high-speed mode | STB at 0 V, See Table 3 | 500 | 650 | | mV |
| V_{hys} | Hysteresis voltage ($V_{IT+} - V_{IT-}$) | | 100 | 125 | | mV |
| V_{IT} | Input threshold voltage, standby mode | STB at V_{CC} | 500 | | 1150 | mV |
| V_{OH} | High-level output voltage | $I_O = -2 \text{ mA}$, See Figure 6 | 4 | 4.6 | | V |
| V_{OL} | Low-level output voltage | $I_O = 2 \text{ mA}$, See Figure 6 | | 0.2 | 0.4 | V |
| $I_{I(off)}$ | Power-off bus input current | CANH = CANL = 5 V, V_{CC} at 0 V, TXD at 0 V | | | 3 | μA |
| $I_{O(off)}$ | Power-off RXD leakage current | V_{CC} at 0 V, RXD at 5 V | | | 20 | μA |
| C_I | Input capacitance to ground (CANH or CANL) | TXD at 3 V, $V_I = 0.4 \sin(4E6\pi t) + 2.5 \text{ V}$ | | 13 | | pF |
| C_{ID} | Differential input capacitance | TXD at 3 V, $V_I = 0.4 \sin(4E6\pi t)$ | | 6 | | pF |
| R_{ID} | Differential input resistance | TXD at 3 V, STB at 0 V | 30 | | 80 | k Ω |
| R_{IN} | Input resistance (CANH or CANL) | TXD at 3 V, STB at 0 V | 15 | 30 | 40 | k Ω |
| $R_{I(m)}$ | Input resistance matching [$1 - (R_{IN(CANH)} / R_{IN(CANL)})$] \times 100% | $V_{(CANH)} = V_{(CANL)}$ | -3 | 0 | 3 | % |

(1) All typical values are at 25°C with a 5-V supply.

RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions, $T_A = -40^\circ\text{C}$ to 125°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|-----------|--|---------------------------------|-----|--------------------|-----|---------------|
| t_{PLH} | Propagation delay time, low-to-high-level output | STB at 0 V, See Figure 6 | 60 | 90 | 130 | ns |
| t_{PHL} | Propagation delay time, high-to-low-level output | STB at 0 V, See Figure 6 | 45 | 70 | 130 | ns |
| t_r | Output signal rise time | STB at 0 V, See Figure 6 | | 8 | | ns |
| t_f | Output signal fall time | STB at 0 V, See Figure 6 | | 8 | | ns |
| t_{BUS} | Dominant time required on bus for wake-up from standby | STB at V_{CC} , See Figure 12 | 1.5 | | 5 | μs |

(1) All typical values are at 25°C with a 5-V supply.

STB PIN CHARACTERISTICS

over recommended operating conditions, $T_A = -40^\circ\text{C}$ to 125°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|-----------|--------------------------|-----------------|-----|-----|---------------|
| I_{IH} | High-level input current | STB at V_{CC} | -10 | 0 | μA |
| I_{IL} | Low-level input current | STB at 0 V | -10 | 0 | μA |

SPLIT PIN CHARACTERISTICS

over recommended operating conditions, $T_A = -40^\circ\text{C}$ to 125°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|--------------|-------------------------------|--|--------------|--------------------|--------------|---------------|
| V_O | Output voltage | $-500 \mu\text{A} < I_O < 500 \mu\text{A}$ | $0.3 V_{CC}$ | $0.5 V_{CC}$ | $0.7 V_{CC}$ | V |
| $I_{O(stb)}$ | Leakage current, standby mode | STB at 2 V, $-12 \text{ V} \leq V_O \leq 12 \text{ V}$ | -5 | | 5 | μA |

(1) All typical values are at 25°C with a 5-V supply.

THERMAL CHARACTERISTICS

over recommended operating conditions, $T_A = -40^\circ\text{C}$ to 125°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------------|---|--|-----|-----|-----|---------------------------|
| θ_{JA} | Junction-to-air thermal resistance ⁽¹⁾ | Low-K thermal resistance ⁽²⁾ | | 211 | | $^\circ\text{C}/\text{W}$ |
| | | High-K thermal resistance ⁽²⁾ | | 131 | | |
| θ_{JB} | Junction-to-board thermal resistance | | | 53 | | $^\circ\text{C}/\text{W}$ |
| θ_{JC} | Junction-to-case thermal resistance | | | 79 | | $^\circ\text{C}/\text{W}$ |
| P_D | Average power dissipation | $V_{CC} = 5 \text{ V}$, $T_J = 27^\circ\text{C}$, $R_L = 60 \Omega$, STB at 0 V, Input to TXD at 500 kHz, 50% duty cycle square wave, C_L at RXD = 15 pF | | 112 | | mW |
| | | $V_{CC} = 5.5 \text{ V}$, $T_J = 130^\circ\text{C}$, $R_L = 45 \Omega$, STB at 0 V, Input to TXD at 500 kHz, 50% duty cycle square wave, C_L at RXD = 15 pF | | | 170 | |
| Thermal shutdown temperature | | | | 185 | | $^\circ\text{C}$ |

(1) The junction temperature (T_J) is calculated using the following $T_J = T_A + (P_D \times \theta_{JA})$.

(2) Tested in accordance with the Low-K (EIA/JESD51-3) or High-K (EIA/JESD51-7) thermal metric definitions for leaded surface-mount packages.

FUNCTION TABLES

Table 1. DRIVER⁽¹⁾

| INPUTS | | OUTPUTS | | BUS STATE |
|--------|-----------|---------|------|-----------|
| TXD | STB | CANH | CANL | |
| L | L | H | L | Dominant |
| H | L | Z | Z | Recessive |
| Open | L | Z | Z | Recessive |
| X | H or Open | Y | Y | Recessive |

(1) H = high level, L = low level, X = irrelevant, ? = indeterminate, Z = high impedance, Y = weak pull down to GND

Table 2. RECEIVER⁽¹⁾

| DIFFERENTIAL INPUTS $V_{ID} = V(\text{CANH}) - V(\text{CANL})$ | STB | OUTPUT RXD | BUS STATE |
|---|-----------|---------------|-----------|
| $V_{ID} \geq 0.9 \text{ V}$ | L | L | Dominant |
| $V_{ID} \geq 1.15 \text{ V}$ | H or Open | L | Dominant |
| $0.5 \text{ V} < V_{ID} < 0.9 \text{ V}$ | X | ? | ? |
| $V_{ID} \leq 0.5 \text{ V}$ | X | H | Recessive |
| Open | X | H | Recessive |

(1) H = high level, L = low level, X = irrelevant, ? = indeterminate, Z = high impedance

PARAMETER MEASUREMENT INFORMATION

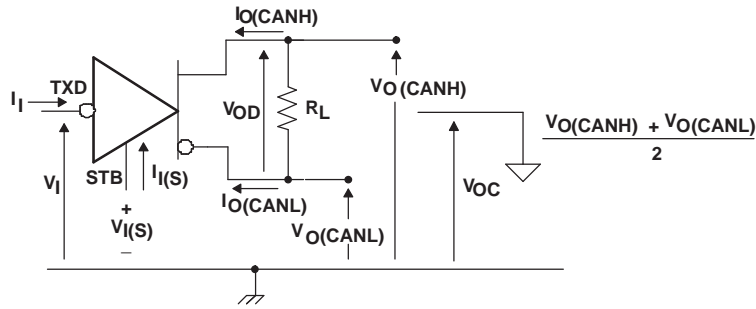


Figure 1. Driver Voltage, Current, and Test Definition

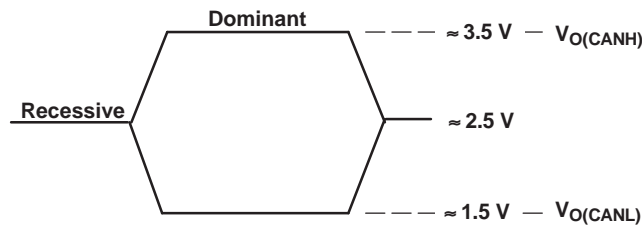


Figure 2. Bus Logic-State Voltage Definitions

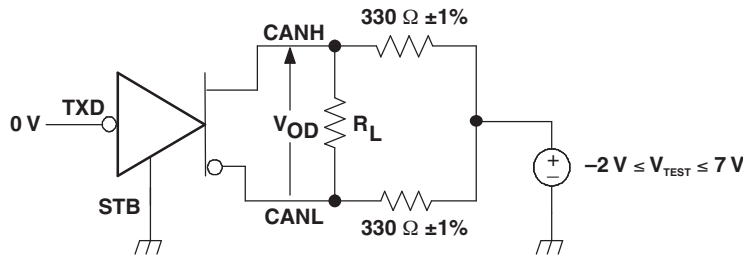


Figure 3. Driver V_{OD} Test Circuit

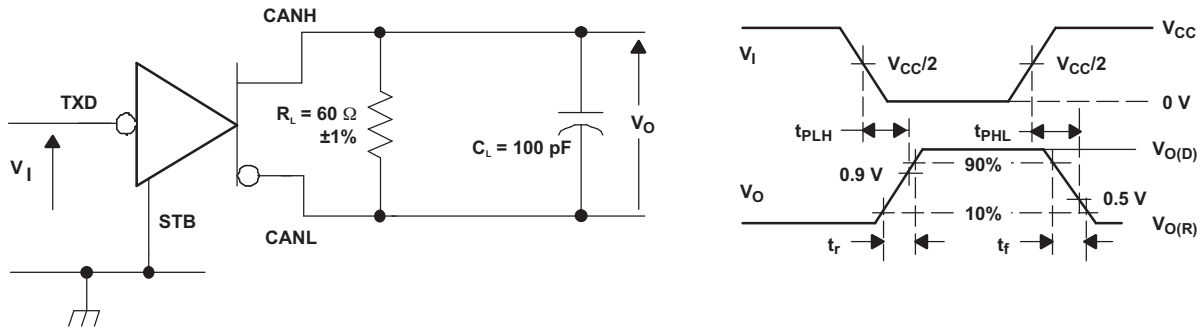


Figure 4. Driver Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

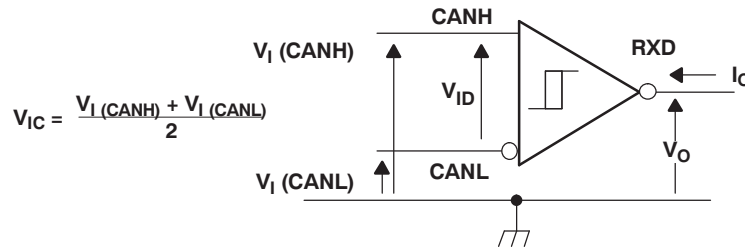
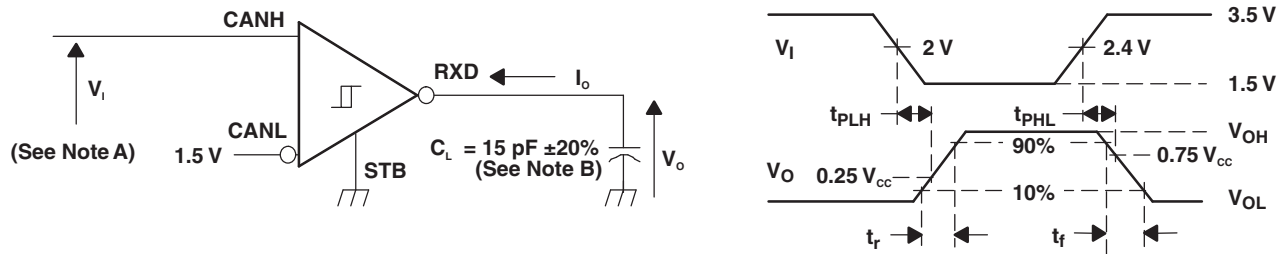


Figure 5. Receiver Voltage and Current Definitions

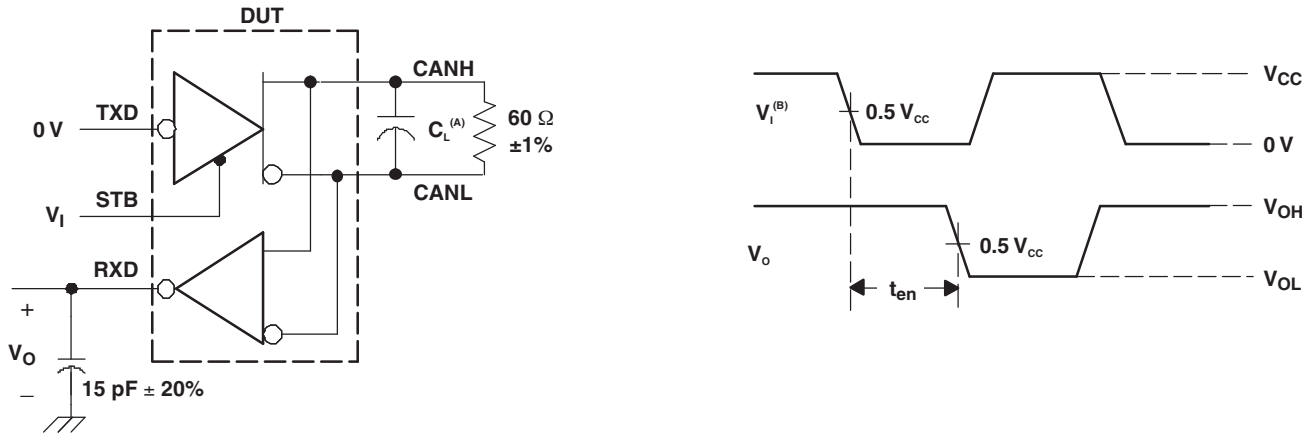


- A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.
- B. C_L includes instrumentation and fixture capacitance within ±20%.

Figure 6. Receiver Test Circuit and Voltage Waveforms

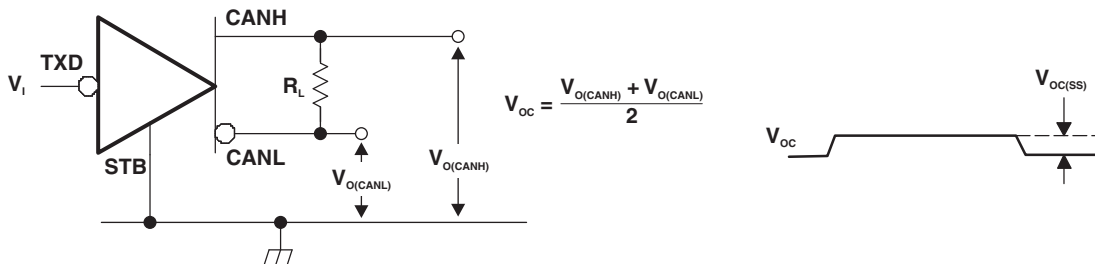
Table 3. Differential Input Voltage Threshold Test

| INPUT | | | OUTPUT | |
|------------|------------|------------|--------|----------|
| V_{CANH} | V_{CANL} | $ V_{ID} $ | R | |
| -11.1 V | -12 V | 900 mV | L | V_{OL} |
| 12 V | 11.1 V | 900 mV | L | |
| -6 V | -12 V | 6 V | L | |
| 12 V | 6 V | 6 V | L | |
| -11.5 V | -12 V | 500 mV | H | V_{OH} |
| 12 V | 11.5 V | 500 mV | H | |
| -12 V | -6 V | 6 V | H | |
| 6 V | 12 V | 6 V | H | |
| Open | Open | X | H | |



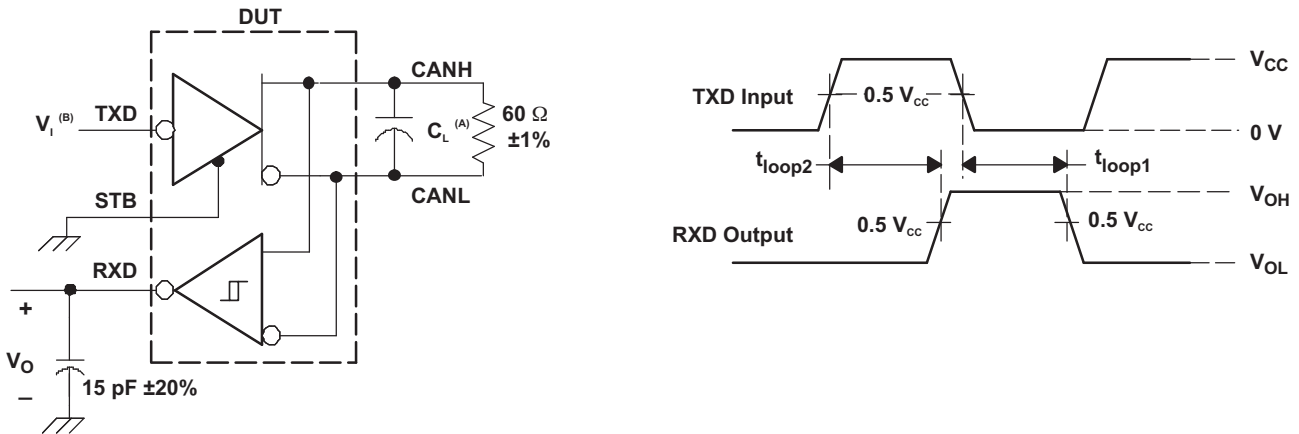
- A. $C_L = 100 \text{ pF}$ and includes instrumentation and fixture capacitance within $\pm 20\%$.
- B. All V_1 input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 6 \text{ ns}$, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 7. t_{en} Test Circuit and Waveforms



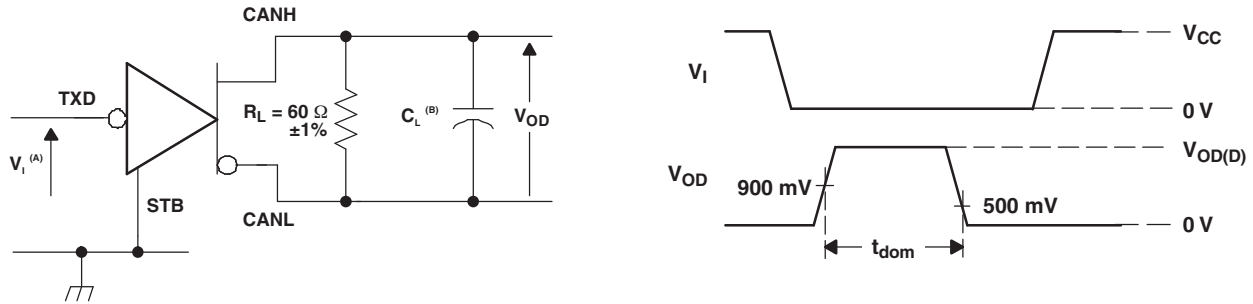
NOTE: All V_1 input pulses are from 0 V to V_{CC} and supplied by a generator having the following characteristics: t_r or $t_f \leq 6 \text{ ns}$, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 8. Common-Mode Output Voltage Test and Waveforms



- A. $C_L = 100 \text{ pF}$ and includes instrumentation and fixture capacitance within $\pm 20\%$.
- B. All V_1 input pulses are from 0 V to V_{CC} and supplied by a generator having the following characteristics: t_r or $t_f \leq 6 \text{ ns}$, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 9. $t_{(LOOP)}$ Test Circuit and Waveforms



- A. All V_1 input pulses are from 0 V to V_{CC} and supplied by a generator having the following characteristics: t_r or $t_f \leq 6$ ns, pulse repetition rate (PRR) = 500 Hz, 50% duty cycle.
- B. $C_L = 100$ pF includes instrumentation and fixture capacitance within $\pm 20\%$.

Figure 10. Dominant Time-Out Test Circuit and Waveforms

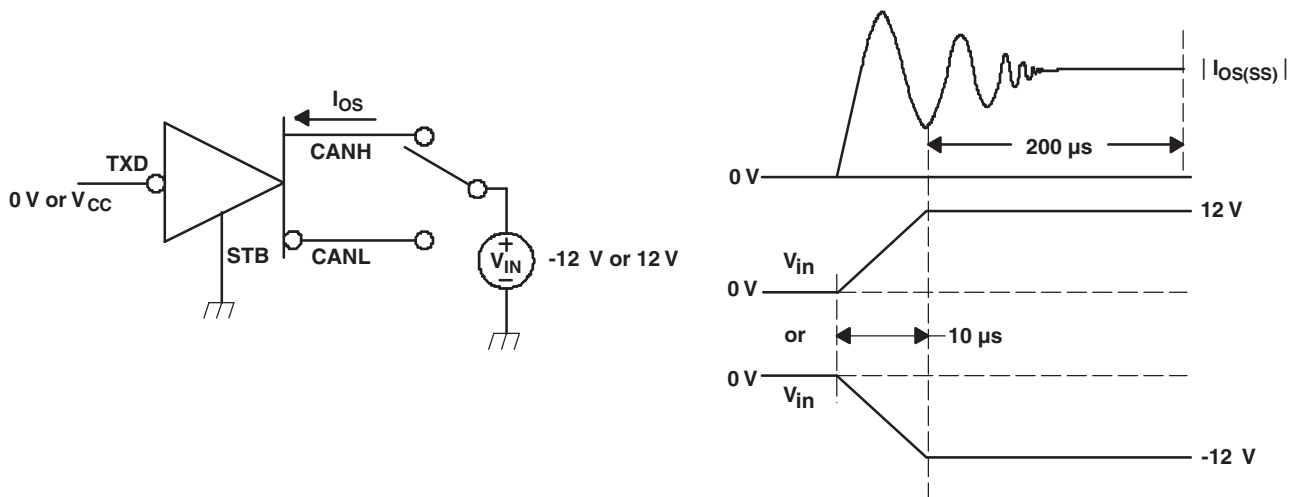
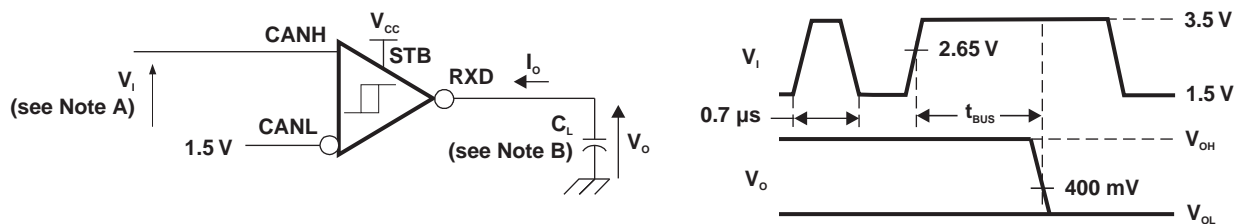
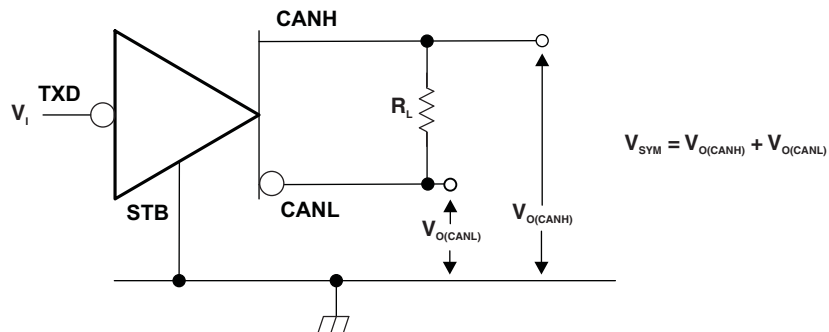


Figure 11. Driver Short-Circuit Current Test and Waveforms



- A. For V_1 bit width ≤ 0.7 μ s, $V_O = V_{OH}$. For V_1 bit width ≥ 5 μ s, $V_O = V_{OL}$. V_1 input pulses are supplied from a generator with the following characteristics: $t_r/t_f < 6$ ns.
- B. $C_L = 15$ pF and includes instrumentation and fixture capacitance within $\pm 20\%$.

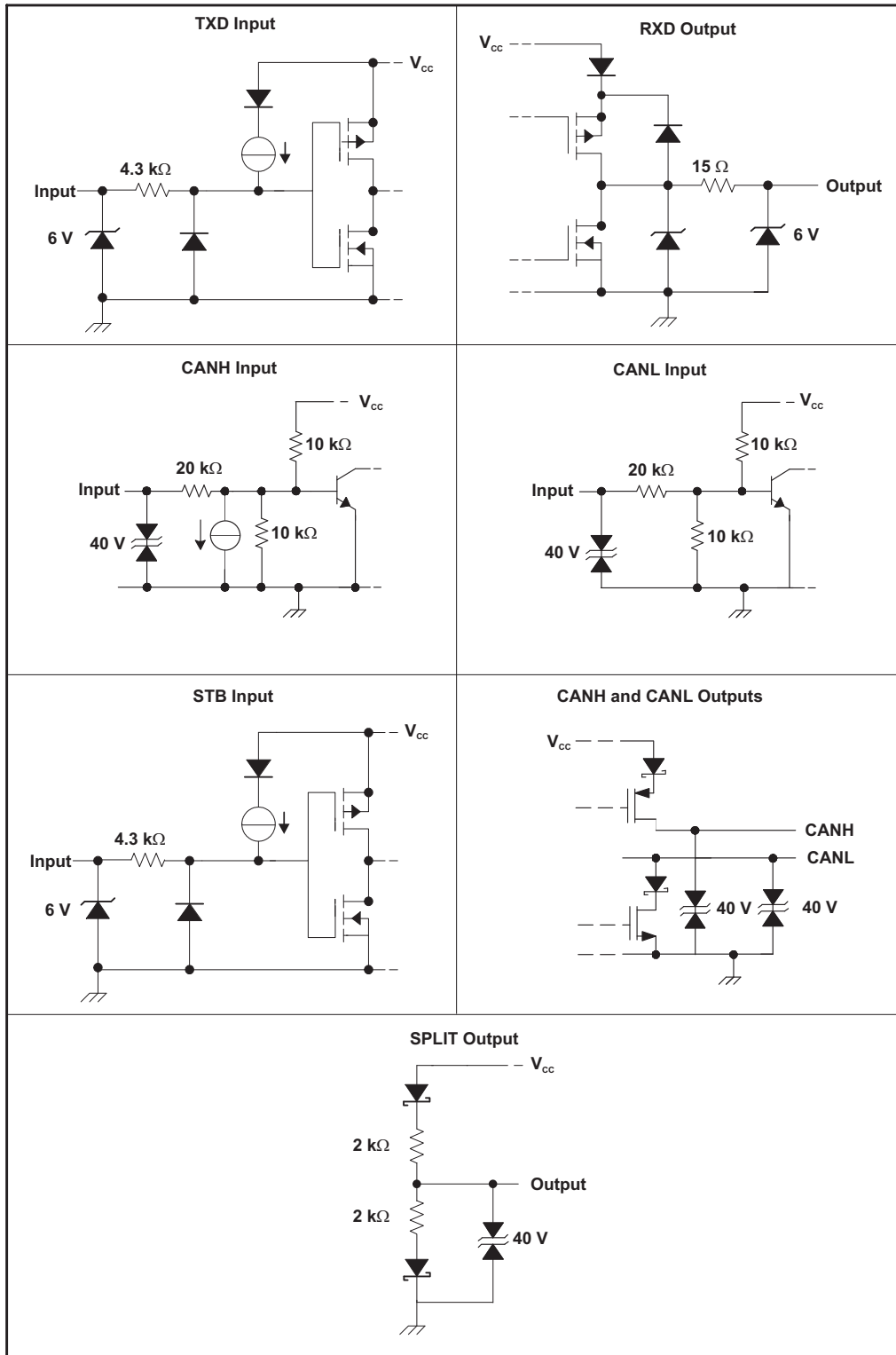
Figure 12. t_{BUS} Test Circuit and Waveforms



- A. All V_I input pulses are from 0 V to V_{CC} and supplied by a generator having the following characteristics: $t_r/t_f \leq 6$ ns, pulse repetition rate (PRR) = 250 kHz, 50% duty cycle.

Figure 13. Driver Output Symmetry Test Circuit

Equivalent Input and Output Schematic Diagrams



APPLICATION INFORMATION

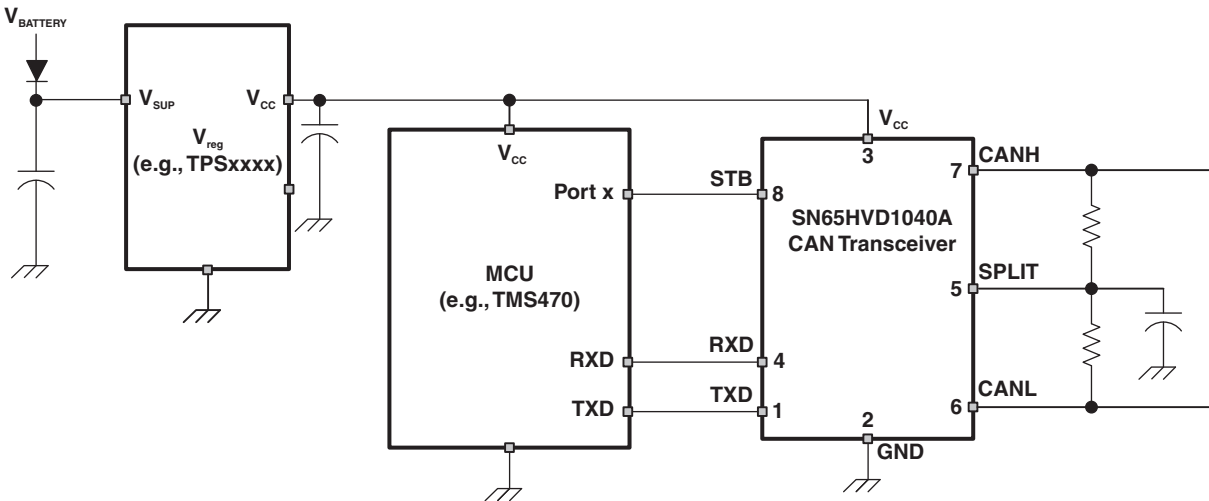


Figure 14. Typical Application Using Split Termination for Stabilization

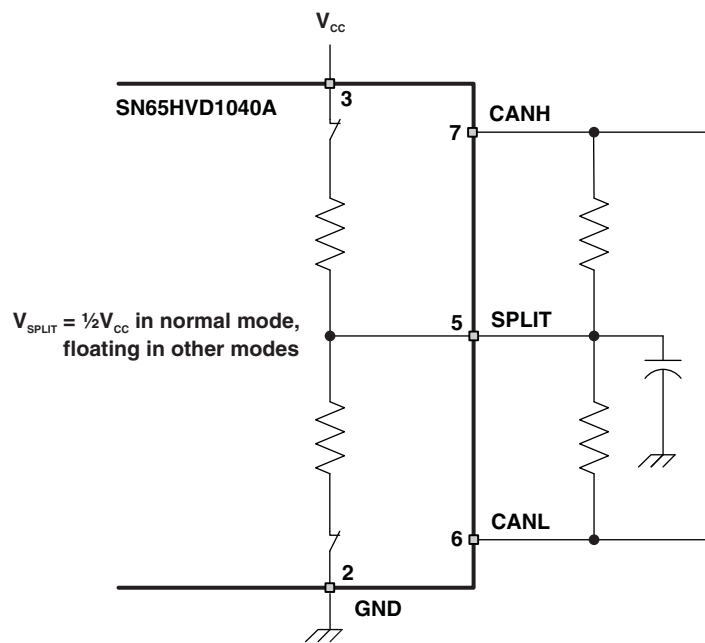


Figure 15. Split Pin Stabilization Circuitry and Application

REVISION HISTORY

Changes from Original (June 2008) to Revision A Page

- Changed V_{CC} Supply voltage range From: -0.3 V to 7 V To: -0.3 V to 6 V [3](#)
 - Changed V_I Voltage input range (TXD, STB) From: -0.5 V to 6 V To: -0.3 V to 6 V [3](#)
-

Changes from Revision A (January 2011) to Revision B Page

- Changed the Driver Function Table foot note to include: Y = weak pull down to GND [7](#)
 - Changed the Split Output diagram [13](#)
-

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/ Ball Finish | MSL Peak Temp ⁽³⁾ | Samples (Requires Login) |
|-------------------|-----------------------|--------------|-----------------|------|-------------|----------------------------|----------------------|------------------------------|-----------------------------|
| SN65HVD1040AQDRQ1 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

TAPE AND REEL INFORMATION

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN65HVD1040AQDRQ1 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN65HVD1040AQDRQ1 | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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