3-V TO 5.5-V MULTICHANNEL RS-232 COMPATIBLE LINE DRIVER/RECEIVER

FEATURES

- **Operates With 3-V to 5.5-V V$_{CC}$ Supply**
- **Always-Active Noninverting Receiver Output (ROUT2B)**
- **Low Standby Current . . . 1 μA Typ**
- **External Capacitors . . . 4 × 0.1 μF**
- **Accepts 5-V Logic Input With 3.3-V Supply**
- **Inter-Operable With SN65C3238, SN75C3238**
- **Supports Operation From 250 kbit/s to 1 Mbit/s**
- **RS-232 Bus-Pin ESD Protection Exceeds ±15 kV Using Human-Body Model (HBM)**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**

APPLICATIONS

- **Battery-Powered Systems**
- **PDAs**
- **Notebooks**
- **Laptops**
- **Palmtop PCs**
- **Hand-Held Equipment**

DB, DW, OR PW PACKAGE
(TOP VIEW)

|		
C2+	1	28	C1+
C2−	2	27	V+
V−	3	26	V$_{CC}$
RIN1	4	25	GND
RIN2	5	24	C1−
RIN3	6	23	FORCEON
RIN4	7	22	$\overline{\text{FORCEOFF}}$
RIN5	8	21	$\overline{\text{INVALID}}$
DOUT1	9	20	ROUT2B
DOUT2	10	19	ROUT1
DOUT3	11	18	ROUT2
DIN3	12	17	ROUT3
DIN2	13	16	ROUT4
DIN1	14	15	ROUT5

DESCRIPTION/ORDERING INFORMATION

The SN65C3243 and SN75C3243 consist of three line drivers, five line receivers, and a dual charge-pump circuit with ±15-kV ESD protection pin to pin (serial-port connection pins, including GND). This device provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. In addition, this device includes an always-active noninverting output (ROUT2B), which allows applications using the ring indicator to transmit data while the device is powered down. The device operates at data signaling rates up to 1 Mbit/s and an increased slew-rate range of 24 V/μs to 150 V/μs.

Flexible control options for power management are available when the serial port is inactive. The auto-powerdown feature functions when FORCEON is low and $\overline{\text{FORCEOFF}}$ is high. During this mode of operation, if the device does not sense a valid RS-232 signal, the driver outputs are disabled. If $\overline{\text{FORCEOFF}}$ is set low, both drivers and receivers (except ROUT2B) are shut off, and the supply current is reduced to 1 μA. Disconnecting the serial port or turning off the peripheral drivers causes the auto-powerdown condition to occur.

Auto-powerdown can be disabled when FORCEON and $\overline{\text{FORCEOFF}}$ are high and should be done when driving a serial mouse. With auto-powerdown enabled, the device is activated automatically when a valid signal is applied to any receiver input. The $\overline{\text{INVALID}}$ output is used to notify the user if an RS-232 signal is present at any receiver input. INVALID is high (valid data) if any receiver input voltage is greater than 2.7 V or less than –2.7 V or has been between –0.3 V and 0.3 V for less than 30 μs. INVALID is low (invalid data) if all receiver input voltages are between –0.3 V and 0.3 V for more than 30 μs. Refer to Figure 5 for receiver input levels.
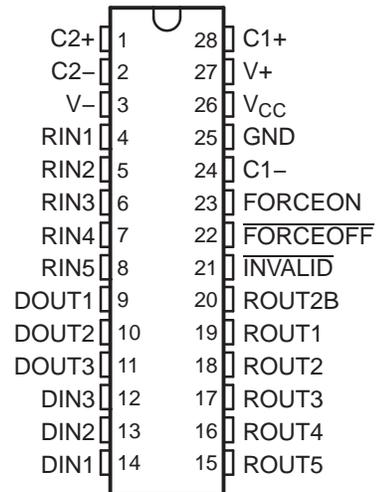
⚠ Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ORDERING INFORMATION

T_A	PACKAGE[1][2]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	SOIC – DW	Tube of 20	SN75C3243DW	75C3243
		Reel of 1000	SN75C3243DWR	
	SSOP – DB	Reel of 2000	SN75C3243DBR	75C3243
	TSSOP – PW	Tube of 50	SN75C3243PW	CA3243
		Reel of 2000	SN75C3243PWR	
−40°C to 85°C	SOIC – DW	Tube of 20	SN65C3243DW	65C3243
		Reel of 1000	SN65C3243DWR	
	SSOP – DB	Reel of 2000	SN65C3243DBR	65C3243
	TSSOP – PW	Tube of 50	SN65C3243PW	CB3243
		Reel of 2000	SN65C3243PWR	

(1) Package drawings, thermal data, symbolization are available at www.ti.com/sc/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

FUNCTION TABLES

EACH DRIVER[1]

INPUTS				OUTPUT DOUT	DRIVER STATUS
DIN	FORCEON	$\overline{\text{FORCEOFF}}$	VALID RIN RS-232 LEVEL		
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with auto-powerdown disabled
H	H	H	X	L	
L	L	H	Yes	H	Normal operation with auto-powerdown enabled
H	L	H	Yes	L	
L	L	H	No	Z	Powered off by auto-powerdown feature
H	L	H	No	Z	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance

EACH RECEIVER[1]

INPUTS				OUTPUTS			RECEIVER STATUS
RIN2	RIN1, RIN3–RIN5	$\overline{\text{FORCEOFF}}$	VALID RIN RS-232 LEVEL	ROUT2B	ROUT2	ROUT1, ROUT3–5	
L	X	L	X	L	Z	Z	Powered off while ROUT2B is active
H	X	L	X	H	Z	Z	
L	L	H	YES	L	H	H	Normal operation with auto-powerdown disabled/enabled
L	H	H	YES	L	L	L	
H	L	H	YES	H	H	H	
H	H	H	YES	H	L	L	
Open	Open	H	YES	L	H	H	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

Product Folder Link(s): *SN65C3243 SN75C3243*

LOGIC DIAGRAM (POSITIVE LOGIC)
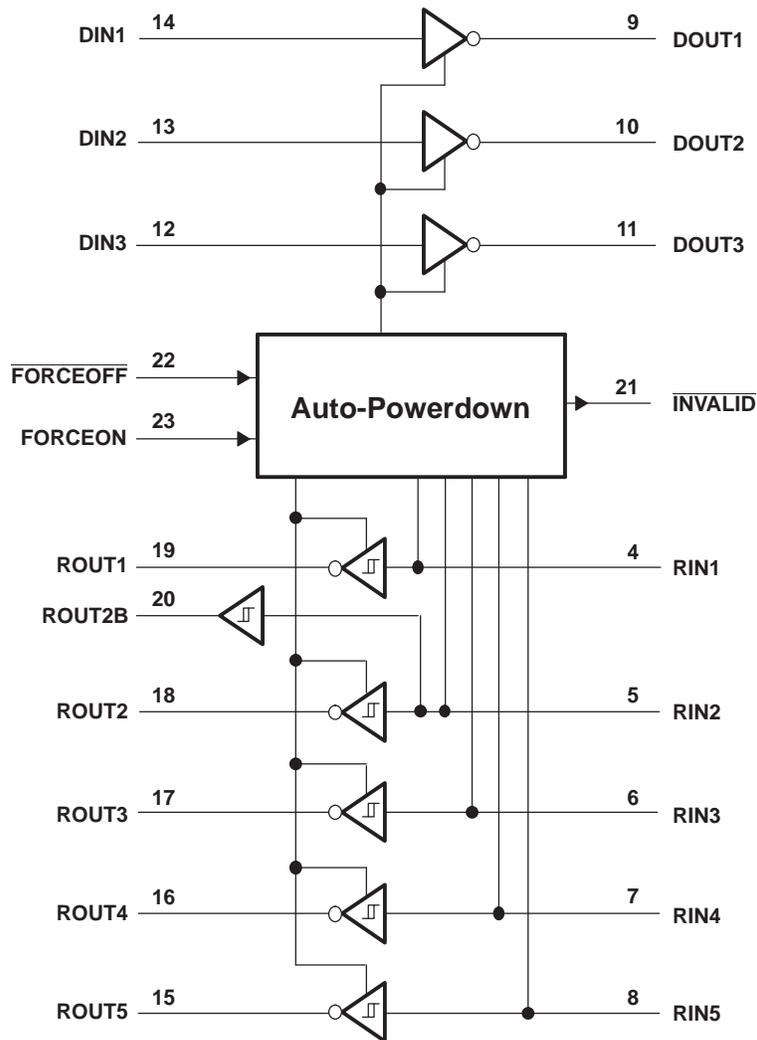
ABSOLUTE MAXIMUM RATINGS[(1)]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range[(2)]		−0.3	6	V
V+	Positive-output supply voltage range[(2)]		−0.3	7	V
V−	Negative-output supply voltage range[(2)]		0.3	−7	V
V+ − V−	Supply voltage difference[(2)]			13	V
V_I	Input voltage range	Driver ($\overline{\text{FORCEOFF}}$, FORCEON)	−0.3	6	V
		Receiver	−25	25	
V_O	Output voltage range	Driver	−13.2	13.2	V
θ_{JA}	Package thermal impedance[(3)][(4)]	DB package		62	°C/W
		DW package		46	
		PW package		62	
T_J	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network GND.
(3) Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) − T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS[(1)]

see Figure 6

				MIN	NOM	MAX	UNIT
	Supply voltage		$V_{CC} = 3.3$ V	3	3.3	3.6	V
			$V_{CC} = 5$ V	4.5	5	5.5	
V_{IH}	Driver and control high-level input voltage	DIN, $\overline{\text{FORCEOFF}}$, FORCEON	$V_{CC} = 3.3$ V	2			V
			$V_{CC} = 5$ V	2.4			
V_{IL}	Driver and control low-level input voltage	DIN, $\overline{\text{FORCEOFF}}$, FORCEON				0.8	V
V_I	Driver and control input voltage	DIN, $\overline{\text{FORCEOFF}}$, FORCEON		0		5.5	V
V_I	Receiver input voltage			−25		25	V
T_A	Operating free-air temperature	SN65C3243		−40		85	°C
		SN75C3243		0		70	

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

ELECTRICAL CHARACTERISTICS[(1)]

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 6)

PARAMETER			TEST CONDITIONS	MIN	TYP[(2)]	MAX	UNIT
I_I	Input leakage current	$\overline{\text{FORCEOFF}}$, FORCEON			±0.01	±1	µA
I_{CC}	Supply current	Auto-powerdown disabled	No load, $\overline{\text{FORCEOFF}}$ and FORCEON = V_{CC}		0.3	1	mA
		Powered off	No load, $\overline{\text{FORCEOFF}}$ = GND		1	10	µA
		Auto-powerdown enabled	No load, $\overline{\text{FORCEOFF}}$ = V_{CC}, FORCEON = GND, All RIN are open or grounded, All DIN are grounded		1	10	

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

Product Folder Link(s): SN65C3243 SN75C3243

DRIVER SECTION

Electrical Characteristics[1]

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 6)

	PARAMETER	TEST CONDITIONS		MIN	TYP[2]	MAX	UNIT
V_{OH}	High-level output voltage	All DOUT at R_L = 3 kΩ to GND		5	5.4		V
V_{OL}	Low-level output voltage	All DOUT at R_L = 3 kΩ to GND		−5	−5.4		V
V_O	Output voltage (mouse driveability)	DIN1 = DIN2 = GND, DIN3 = V_{CC}, 3-kΩ to GND at DOUT3, DOUT1 = DOUT2 = 2.5 mA		±5			V
I_{IH}	High-level input current	$V_I = V_{CC}$			±0.01	±1	µA
I_{IL}	Low-level input current	V_I = GND			±0.01	±1	µA
I_{OS}	Short-circuit output current[3]	V_{CC} = 3.6 V,	V_O = 0 V		±35	±60	mA
		V_{CC} = 5.5 V,	V_O = 0 V		±35	±90	
r_o	Output resistance	V_{CC}, V+, and V− = 0 V,	V_O = ±2 V	300	10M		Ω
I_{off}	Output leakage current	$\overline{FORCEOFF}$ = GND	V_O = ±12 V, $\quad$ V_{CC} = 3 V to 3.6 V			±25	µA
			V_O = ±10 V, $\quad$ V_{CC} = 4.5 V to 5.5 V			±25	

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(3) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

Switching Characteristics[1]

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 6)

	PARAMETER	TEST CONDITIONS			MIN	TYP[2]	MAX	UNIT
	Maximum data rate (see Figure 1)	R_L = 3 kΩ, One DOUT switching	C_L = 1000 pF		250			kbit/s
			C_L = 250 pF,	V_{CC} = 3 V to 4.5 V	1000			
			C_L = 1000 pF,	V_{CC} = 4.5 V to 5.5 V	1000			
$t_{sk(p)}$	Pulse skew[3]	C_L = 150 pF to 2500 pF,	R_L = 3 kΩ to 7 kΩ,	See Figure 2		25		ns
SR(tr)	Slew rate, transition region (see Figure 1)	C_L = 150 pF to 1000 pF,	R_L = 3 kΩ to 7 kΩ,	V_{CC} = 3.3 V	18		150	V/µs

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(3) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

RECEIVER SECTION

Electrical Characteristics[1]

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 6)

	PARAMETER	TEST CONDITIONS	MIN	TYP[2]	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -1$ mA	$V_{CC} - 0.6$	$V_{CC} - 0.1$		V
V_{OL}	Low-level output voltage	$I_{OL} = 1.6$ mA			0.4	V
V_{IT+}	Positive-going input threshold voltage	$V_{CC} = 3.3$ V		1.6	2.4	V
		$V_{CC} = 5$ V		1.9	2.4	
V_{IT-}	Negative-going input threshold voltage	$V_{CC} = 3.3$ V	0.6	1.1		V
		$V_{CC} = 5$ V	0.8	1.4		
V_{hys}	Input hysteresis ($V_{IT+} - V_{IT-}$)			0.5		V
I_{off}	Output leakage current (except ROUT2B)	$\overline{FORCEOFF} = 0$ V		±0.05	±10	µA
r_i	Input resistance	$V_I = \pm3$ V to ±25 V	3	5	7	kΩ

(1)   Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.
(2)   All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

Switching Characteristics[1]

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	TYP[2]	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 150 pF, See Figure 3	150	ns
t_{PHL}	Propagation delay time, high- to low-level output	C_L = 150 pF, See Figure 3	150	ns
t_{en}	Output enable time	C_L = 150 pF, R_L = 3 kΩ, See Figure 4	200	ns
t_{dis}	Output disable time	C_L = 150 pF, R_L = 3 kΩ, See Figure 4	200	ns
$t_{sk(p)}$	Pulse skew[3]	See Figure 3	50	ns

(1)   Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.
(2)   All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(3)   Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

Product Folder Link(s): *SN65C3243 SN75C3243*

AUTO-POWERDOWN SECTION

Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5)

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
$V_{T+(valid)}$	Receiver input threshold for $\overline{INVALID}$ high-level output voltage	FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}		2.7	V
$V_{T-(valid)}$	Receiver input threshold for $\overline{INVALID}$ high-level output voltage	FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}	−2.7		V
$V_{T(invalid)}$	Receiver input threshold for $\overline{INVALID}$ low-level output voltage	FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}	−0.3	0.3	V
V_{OH}	$\overline{INVALID}$ high-level output voltage	I_{OH} = −1 mA, FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}	V_{CC} − 0.6		V
V_{OL}	$\overline{INVALID}$ low-level output voltage	I_{OL} = 1.6 mA, FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}		0.4	V

Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5)

	PARAMETER	TYP[1]	UNIT
t_{valid}	Propagation delay time, low- to high-level output	1	μs
$t_{invalid}$	Propagation delay time, high- to low-level output	30	μs
t_{en}	Supply enable time	100	μs

(1)   All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION
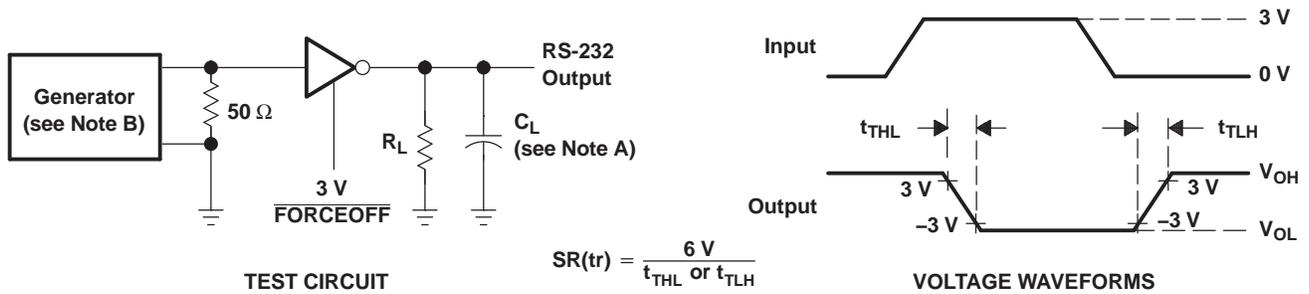
TEST CIRCUIT

$$SR(tr) = \frac{6\ V}{t_{THL}\ or\ t_{TLH}}$$

VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
        B. The pulse generator has the following characteristics: PRR = 1 Mbit/s, Z_O = 50 Ω, 50% duty cycle, $t_r \leq$ 10 ns, $t_f \leq$ 10 ns.

Figure 1. Driver Slew Rate
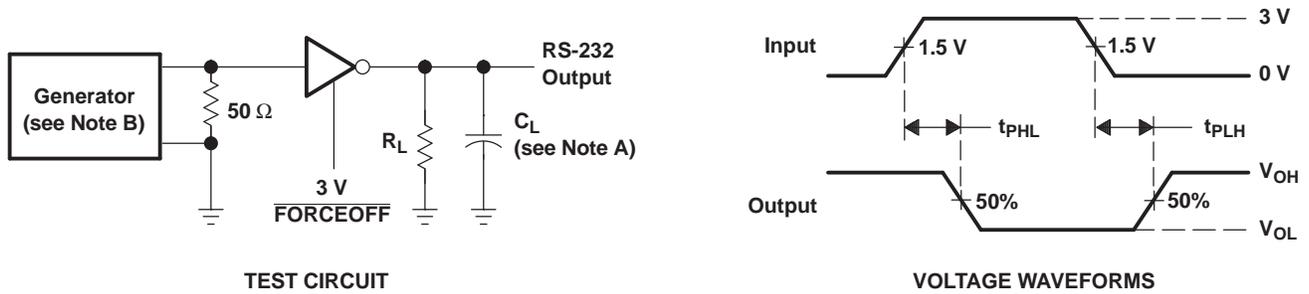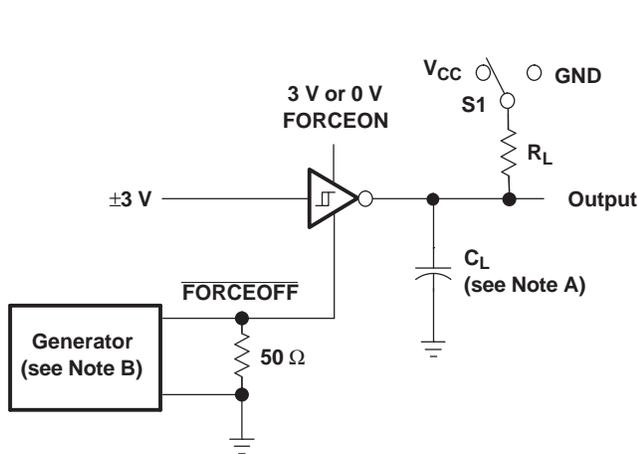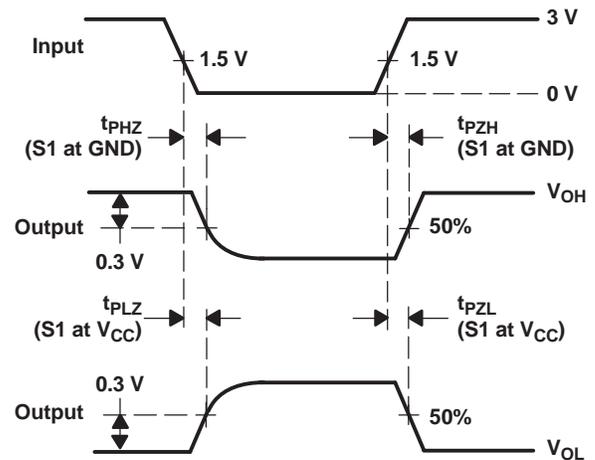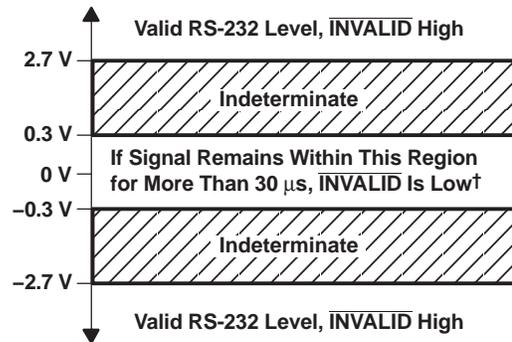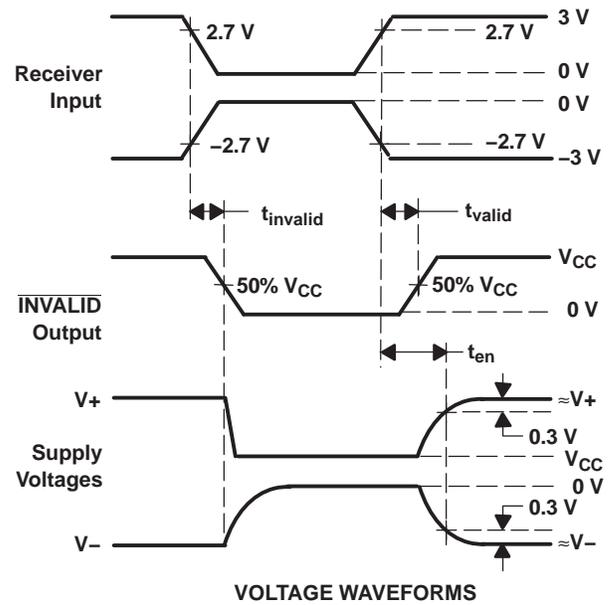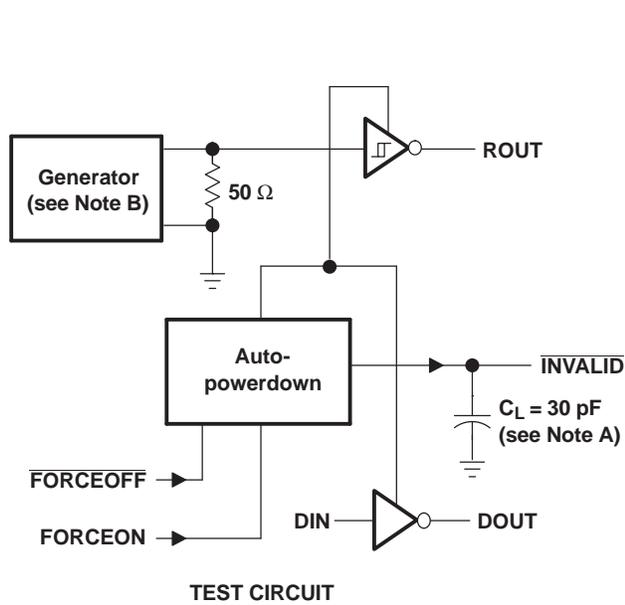
TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
        B. The pulse generator has the following characteristics: PRR = 1 Mbit/s, Z_O = 50 Ω, 50% duty cycle, $t_r \leq$ 10 ns, $t_f \leq$ 10 ns.

Figure 2. Driver Pulse Skew
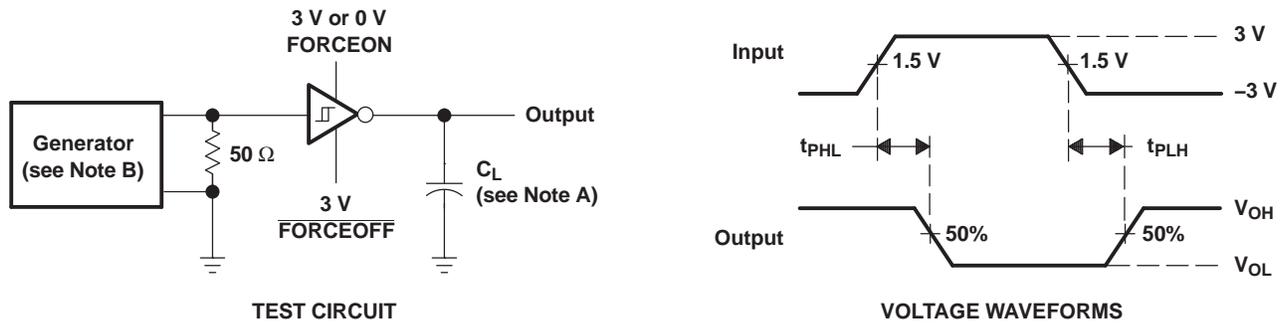
TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
        B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, $t_r \leq$ 10 ns, $t_f \leq$ 10 ns.

Figure 3. Receiver Propagation Delay Times

Product Folder Link(s): *SN65C3243 SN75C3243*

PARAMETER MEASUREMENT INFORMATION (continued)

TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
           B. The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.
           C. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
           D. t_{PZL} and t_{PZH} are the same as t_{en}.

Figure 4. Receiver Enable and Disable Times

PARAMETER MEASUREMENT INFORMATION (continued)

TEST CIRCUIT

VOLTAGE WAVEFORMS

Valid RS-232 Level, $\overline{\text{INVALID}}$ High

Indeterminate

If Signal Remains Within This Region
for More Than 30 μs, $\overline{\text{INVALID}}$ Is Low[†]

Indeterminate

Valid RS-232 Level, $\overline{\text{INVALID}}$ High

[†] Auto-powerdown disables drivers and reduces supply
current to 1 μA.

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 5 kbit/s, Z_O = 50 Ω, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

Figure 5. $\overline{\text{INVALID}}$ Propagation Delay Times and Supply Enabling Time

PARAMETER MEASUREMENT INFORMATION (continued)
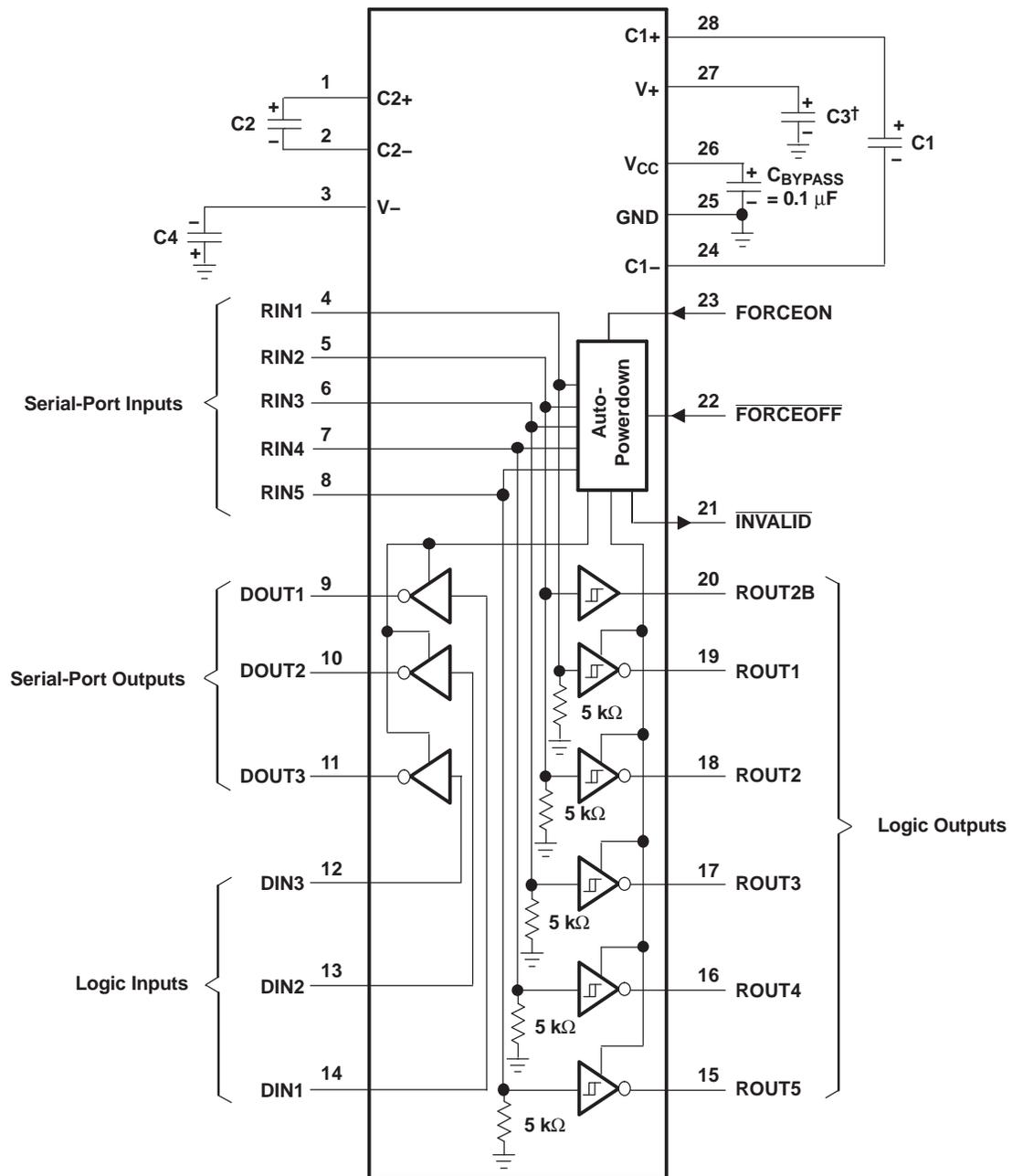
† C3 can be connected to V_{CC} or GND.
NOTE A: Resistor values shown are nominal.

V_{CC} vs CAPACITOR VALUES

V_{CC}	C1	C2, C3, and C4
3.3 V ± 0.3 V	0.1 μF	0.1 μF
5 V ± 0.5 V	0.047 μF	0.33 μF
3 V to 5.5 V	0.1 μF	0.47 μF

Figure 6. Typical Operating Circuit and Capacitor Values

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN65C3243DBR	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C3243	Samples
SN65C3243DBRE4	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C3243	Samples
SN65C3243DBRG4	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C3243	Samples
SN65C3243DW	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C3243	Samples
SN65C3243DWE4	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C3243	Samples
SN65C3243DWG4	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C3243	Samples
SN65C3243DWR	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C3243	Samples
SN65C3243DWRE4	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C3243	Samples
SN65C3243DWRG4	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C3243	Samples
SN65C3243PW	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3243	Samples
SN65C3243PWE4	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3243	Samples
SN65C3243PWG4	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3243	Samples
SN65C3243PWR	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3243	Samples
SN65C3243PWRE4	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3243	Samples
SN65C3243PWRG4	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3243	Samples
SN75C3243DBR	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75C3243	Samples
SN75C3243DBRE4	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75C3243	Samples

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24-Jan-2013

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN75C3243DBRG4	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75C3243	Samples
SN75C3243DW	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75C3243	Samples
SN75C3243DWE4	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75C3243	Samples
SN75C3243DWG4	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75C3243	Samples
SN75C3243DWR	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75C3243	Samples
SN75C3243DWRE4	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75C3243	Samples
SN75C3243DWRG4	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75C3243	Samples
SN75C3243PW	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	CA3243	Samples
SN75C3243PWE4	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	CA3243	Samples
SN75C3243PWG4	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	CA3243	Samples
SN75C3243PWR	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	CA3243	Samples
SN75C3243PWRE4	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	CA3243	Samples
SN75C3243PWRG4	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	CA3243	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65C3243DBR	SSOP	DB	28	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN65C3243DWR	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
SN65C3243PWR	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
SN65C3243PWR	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
SN75C3243DBR	SSOP	DB	28	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN75C3243DWR	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
SN75C3243PWR	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

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PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS
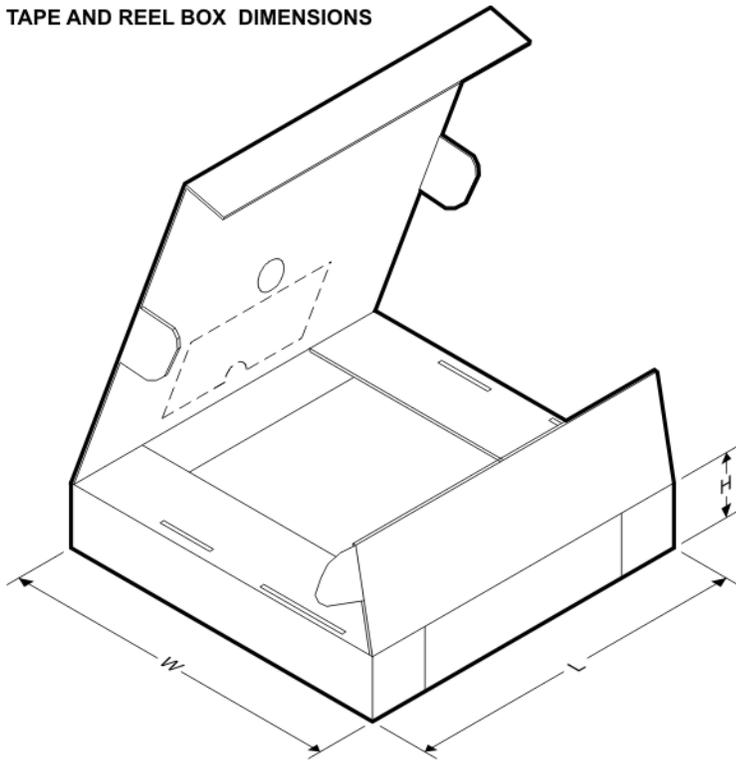
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65C3243DBR	SSOP	DB	28	2000	367.0	367.0	38.0
SN65C3243DWR	SOIC	DW	28	1000	367.0	367.0	55.0
SN65C3243PWR	TSSOP	PW	28	2000	367.0	367.0	38.0
SN65C3243PWR	TSSOP	PW	28	2000	367.0	367.0	38.0
SN75C3243DBR	SSOP	DB	28	2000	367.0	367.0	38.0
SN75C3243DWR	SOIC	DW	28	1000	367.0	367.0	55.0
SN75C3243PWR	TSSOP	PW	28	2000	367.0	367.0	38.0

DW (R−PDSO−G28)   PLASTIC SMALL OUTLINE

0.713 (18,10)
─────────────
0.697 (17,70)

28   15

0.419 (10,63)
─────────────
0.393 (9,97)

0.299 (7,60)
────────────
0.291 (7,40)

1

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
────────────
0.012 (0,31)

14

⊕ | 0.010 (0,25) Ⓜ

0.104 (2,65) Max

0.012 (0,30)
────────────
0.004 (0,10)

0.013 (0,33)
────────────
0.008 (0,20)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°–8°

0.050 (1,27)
────────────
0.016 (0,40)
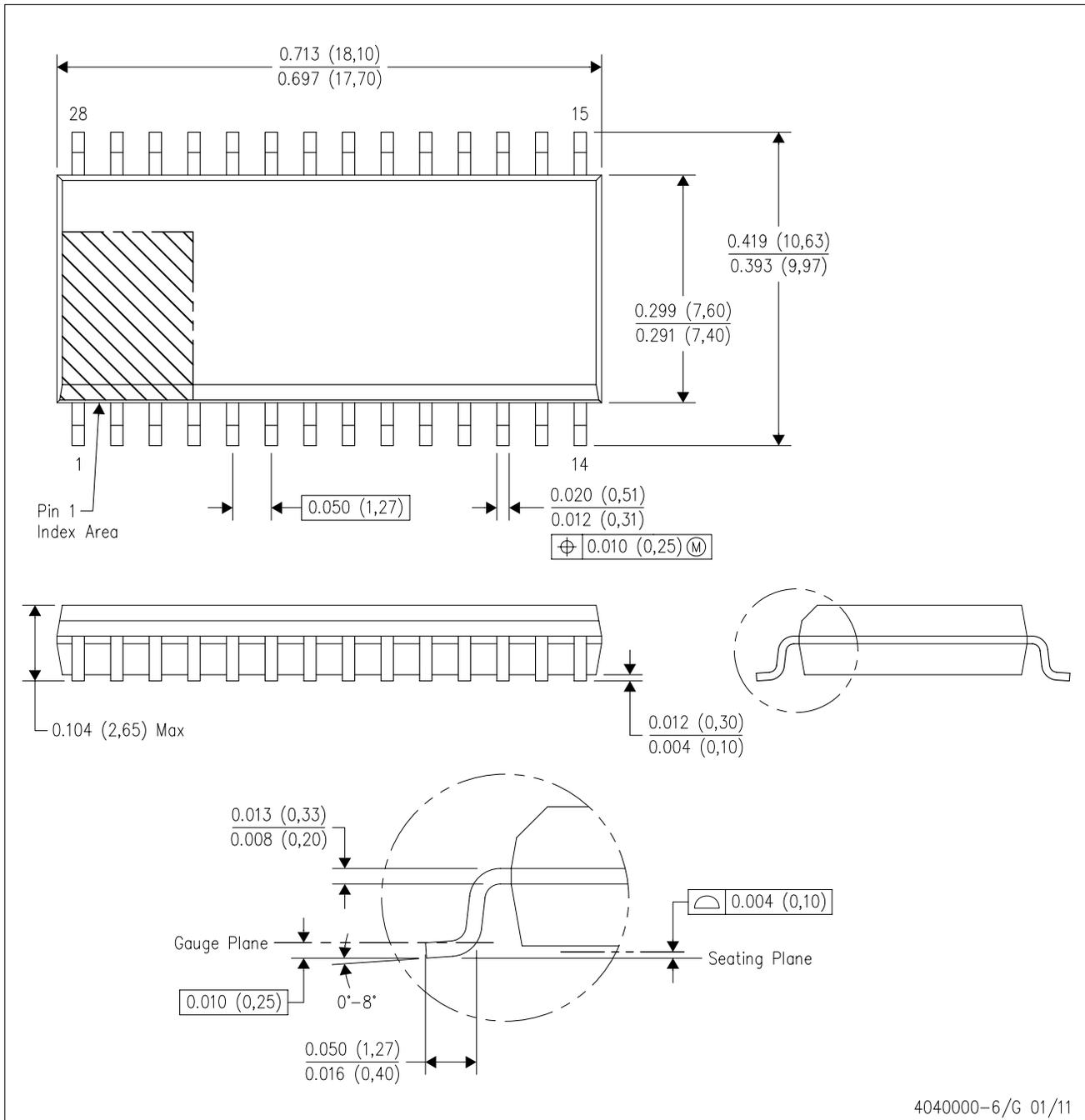
4040000−6/G 01/11

NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M−1994.
         B. This drawing is subject to change without notice.
         C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
         D. Falls within JEDEC MS−013 variation AE.
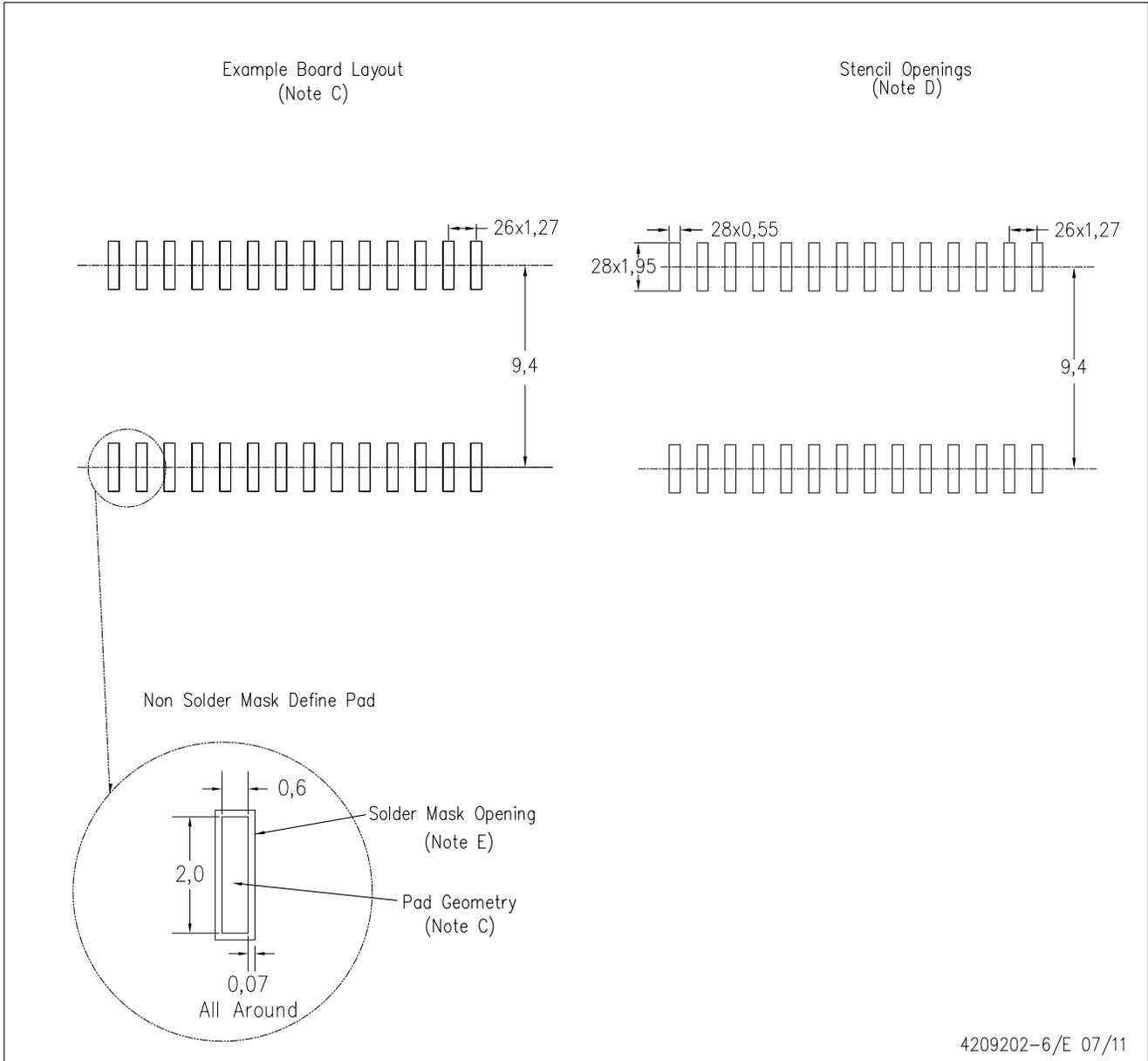
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DW (R−PDSO−G28)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

Stencil Openings
(Note D)

26x1,27

28x0,55

26x1,27

28x1,95

9,4

9,4

Non Solder Mask Define Pad

0,6

Solder Mask Opening
(Note E)

2,0

Pad Geometry
(Note C)

0,07
All Around

4209202−6/E 07/11

NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
         C. Refer to IPC7351 for alternate board design.
         D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
             contact their board assembly site for stencil design recommendations. Refer to IPC−7525
         E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R−PDSO−G28) PLASTIC SMALL OUTLINE

0,65

0,30
0,19

⊕ 0,10 Ⓜ

28   15

D 4,50
   4,30

6,60
6,20

1   14

9,80
9,60

C

0,15 NOM

Gage Plane

0°−8°

0,25

0,75
0,50

1,20 MAX

0,15
0,05

Seating Plane

⌒ 0,10
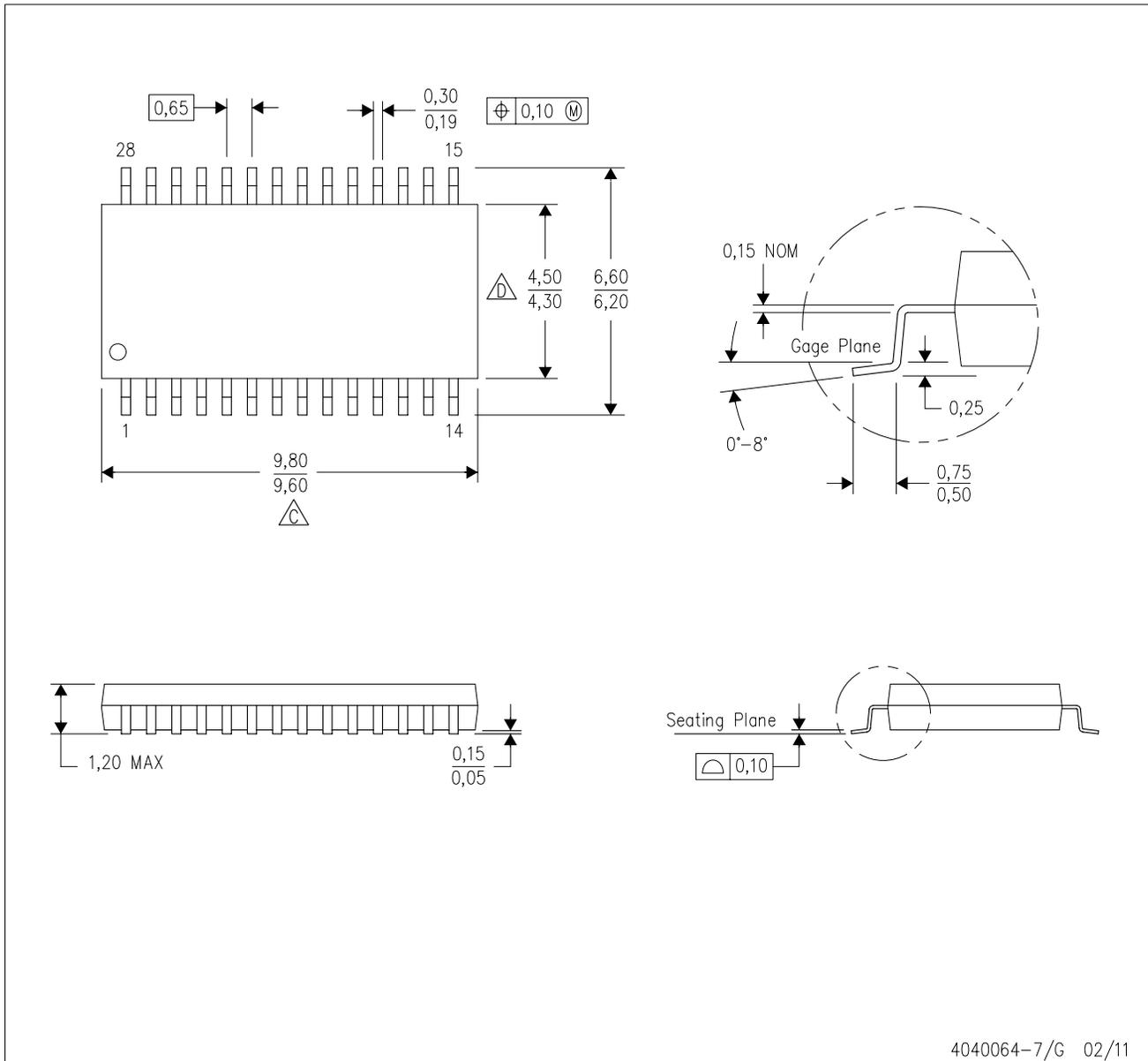
4040064−7/G 02/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
        B. This drawing is subject to change without notice.
        C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
            not exceed 0,15 each side.
        D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
        E. Falls within JEDEC MO−153

PW (R−PDSO−G28)   PLASTIC SMALL OUTLINE

Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).

26x0,65

28x0,25

1,55

5,60

5,60

26x0,65

Example
Non Soldermask Defined Pad

0,3

Example
Solder Mask Opening
(See Note F)

1,6

Pad Geometry

0,07 All Around

4211284−6/F   12/12

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Publication IPC−7351 is recommended for alternate design.
         D.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
         E.   Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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PW (R−PDSO−G28)   PLASTIC SMALL OUTLINE

Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).

26x0,65

28x0,25   1,55

5,60

5,60

26x0,65

Example
Non Soldermask Defined Pad

0,3

Example
Solder Mask Opening
(See Note F)

1,6

Pad Geometry

0,07 All Around

4211284−6/F   12/12

NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
         C. Publication IPC−7351 is recommended for alternate design.
         D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
             contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
         E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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DB (R-PDSO-G**) PLASTIC SMALL-OUTLINE

28 PINS SHOWN
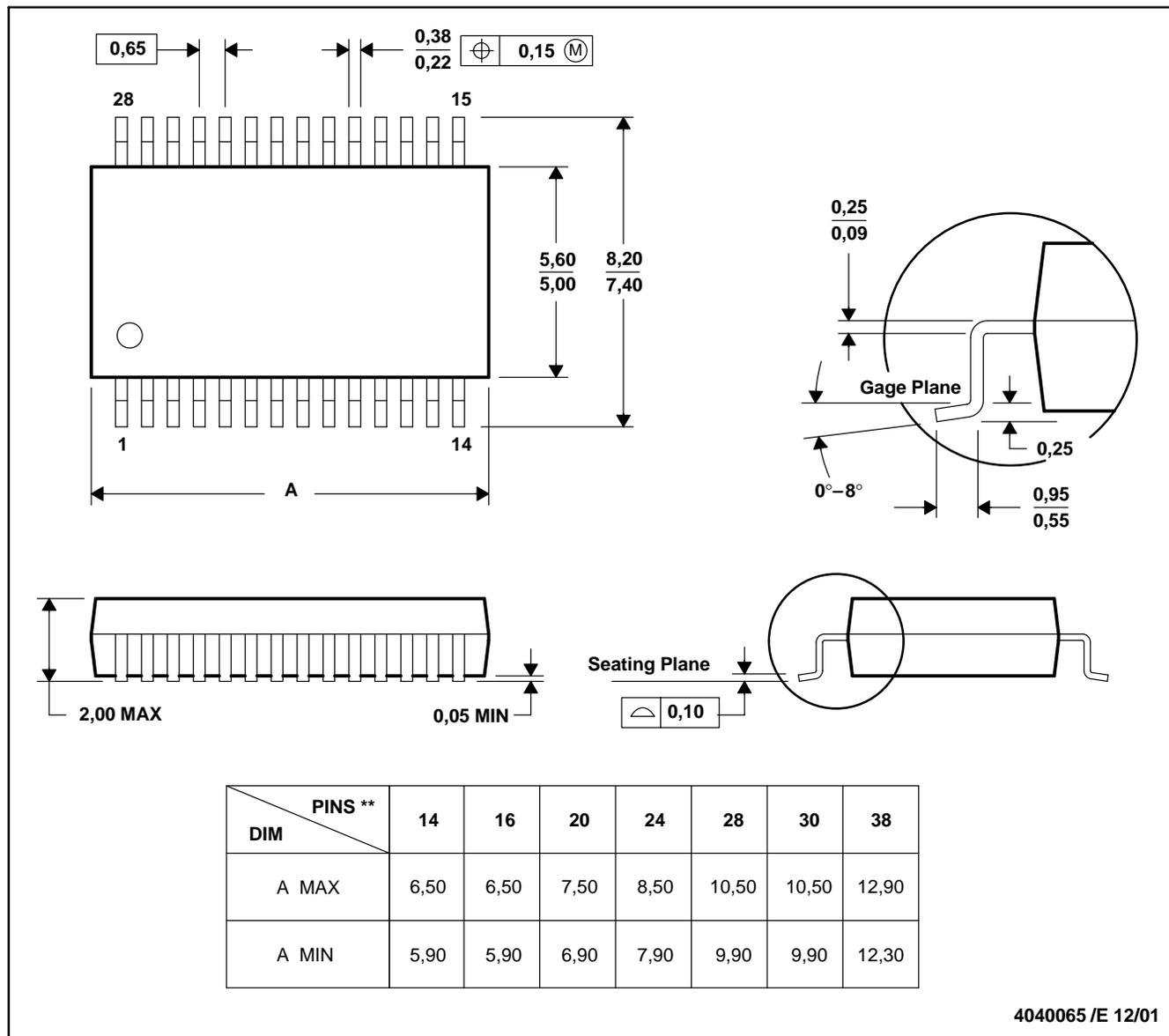
PINS ** DIM	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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