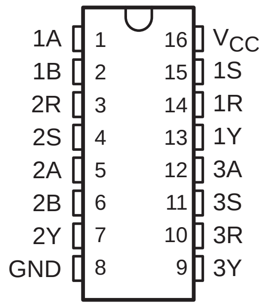
N8T14, SN55122, SN75122
TRIPLE LINE RECEIVERS

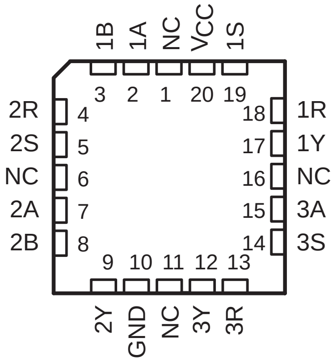
SLLS075B – D1334, SEPTEMBER 1973 – REVISED FEBRUARY 1993

- **Designed for Digital Data Transmission Over Coaxial Cable, Strip Line, or Twisted Pair**
- **Designed for Operation With 50-Ω to 500-Ω Transmission Lines**
- **TTL Compatible**
- **Single 5-V Supply**
- **Built-Input Threshold Hysteresis**
- **High-Speed . . . Typical Propagation Delay Time = 20 ns**
- **Independent Channel Strobes**
- **Input Gating Increases Application Flexibility**
- **Fanout to 10 Series 54/74 Standard Loads**
- **Can Be Used With Dual Line Drivers SN55121 and SN75121**
- **Interchangeable With Signetics N8T14**

SN55122 . . . J PACKAGE
N8T14, SN75122 . . . D OR N PACKAGE
(TOP VIEW)



SN55122 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

THE N8T14 AND SN75122 ARE NOT RECOMMENDED FOR NEW DESIGN

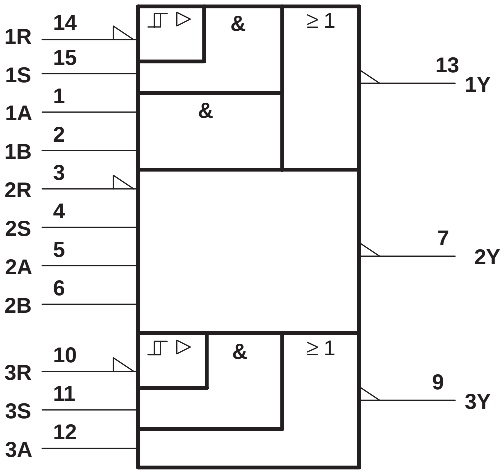
description

The N8T14, SN55122, and SN75122 are triple line receivers that are designed for digital data transmission over lines having impedances from 50 Ω to 500 Ω. They are also compatible with standard TTL-logic and supply voltage levels.

The N8T14, SN55122, and SN75122 have receiver inputs with built-in hysteresis to provide increased noise margin for single-ended systems. The high impedance of this input presents a minimum load to the driver and allows termination of the transmission line in its characteristic impedance to minimize line reflection. An open line will affect the receiver input as would a low-level voltage. The receiver can withstand a level of –0.15 V with power on or off. The other inputs are in TTL configuration. The S input must be high to enable the receiver input. Two of the line receivers have A and B inputs that, if both are high, will hold the output low. The third receiver has only an A input that, if high, will hold the output low.

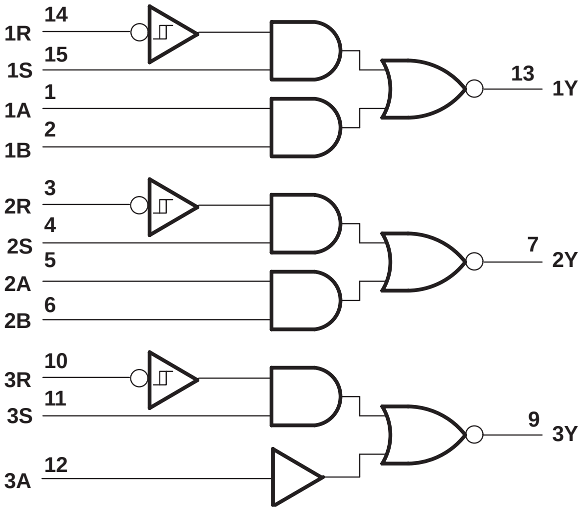
The SN55122 is characterized for operation over the full military temperature range of –55°C to 125°C. The N8T14 and SN75122 are characterized for operation from 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

logic diagram

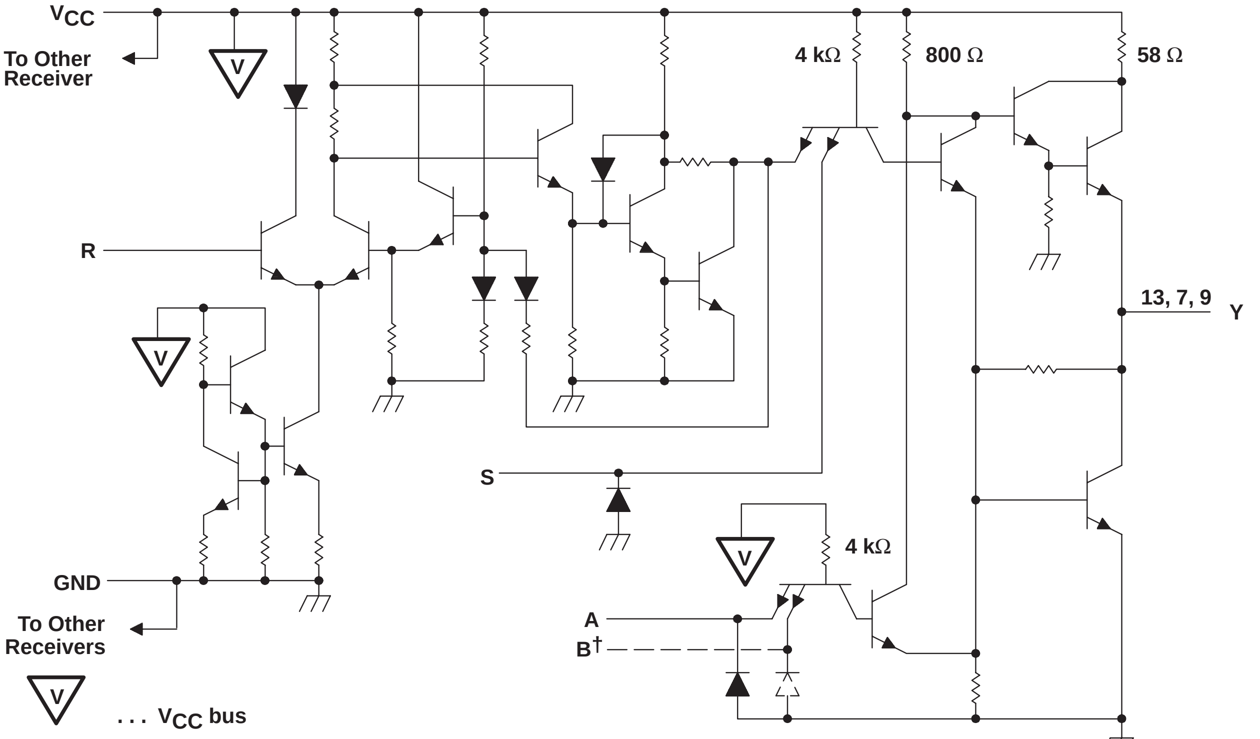


FUNCTION TABLE

INPUTS				OUTPUT
A	B‡	R	S	Y
H	H	X	X	L
X	X	L	H	L
L	X	H	X	H
L	X	X	L	H
X	L	H	X	H
X	L	X	L	H

‡ B input and last two lines of the function table are applicable to receivers 1 and 2 only.
H = high level, L = low level, X = irrelevant

schematic diagram (each receiver)



† B input is provided on receivers 1 and 2 only.
Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)		6 V
Input voltage:	R input	6 V
	A, B, or S input	5.5 V
Output voltage		6 V
Output current		±100 mA
Continuous total power dissipation (see Note 2)		See Dissipation Rating Table
Operating free-air temperature range:	SN55122	−55°C to 125°C
	N8T14, SN75122	0°C to 70°C
Storage temperature range		−65°C to 150°C
Case temperature for 60 seconds: FK package		260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package		300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package		260°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. The SN55122 chips are alloy mounted, and the SN75122 chips are glass mounted.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	–
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	–

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}	A, B, R, or S	2			V
Low-level input voltage, V_{IL}	A, B, R, or S			0.8	V
High-level output current, I_{OH}				–500	µA
Low-level output current, I_{OL}				16	mA
Operating free-air temperature, T_A	SN55122	–55		125	°C
	SN75122	0		70	

electrical characteristics over recommended operating free-air temperature, V_{CC} = 4.75 V to 5.25 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)	R	V_{CC} = 5 V, T_A = 25°C, See Figures 2 and 4	0.3	0.6		V
V_{IK}	Input clamp voltage	A, B, or S	V_{CC} = 5 V, I_I = –12 mA			–1.5	V
$V_{I(BR)}$	Input breakdown voltage	A, B, or S	V_{CC} = 5 V, I_I = 10 mA	5.5			V
V_{OH}	High-level output voltage		V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = –500 µA	2.6			V
			$V_{I(A)}$ = 0, $V_{I(B)}$ = 0, $V_{I(S)}$ = 2 V, $V_{I(R)}$ = 1.45 V, I_{OH} = –500 µA, See Note 3	2.6			
V_{OL}	Low-level output voltage		V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.4	V
			$V_{I(A)}$ = 0, $V_{I(B)}$ = 0, $V_{I(S)}$ = 2 V, $V_{I(R)}$ = 1.45 V, I_{OL} = 16 mA, See Note 4			0.4	
I_{IH}	High-level input current	A, B, or S	V_I = 4.5 V			40	µA
		R	V_I = 3.8 V			170	
I_{IL}	Low-level input current	A, B, or S	V_I = 0.4 V, V_{IR} = 0.8 V	–0.1		–1.6	mA
I_{OS}‡	Short-circuit output current		V_{CC} = 5 V, T_A = 25°C	–50		–100	mA
I_{CCH}	High-level supply current		V_{CC} = MAX, All inputs at 0.8 V, Outputs open			72	mA
I_{CCL}	Low-level supply current		V_{CC} = MAX, All inputs at 2 V, Outputs open			100	mA

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

‡ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

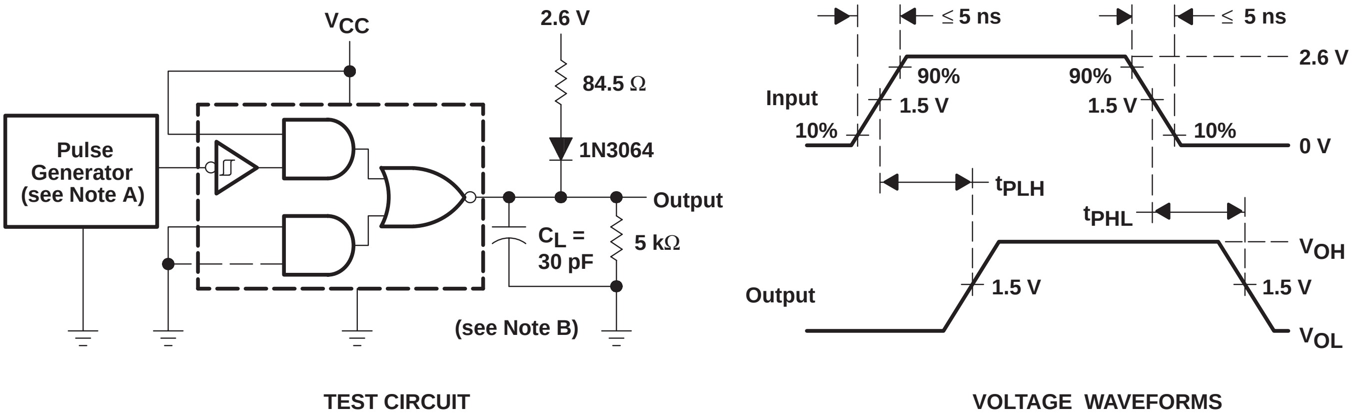
NOTES: 3. The receiver input is high immediately before being reduced to 1.45 V.

4. The receiver input is low immediately before being increased to 1.45 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from R input	See Figure 1		20	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output from R input			20	30	

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, t_W = 200 ns, duty cycle = 50%, PRR ≤ 500 kHz.
B. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
INPUT VOLTAGE

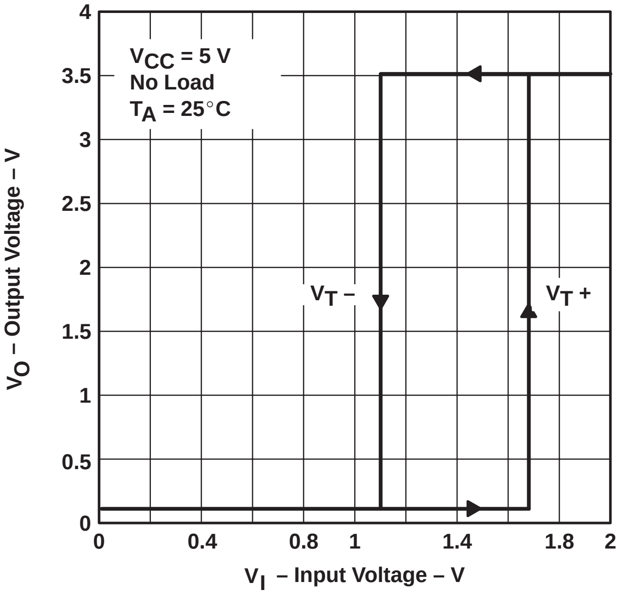


Figure 2

APPLICATION INFORMATION

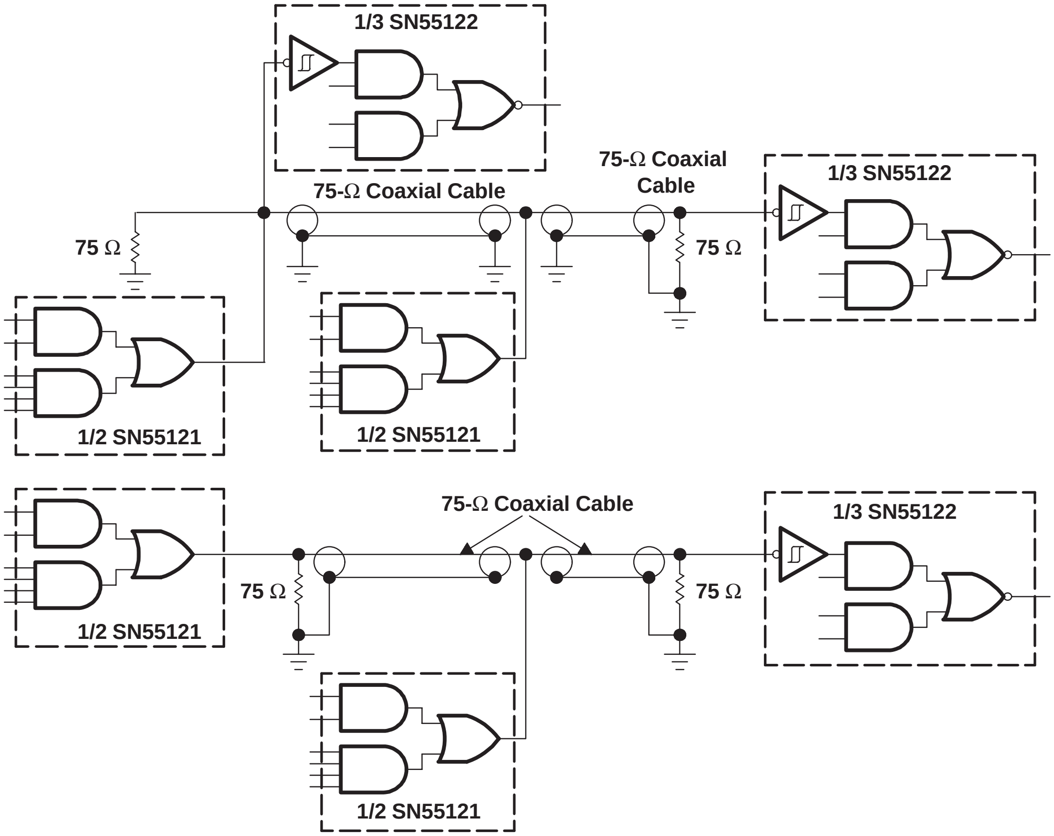
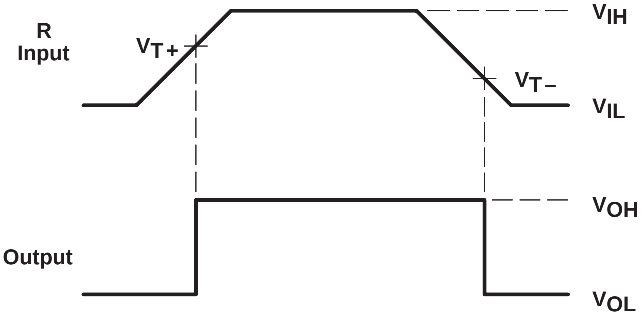


Figure 3. Single-Ended Party Line Circuits



NOTE: The high gain and built-in hysteresis of the SN55122 and SN75122 line receivers enable them to be used as Schmitt triggers in squaring pulses.

Figure 4. Pulse Squaring

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
SN55122J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SN75122D	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI
SN75122N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SNJ55122J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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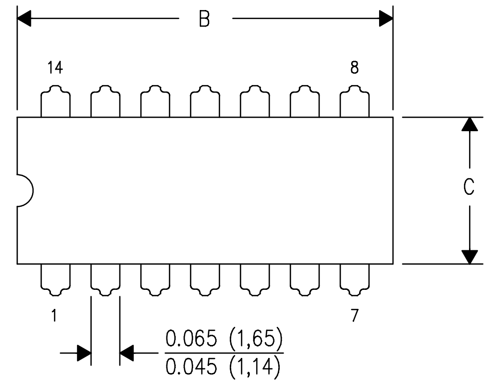
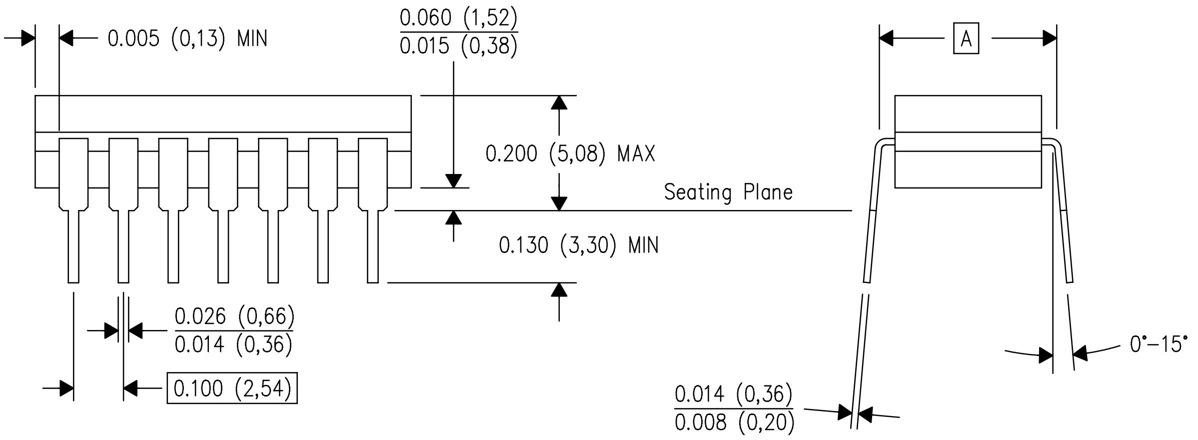
J (R–GDIP–T**) CERAMIC DUAL IN–LINE PACKAGE

14 LEADS SHOWN



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	——	——	——	——
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

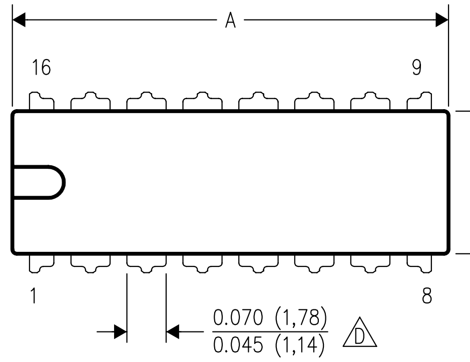


4040083/F 03/03

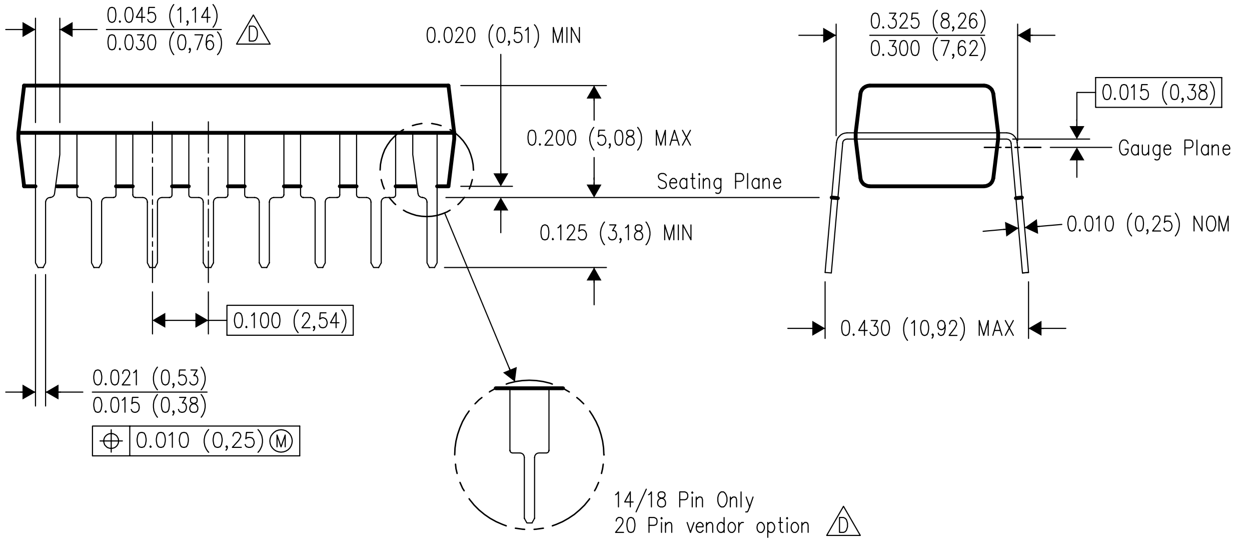
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



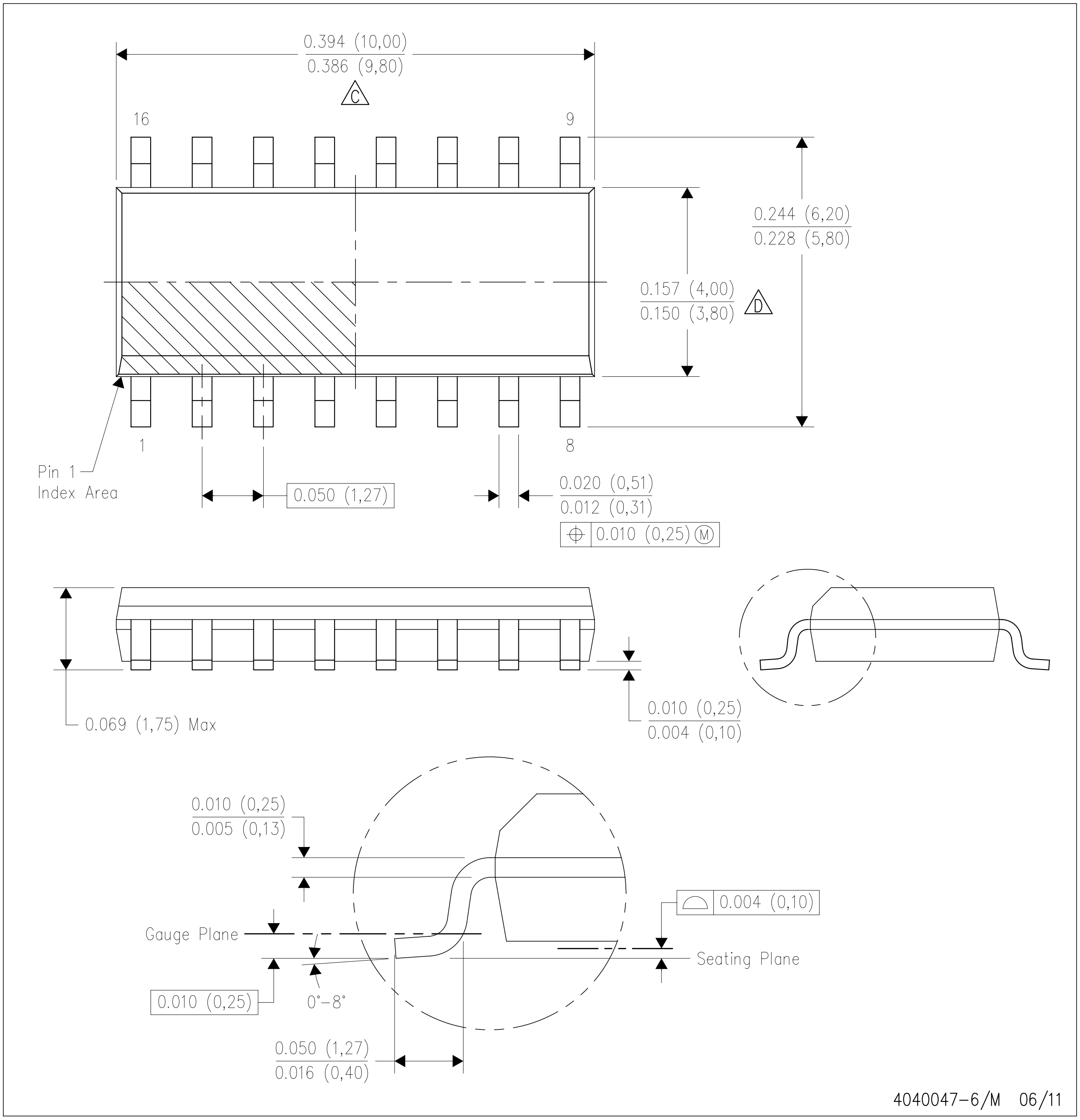
PINS ** / DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
C MS–001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS–012 variation AC.

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