SN54LVTT244, SN74LVTT244
3.3-V ABT OCTAL BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation**
- **Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Support Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Supports Live Insertion**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Packages, and Ceramic (J) DIPs**

SN54LVTT244 . . . J OR W PACKAGE
SN74LVTT244 . . . DB, DW, OR PW PACKAGE
(TOP VIEW)

Pin			Pin
1$\overline{OE}$	1	20	V_{CC}
1A1	2	19	2$\overline{OE}$
2Y4	3	18	1Y1
1A2	4	17	2A4
2Y3	5	16	1Y2
1A3	6	15	2A3
2Y2	7	14	1Y3
1A4	8	13	2A2
2Y1	9	12	1Y4
GND	10	11	2A1
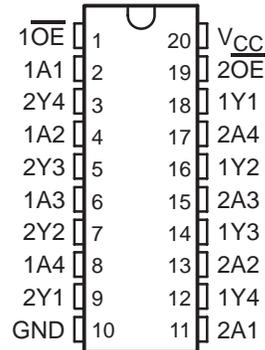
SN54LVTT244 . . . FK PACKAGE
(TOP VIEW)

Top pins: 2Y4 (3), 1A1 (2), 1$\overline{OE}$ (1), V_{CC} (20), 2$\overline{OE}$ (19)

Left	Pin		Pin	Right
1A2	4		18	1Y1
2Y3	5		17	2A4
1A3	6		16	1Y2
2Y2	7		15	2A3
1A4	8		14	1Y3

Bottom pins: 2Y1 (9), GND (10), 2A1 (11), 1Y4 (12), 2A2 (13)

description

These octal buffers and line drivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVTT244 are organized as two 4-bit line drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVTT244 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVTT244 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVTT244 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

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logic symbol†

logic diagram (positive logic)
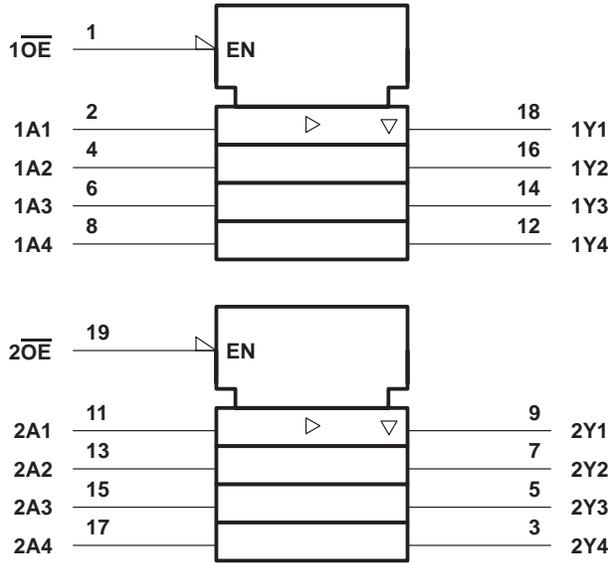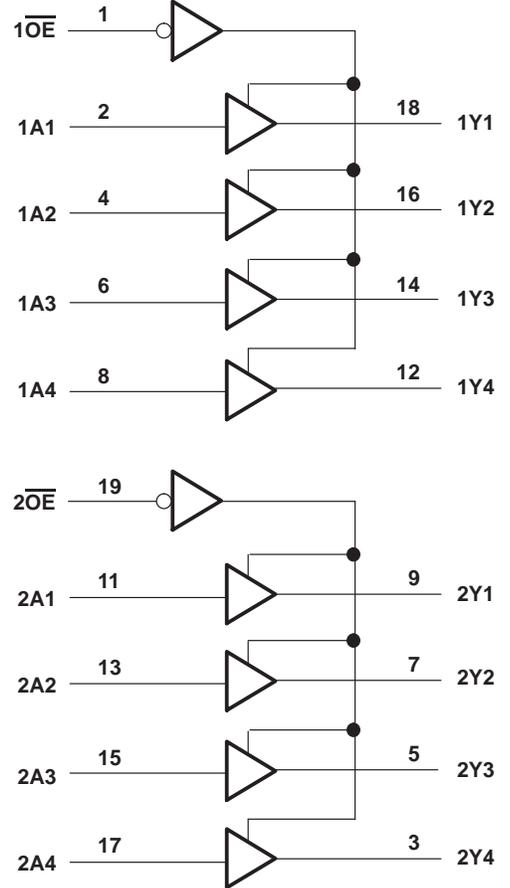
† This symbol is in accordance with ANSI/IEEE Std 91-1984
and IEC Publication 617-12.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) .... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVTT244 .... 96 mA
SN74LVTT244 .... 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTT244 .... 48 mA
SN74LVTT244 .... 64 mA
Input clamp current, I_{IK} (V_I < 0) .... −50 mA
Output clamp current, I_{OK} (V_O < 0) .... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DB package .... 0.6 W
DW package .... 1.6 W
PW package .... 0.7 W
Storage temperature range .... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and V_O > V_{CC}.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 4)

			SN54LVTT244		SN74LVTT244		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: Unused or floating control inputs must be held high or low.

![Texas Instruments logo]

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54LVTT244			SN74LVTT244			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = –18 mA				–1.2			–1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = –100 µA		V_{CC}–0.2			V_{CC}–0.2			V
	V_{CC} = 2.7 V,	I_{OH} = – 8 mA		2.4			2.4			
	V_{CC} = 3 V	I_{OH} = – 24 mA		2						
		I_{OH} = – 32 mA					2			
V_{OL}	V_{CC} = 2.7 V	I_{OL} = 100 µA				0.2			0.2	V
		I_{OL} = 24 mA				0.5			0.5	
	V_{CC} = 3 V	I_{OL} = 16 mA				0.4			0.4	
		I_{OL} = 32 mA				0.5			0.5	
		I_{OL} = 48 mA				0.55				
		I_{OL} = 64 mA							0.55	
I_I	V_{CC} = 0 or MAX‡,	V_I = 5.5 V				50			10	µA
	V_{CC} = 3.6 V,	V_I = V_{CC} or GND				±1			±1	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V							±100	µA
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				1			5	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V				–1			–5	µA
I_{CC}	V_{CC} = 3.6 V, I_O = 0, V_I = V_{CC} or GND		Outputs high	0.12	0.39		0.12	0.19		mA
			Outputs low	8.6	14		8.6	12		
			Outputs disabled	0.12	0.39		0.12	0.19		
ΔI_{CC}§	V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND					0.3			0.2	mA
C_i	V_I = 3 V or 0					4			4	pF
C_o	V_O = 3 V or 0					8			8	pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTT244				SN74LVTT244					UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN	MAX	
t_{PLH}	A	Y	0.5	4.7		5.2	1	2.5	4.1		5	ns
t_{PHL}			0.5	4.4		5.4	1	2.5	4.1		5.2	
t_{PZH}	$\overline{OE}$	Y	0.8	5.4		6.5	1	2.7	5.2		6.3	ns
t_{PZL}			0.8	5.4		7.6	1.1	3.1	5.2		6.7	
t_{PHZ}	$\overline{OE}$	Y	1.5	6.2		6.9	1.9	3.9	5.6		6.3	ns
t_{PLZ}			1.2	5.5		6	1.8	3.2	5.1		5.6	

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

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PARAMETER MEASUREMENT INFORMATION

From Output
Under Test

500 Ω   S1

6 V

○ Open

○ GND

C_L = 50 pF
(see Note A)

500 Ω
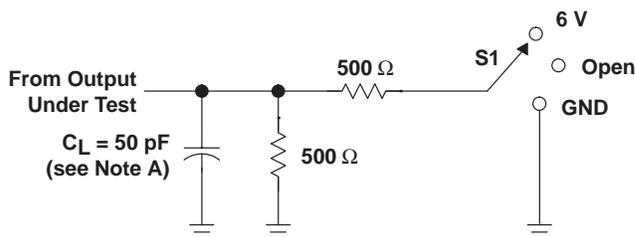
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT FOR OUTPUTS

Input   1.5 V t_W 1.5 V   2.7 V / 0 V
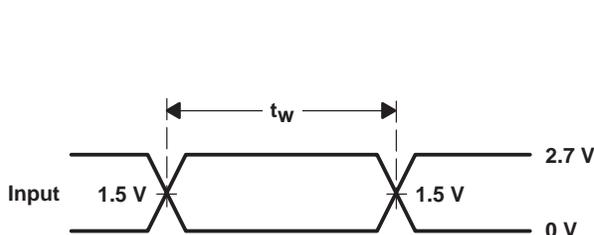
VOLTAGE WAVEFORMS
PULSE DURATION

Timing Input   1.5 V   2.7 V / 0 V

t_{su} t_h

Data Input   1.5 V   1.5 V   2.7 V / 0 V
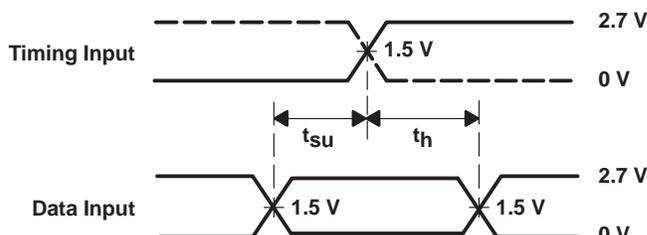
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

Input   1.5 V   1.5 V   2.7 V / 0 V

t_{PLH} t_{PHL}

Output   1.5 V   1.5 V V_{OH} / V_{OL}

t_{PHL} t_{PLH}

Output   1.5 V   1.5 V V_{OH} / V_{OL}
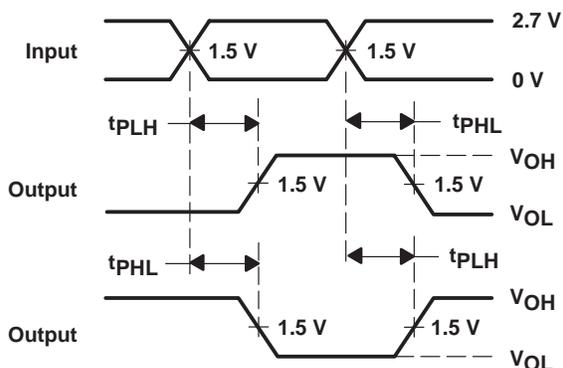
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

Output
Control   1.5 V   1.5 V   2.7 V / 0 V

t_{PZL} t_{PLZ}

Output
Waveform 1
S1 at 6 V
(see Note B)   1.5 V V_{OL} + 0.3 V   3 V / V_{OL}

t_{PZH} t_{PHZ}

Output
Waveform 2
S1 at GND
(see Note B)   1.5 V V_{OH} − 0.3 V V_{OH} / ≈ 0 V
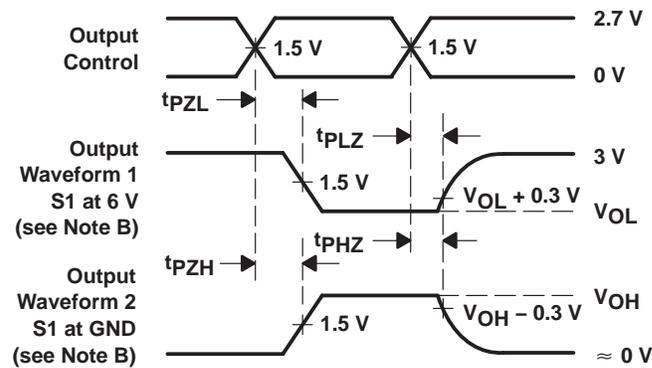
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PW (R−PDSO−G20)   PLASTIC SMALL OUTLINE

0,65

0,30
0,19

⊕ | 0,10 Ⓜ

20   11

4,50
4,30

6,60
6,20

Ⓓ

1   10

6,60
6,40

Ⓒ

0,15 NOM

Gage Plane

0°−8°

0,25

0,75
0,50

1,20 MAX

0,15
0,05

Seating Plane

◁ | 0,10
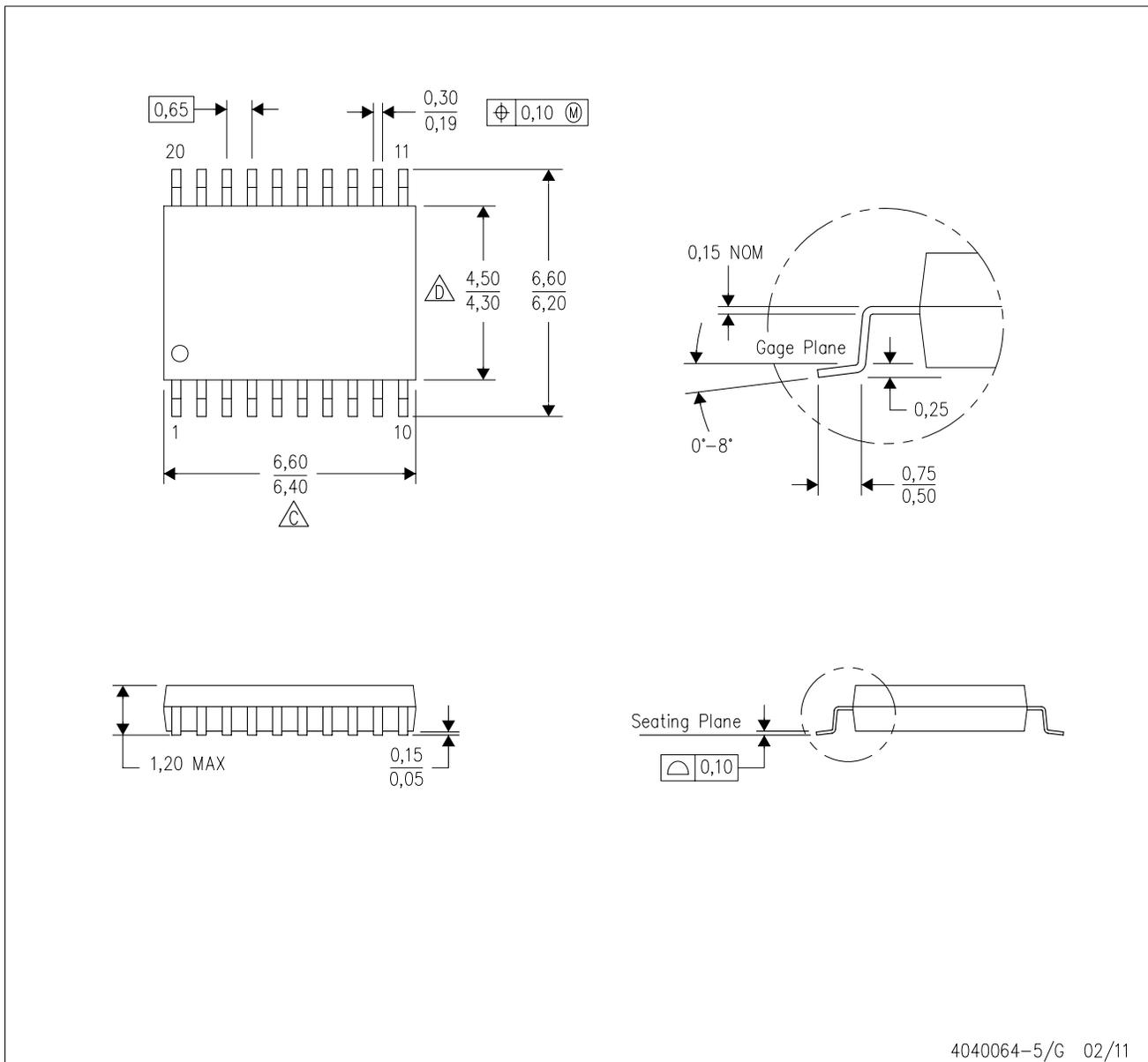
4040064−5/G 02/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
        B. This drawing is subject to change without notice.
        Ⓒ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
            not exceed 0,15 each side.
        Ⓓ Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
        E. Falls within JEDEC MO−153

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