

## FEATURES

- Synchronous Parallel Load
- Positive-Edge-Triggered Clocking
- J and  $\bar{K}$  Inputs to First Stage
- Complementary Outputs From Last Stage
- Package Options: Plastic and Ceramic DIPS and Ceramic Chip Carriers
- Dependable Texas Instruments Quality and Reliability

## DESCRIPTION/ORDERING INFORMATION

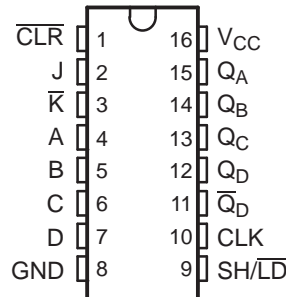
These 4-bit registers feature parallel inputs, parallel outputs, J-K serial inputs, shift/load control input, and a direct overriding clear. The registers have two modes of operation: parallel (broadside) load, and shift (in the direction  $Q_A$  and  $Q_D$ ).

Parallel loading is accomplished by applying the 4-bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

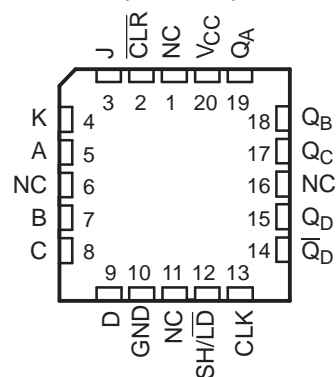
Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J- $\bar{K}$  inputs. These inputs permit the first stage to perform as a J- $\bar{K}$ , D, or T type flip-flop as shown in the function table.

The SN54HC195 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

SN54HC195 . . . J PACKAGE  
(TOP VIEW)

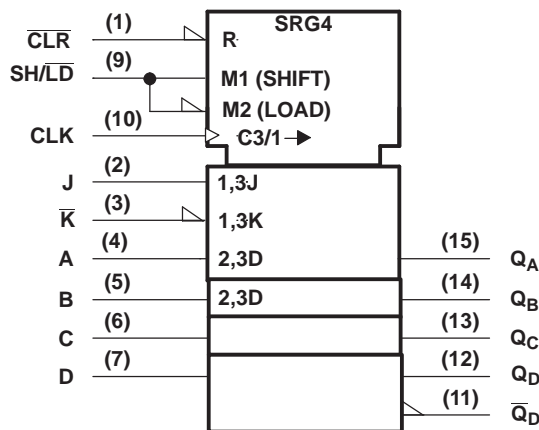


SN54HC195 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## LOGIC SYMBOL†



† This symbol is in accordance with ANSI/IEEE Std 91–1984 and IEC Publication 617–12.

Pin numbers shown are for J package.

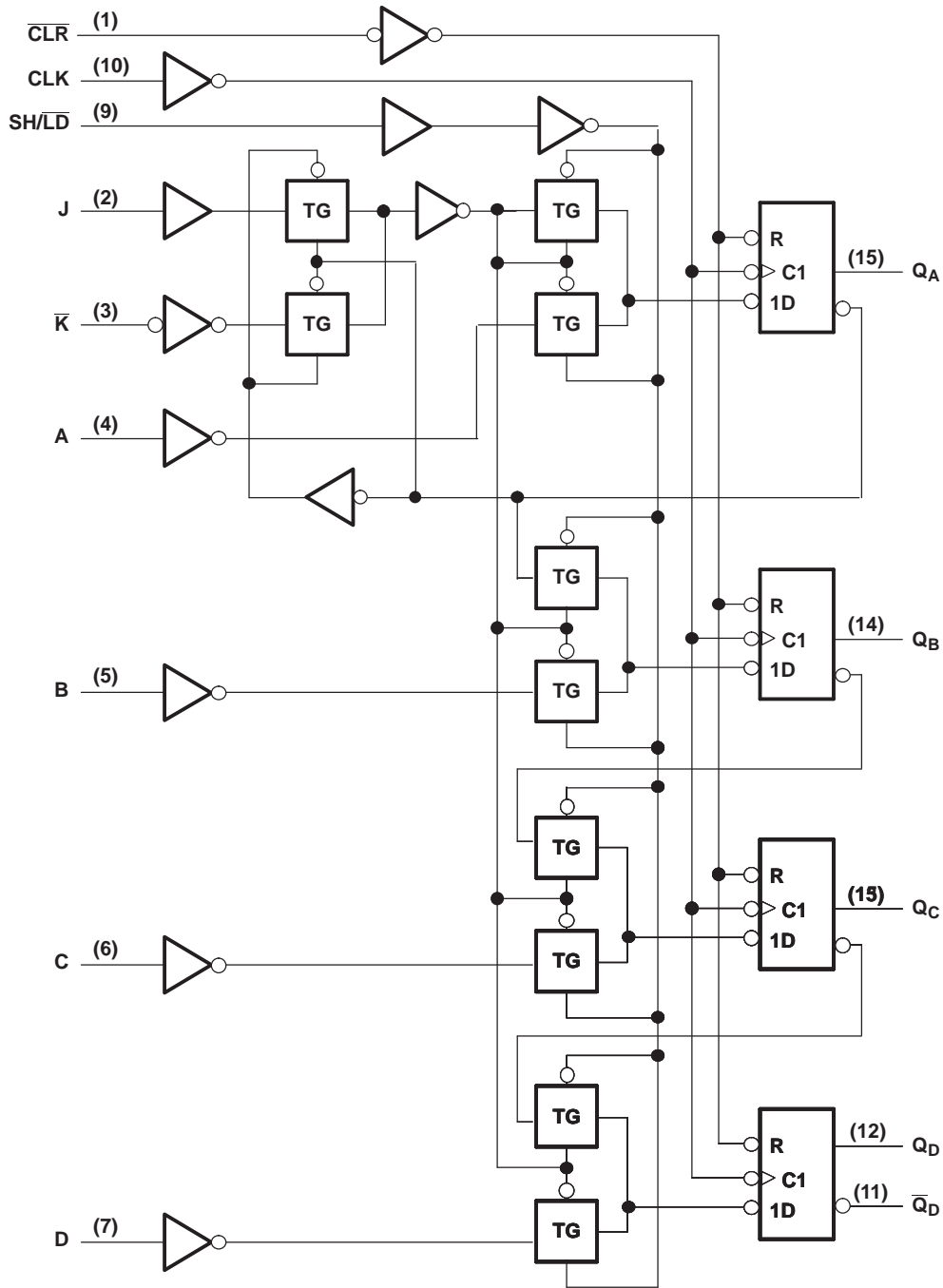


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# SN54HC195 4-BIT PARALLEL-ACCESS SHIFT REGISTERS

SCLS124A—DECEMBER 1992—REVISED NOVEMBER 2007

## LOGIC DIAGRAM (POSITIVE LOGIC)

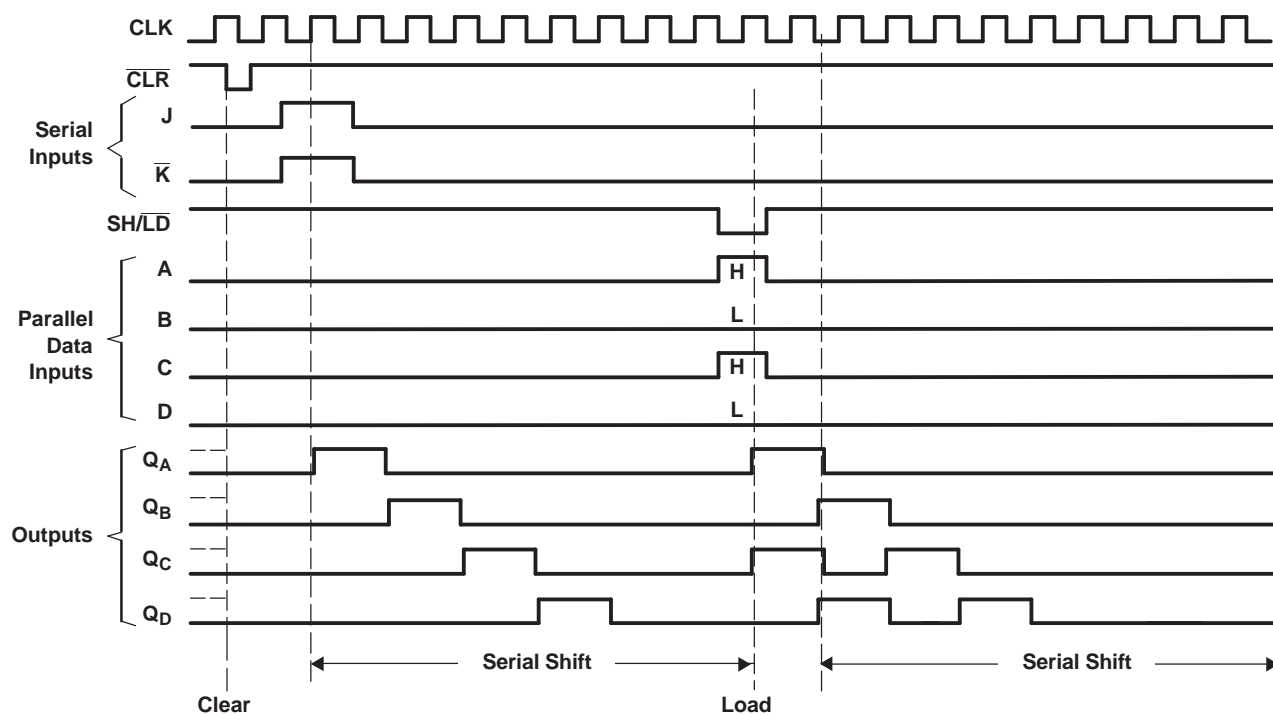


Pin numbers shown are for J package.

**FUNCTION TABLE**

CLR	SH/LD	CLK	INPUTS						OUTPUTS				
			SERIAL		PARALLEL				Q <sub>A</sub>	Q <sub>B</sub>	Q <sub>C</sub>	Q <sub>D</sub>	$\bar{Q}_D$
			J	$\bar{K}$	A	B	C	D					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	$\bar{d}$
H	H	L	X	X	X	X	X	X	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>C0</sub>	Q <sub>D0</sub>	$\bar{Q}_{D0}$
H	H	↑	L	H	X	X	X	X	Q <sub>A0</sub>	Q <sub>A0</sub>	Q <sub>Bn</sub>	Q <sub>Cn</sub>	$\bar{Q}_{Cn}$
H	H	↑	L	L	X	X	X	X	L	Q <sub>An</sub>	Q <sub>Bn</sub>	Q <sub>Cn</sub>	$\bar{Q}_{Cn}$
H	H	↑	H	H	X	X	X	X	H	Q <sub>An</sub>	Q <sub>Bn</sub>	Q <sub>Cn</sub>	$\bar{Q}_{Cn}$
H	H	↑	H	L	X	X	X	X	$\bar{Q}_{An}$	Q <sub>An</sub>	Q <sub>Bn</sub>	Q <sub>Cn</sub>	$\bar{Q}_{Cn}$

**TYPICAL CLEAR, SHIFT, AND LOAD SEQUENCES**



# SN54HC195 4-BIT PARALLEL-ACCESS SHIFT REGISTERS

SCLS124A–DECEMBER 1992–REVISED NOVEMBER 2007

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	-0.5	7	V
$I_{IK}$	Input clamp current $V_I < 0$ or $V_I > V_{CC}$		$\pm 20$	mA
$I_{OK}$	Output clamp current $V_O < 0$ or $V_O > V_{CC}$		$\pm 20$	mA
$I_O$	Continuous output current $V_O = 0$ to $V_{CC}$		25	mA
	Continuous current through $V_{CC}$ or GND pins		50	mA
	Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package		300	°C
	Lead temperature 1,6 mm (1/16 in) from case for 10 s: N package		260	°C
$T_{stg}$	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	2	5	6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2$ V	1.5		V
		$V_{CC} = 4.5$ V	3.15		
		$V_{CC} = 6$ V	4.2		
$V_{IL}$	Low-level input voltage	$V_{CC} = 2$ V	0	0.3	V
		$V_{CC} = 4.5$ V	0	0.9	
		$V_{CC} = 6$ V	0	1.2	
$V_I$	Input voltage	0		$V_{CC}$	V
$V_O$	Output voltage	0		$V_{CC}$	V
$t_t$	Input transition (rise and fall) times	$V_{CC} = 2$ V	0	1000	ns
		$V_{CC} = 4.5$ V	0	500	
		$V_{CC} = 6$ V	0	400	
$T_A$	Operating free-air temperature	-55		125	°C

## ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}$	$T_A = 25^\circ\text{C}$			SN54HC195		UNIT
			MIN	TYP	MAX	MIN	MAX	
$V_{OH}$	$V_I = V_{IH}$ or $V_{IL}$ , $I_{OH} = -20 \mu\text{A}$	2 V	1.9	1.998		1.9	V	
		4.5 V	4.4	4.499		4.4		
		6 V	5.9	5.999		5.9		
	$V_I = V_{IH}$ or $V_{IL}$ , $I_{OH} = -4 \text{ mA}$	4.5 V	3.98	4.30		3.7		
		6 V	5.48	5.80		5.2		
$V_{OL}$	$V_I = V_{IH}$ or $V_{IL}$ , $I_{OL} = 20 \mu\text{A}$	2 V		0.002	0.1	0.1	V	
		4.5 V		0.001	0.1	0.1		
		6 V		0.001	0.1	0.1		
	$V_I = V_{IH}$ or $V_{IL}$ , $I_{OL} = 4 \text{ mA}$	4.5 V		0.17	0.26	0.4		
		6 V		0.15	0.26	0.4		
$I_I$	$V_I = V_{CC}$ or 0	6 V		$\pm 0.1$	$\pm 100$	$\pm 1000$	nA	
$I_{CC}$	$V_I = V_{CC}$ or 0, $I_O = 0$	6 V			8	160	$\mu\text{A}$	
$C_I$	$V_I = V_{CC}$ or GND	2 V to 6 V		3	10	10	pF	

## TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted)

		$V_{CC}$	$T_A = 25^\circ\text{C}$		SN54HC195		UNIT
			MIN	MAX	MIN	MAX	
$f_{\text{clock}}$	Clock frequency	2 V	0	6	0	4.2	MHz
		4.5 V	0	31	0	21	
		6 V	0	36	0	25	
$t_w$	Pulse duration	CLK high or low		2 V	80	120	ns
				4.5 V	16	24	
				6 V	14	20	
	$\overline{\text{CLR}}$ low		2 V	80	120		
			4.5 V	16	24		
			6 V	14	20		
$t_{\text{su}}$	Setup time, before CLK $\uparrow$	SH/ $\overline{\text{LD}}$ , or serial and parallel data, or CLR inactive		2 V	100	150	ns
				4.5 V	20	30	
				6 V	17	26	
$t_h$	Hold time, after CLK $\uparrow$	SH/ $\overline{\text{LD}}$ , or serial and parallel data, or CLR inactive		2 V	0	0	ns
				4.5 V	0	0	
				6 V	0	0	

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted),  $C_L = 50 \text{ pF}^{(1)}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			SN54HC195		UNIT
				MIN	TYP	MAX	MIN	MAX	
$f_{\text{max}}$			2 V	6	12		4.2	MHz	
			4.5 V	31	50		21		
			6 V	36	60		25		
$t_{\text{pd}}$	CLK	$Q_A$ thru $Q_D$ or $\overline{Q}_D$	2 V		67	145		220	ns
			4.5 V		17	29		44	
			6 V		14	25		37	
$t_{\text{pd}}$	$\overline{\text{CLR}}$	$Q_A$ thru $Q_D$ or $\overline{Q}_D$	2 V		67	150		225	ns
			4.5 V		17	30		45	
			6 V		13	26		38	
$t_t$		Any	2 V		28	75		110	ns
			4.5 V		8	15		22	
			6 V		6	13		19	
$C_{\text{pd}}$	Power dissipation capacitance			No load, $T_A = 25^\circ\text{C}$				65 pF typ	

(1) Load circuit and voltage waveforms are shown in previous pages.

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
5962-86827012A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
5962-8682701EA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Call TI	
SN54HC195J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
SNJ54HC195FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54HC195J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**OTHER QUALIFIED VERSIONS OF SN54HC195 :**

- Catalog: [SN74HC195](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.



FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

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