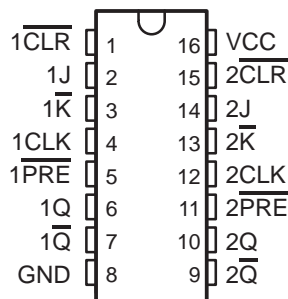- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

description

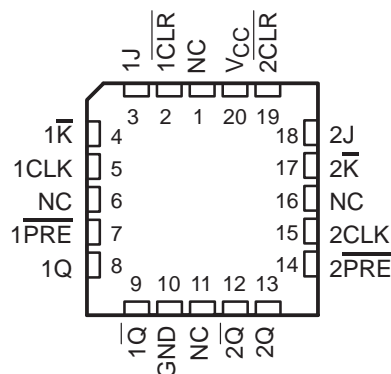These devices contain two independent J-$\overline{\text{K}}$ positive-edge-triggered flip-flops. A low level at the preset ($\overline{\text{PRE}}$) or clear ($\overline{\text{CLR}}$) inputs sets or resets the outputs regardless of the levels of the other inputs. When $\overline{\text{PRE}}$ and $\overline{\text{CLR}}$ are inactive (high), data at the J and $\overline{\text{K}}$ input meeting the setup-time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and $\overline{\text{K}}$ inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by grounding $\overline{\text{K}}$ and trying J high. They also can perform as D-type flip-flops if J and $\overline{\text{K}}$ are tied together.

The SN54F109 is characterized for operation over the full military temperature range of $-55°$C to $125°$C. The SN74F109 is characterized for operation from $0°$C to $70°$C.

SN54F109 . . . J PACKAGE
SN74F109 . . . D OR N PACKAGE
(TOP VIEW)

1$\overline{\text{CLR}}$	1	16	VCC
1J	2	15	2$\overline{\text{CLR}}$
1$\overline{\text{K}}$	3	14	2J
1CLK	4	13	2$\overline{\text{K}}$
1$\overline{\text{PRE}}$	5	12	2CLK
1Q	6	11	2$\overline{\text{PRE}}$
1$\overline{\text{Q}}$	7	10	2Q
GND	8	9	2$\overline{\text{Q}}$

SN54F109 . . . FK PACKAGE
(TOP VIEW)

Pins (top): 1J, 1$\overline{\text{CLR}}$, NC, V$_{\text{CC}}$, 2$\overline{\text{CLR}}$ (pins 3 2 1 20 19)

1$\overline{\text{K}}$	4	18	2J
1CLK	5	17	2$\overline{\text{K}}$
NC	6	16	NC
1$\overline{\text{PRE}}$	7	15	2CLK
1Q	8	14	2$\overline{\text{PRE}}$

Pins (bottom, 9 10 11 12 13): 1$\overline{\text{Q}}$, GND, NC, 2Q, 2$\overline{\text{Q}}$

NC – No internal connection

FUNCTION TABLE

INPUTS					OUTPUTS	
$\overline{\text{PRE}}$	$\overline{\text{CLR}}$	CLK	J	$\overline{\text{K}}$	Q	$\overline{\text{Q}}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H†	H†
H	H	↑	L	L	L	H
H	H	↑	H	L	Toggle	
H	H	↑	L	H	Q_0	$\overline{Q}_0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q_0	$\overline{Q}_0$

† The output levels are not guaranteed to meet the minimum levels for V_{OH}. Furthermore, this configuration is nonstable; that is, it will not persist when $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ returns to its inactive (high) level.

TEXAS INSTRUMENTS

SN54F109, SN74F109
DUAL J-$\overline{\text{K}}$ POSITIVE-EDGE-TRIGGERED FLIP-FLOPS
WITH CLEAR AND PRESET

SDFS047A – MARCH 1987 – REVISED OCTOBER 1993

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} .... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) .... −1.2 V to 7 V
Input current range .... −30 mA to 5 mA
Voltage range applied to any output in the high state .... −0.5 V to V_{CC}
Current into any output in the low state .... 40 mA
Operating free-air temperature range: SN54F109 .... −55°C to 125°C
                                                                 SN74F109 .... 0°C to 70°C
Storage temperature range .... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and
   functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
   implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F109			SN74F109			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54F109			SN74F109			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = − 18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = − 1 mA	2.5	3.4		2.5	3.4		V
		V_{CC} = 4.75 V,	I_{OH} = − 1 mA				2.7			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.3	0.5		0.3	0.5	V
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
I_{IL}	J, $\overline{\text{K}}$, CLK	V_{CC} = 5.5 V,	V_I = 0.5 V			− 0.6			− 0.6	mA
	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$					− 1.8			− 1.8	
I_{OS}‡		V_{CC} = 5.5 V,	V_O = 0	−60		−150	−60		−150	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 2		11.7	17		11.7	17	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 2: I_{CC} is measured with J, $\overline{\text{K}}$, CLK, and $\overline{\text{PRE}}$ grounded then with J, $\overline{\text{K}}$, CLK, and $\overline{\text{CLR}}$ grounded.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V_{CC} = 5 V, T_A = 25°C		SN54F109		SN74F109		UNIT
			'F74						
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	100	0	70	0	90	MHz
t_w	Pulse duration	CLK high, $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low	4		4		4		ns
		CLK low	5		5		5		
t_{su}	Setup time, data before CLK↑	High	3		3		3		ns
		Low	3		3		3		
	Setup time, inactive-state before CLK↑§	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ to CLK	2		2		2		
t_h	Hold time, data after CLK↑	High	1		1		1		ns
		Low	1		1		1		

§ Inactive-state setup time is also referred to as recovery time.

switching characteristics (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX¶				UNIT
			'F109			SN54F109		SN74F109		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			100	150		70		90		MHz
t_{PLH}	CLK	Q or $\overline{\text{Q}}$	3	4.9	7	3	9	3	8	ns
t_{PHL}			3.6	5.8	8	3.6	10.5	3.6	9.2	
t_{PLH}	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\overline{\text{Q}}$	2.4	4.8	7	2.4	9	2.4	8	ns
t_{PHL}			2.7	6.6	9	2.7	11.5	2.7	10.5	

¶ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
NOTE 3: Load circuits and waveforms are shown in Section 1.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/ Ball Finish	MSL Peak Temp [3]	Samples (Requires Login)
5962-9758001Q2A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
5962-9758001QEA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Call TI	
5962-9758001QFA	ACTIVE	CFP	W	16	1	TBD	Call TI	Call TI	
JM38510/34102B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
JM38510/34102BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
JM38510/34102BFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	
M38510/34102B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
M38510/34102BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
M38510/34102BFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	
SN74F109D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74F109DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74F109DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74F109DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74F109DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74F109DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74F109N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74F109NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SNJ54F109FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54F109J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
SNJ54F109W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	

[1] The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN54F109, SN74F109 :

- Catalog: SN74F109

- Military: SN54F109

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

Reel Diameter

Reel Width (W1)

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

Sprocket Holes

Q1 | Q2
Q3 | Q4

User Direction of Feed

Pocket Quadrants

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74F109DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74F109DR	SOIC	D	16	2500	333.2	345.9	28.6

J (R—GDIP—T**)

CERAMIC DUAL IN—LINE PACKAGE

14 LEADS SHOWN

DIM / PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	——	——	——	——
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

C

1   7

0.065 (1,65)
0.045 (1,14)

0.005 (0,13) MIN

0.060 (1,52)
0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.026 (0,66)
0.014 (0,36)

0.100 (2,54)

A

0°—15°

0.014 (0,36)
0.008 (0,20)

4040083/F 03/03

NOTES: A.   All linear dimensions are in inches (millimeters).
B.   This drawing is subject to change without notice.
C.   This package is hermetically sealed with a ceramic lid using glass frit.
D.   Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E.   Falls within MIL STD 1835 GDIP1—T14, GDIP1—T16, GDIP1—T18 and GDIP1—T20.

W (R–GDFP–F16) CERAMIC DUAL FLATPACK

0.045 (1,14)
0.026 (0,66)

0.080 (2,03)
0.055 (1,40)

0.285 (7,24)
0.245 (6,22)

Base and Seating Plane

0.006 (0,15)
0.004 (0,10)

0.305 (7,75) MAX

0.019 (0,48)
0.015 (0,38)

0.050 (1,27)

0.430 (10,92)
0.370 (9,40)

0.005 (0,13) MIN
4 Places

1   16

8   9

0.360 (9,14)
0.250 (6,35)

0.360 (9,14)
0.250 (6,35)

4040180–3/D 07/03

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F16 and JEDEC MO–092AC

FK (S−CQCC−N**)   LEADLESS CERAMIC CHIP CARRIER
28 TERMINAL SHOWN

NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

4040140/D 01/11

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   This package can be hermetically sealed with a metal lid.
         D.   Falls within JEDEC MS−004

N (R–PDIP–T**)

16 PINS SHOWN

PLASTIC DUAL–IN–LINE PACKAGE

PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION	AA	BB	AC	AD

A

16   9

$\dfrac{0.260\ (6,60)}{0.240\ (6,10)}$

1   8

$\dfrac{0.070\ (1,78)}{0.045\ (1,14)}$ ⟋D⟍

$\dfrac{0.045\ (1,14)}{0.030\ (0,76)}$ ⟋D⟍

0.020 (0,51) MIN

$\dfrac{0.325\ (8,26)}{0.300\ (7,62)}$

0.015 (0,38)

Gauge Plane

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.010 (0,25) NOM

0.100 (2,54)

$\dfrac{0.021\ (0,53)}{0.015\ (0,38)}$

⊕ | 0.010 (0,25) Ⓜ

0.430 (10,92) MAX

14/18 Pin Only
20 Pin vendor option ⟋D⟍

4040049/E   12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
   B. This drawing is subject to change without notice.
   ⟋C⟍ Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
   ⟋D⟍ The 20 pin end lead shoulder width is a vendor option, either half or full width.

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D (R−PDSO−G16)   PLASTIC SMALL OUTLINE

0.394 (10,00)
0.386 (9,80)
△C

16   9

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80) △D

Pin 1
Index Area

1   8

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

⌒ 0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−6/M   06/11

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
      △C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
           not exceed 0.006 (0,15) each side.
      △D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
         E. Reference JEDEC MS−012 variation AC.

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IMPORTANT NOTICE