JUNE 1984—REVISED MAY 1986

- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**

- **P-N-P Inputs Reduce DC Loading**

- **Outputs Have 25-Ω Series Resistor, So No External Resistors are Required**

- **Package Options Include Plastic "Small Outline" Packages, Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

- **Dependable Texas Instruments Qualilty and Reliability**

description

These octal buffers and line drivers are designed to drive capacitive input characteristics of MOS devices and have the performance of the popular SN54ALS240A/SN74ALS240A series. At the same time, they offer a pinout with inputs and outputs on opposite sides of the package. This arrangement greatly enhances printed-circuit-board layout.

The three-state control gate is a 2-input AND with active-low inputs such that if either $\overline{G}1$ or $\overline{G}2$ is high, all eight outputs are in the high-impedance state.

The 'ALS2540 offers inverting data and the 'ALS2541 offers true data at the outputs.

The SN54ALS' is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS' is characterized for operation from 0°C to 70°C.

SN54ALS2540, SN54ALS2541 . . . J PACKAGE
SN74ALS2540, SN74ALS2541 . . . DW OR N PACKAGE
(TOP VIEW)

$\overline{G}1$	1	20	VCC
A1	2	19	$\overline{G}2$
A2	3	18	Y1
A3	4	17	Y2
A4	5	16	Y3
A5	6	15	Y4
A6	7	14	Y5
A7	8	13	Y6
A8	9	12	Y7
GND	10	11	Y8

SN54ALS2540, SN54ALS2541 . . . FK PACKAGE
(TOP VIEW)

Pins (top): A2, A1, $\overline{G}1$, VCC, $\overline{G}2$ — pins 3 2 1 20 19

A3	4	18	Y1
A4	5	17	Y2
A5	6	16	Y3
A6	7	15	Y4
A7	8	14	Y5

Pins (bottom): 9 10 11 12 13 — A8, GND, Y8, Y7, Y6

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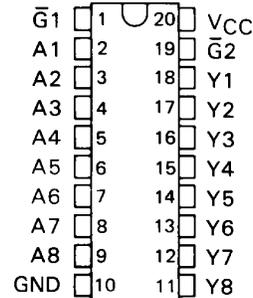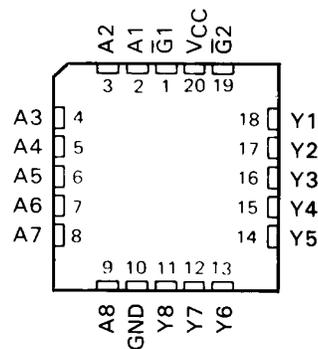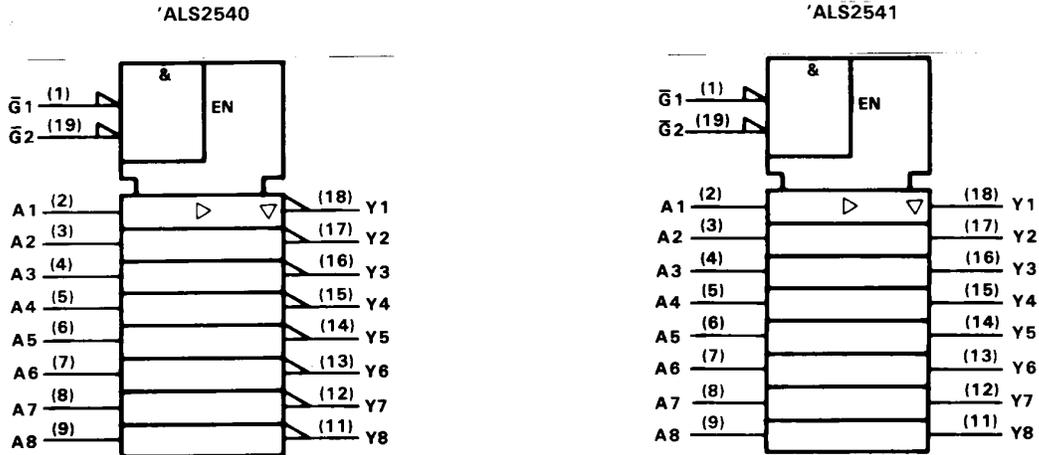**TEXAS INSTRUMENTS**

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SN54ALS2540, SN54ALS2541, SN74ALS2540, SN74ALS2541
OCTAL LINE DRIVERS/MOS DRIVERS WITH 3-STATE OUTPUTS

JUNE 1984 – REVISED MAY 1986

logic symbols†

'ALS2540

'ALS2541

†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)
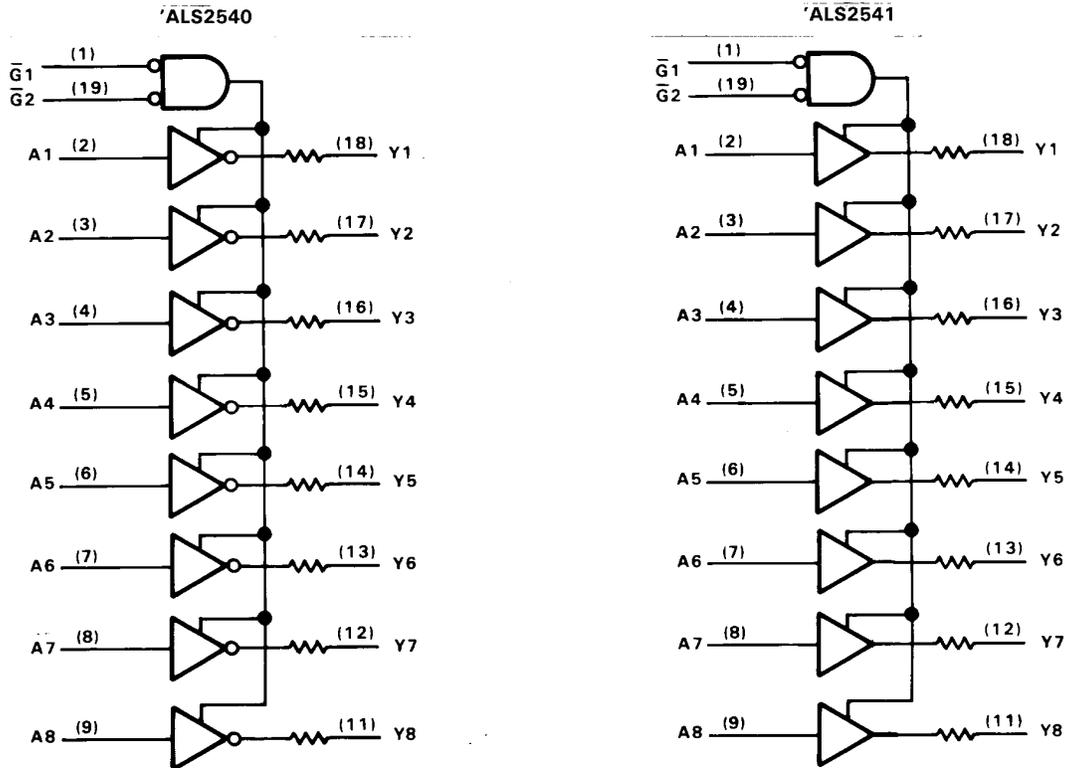
'ALS2540

'ALS2541

All output resistors are 25 Ω.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} .... 7 V
Input voltage .... 7 V
Voltage applied to a disabled 3-state output .... 5.5 V
Operating free-air temperature range: SN54ALS2540, SN54ALS2541 .... −55°C to 125°C
                                      SN74ALS2540, SN74ALS2541 .... 0°C to 70°C
Storage temperature range .... −65°C to 150°C

recommended operating conditions

		SN54ALS2540 SN54ALS2541			SN74ALS2540 SN74ALS2541			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			12			12	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS2540 SN54ALS2541			SN74ALS2540 SN74ALS2541			UNIT
				MIN	TYP[†]	MAX	MIN	TYP[†]	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 1 mA		0.15	0.5		0.15	0.5	V
		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.35	0.8		0.35	0.8	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	µA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	µA
I_{OH}		V_{CC} = 4.5 V,	V_O = 2 V	−15			−15			mA
I_{OL}		V_{CC} = 4.5 V,	V_O = 2 V	30			30			mA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O[‡]		V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
I_{CC}	'ALS2540	V_{CC} = 5.5 V	Outputs high		5	10		5	10	mA
			Outputs low		13	22		13	22	
			Outputs disabled		11	19		11	19	
	'ALS2541	V_{CC} = 5.5 V	Outputs high		6	14		6	14	mA
			Outputs low		15	25		15	25	
			Outputs disabled		13.5	22		13.5	22	

[†]All typical values are at V_{CC} = 5 V, T_A = 25°C.
[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

TEXAS
INSTRUMENTS

10-11

SN54ALS2540, SN54ALS2541, SN74ALS2540, SN74ALS2541
OCTAL LINE DRIVERS/MOS DRIVERS WITH 3-STATE OUTPUTS

JUNE 1984–REVISED MAY 1986

'ALS2540 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS2540	SN54ALS2540		SN74ALS2540		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	7.5	2	14	2	12	ns
t_{PHL}	A	Y	5.6	2	13	2	11	ns
t_{PZH}	$\overline{G}$	Y	9	5	18	5	15	ns
t_{PZL}	$\overline{G}$	Y	12.6	8	24	8	20	ns
t_{PHZ}	$\overline{G}$	Y	4	1	12	1	10	ns
t_{PLZ}	$\overline{G}$	Y	7	2	14	2	12	ns

'ALS2541 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS2541	SN54ALS2541		SN74ALS2541		
			TYP	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	8.7	2	17	2	15	ns
t_{PHL}	A	Y	7	2	14	2	12	ns
t_{PZH}	$\overline{G}$	Y	9	5	18	5	15	ns
t_{PZL}	$\overline{G}$	Y	12.6	8	24	8	20	ns
t_{PHZ}	$\overline{G}$	Y	4	1	12	1	10	ns
t_{PLZ}	$\overline{G}$	Y	7	2	14	2	12	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN74ALS2540N	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI	0 to 70		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and the leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

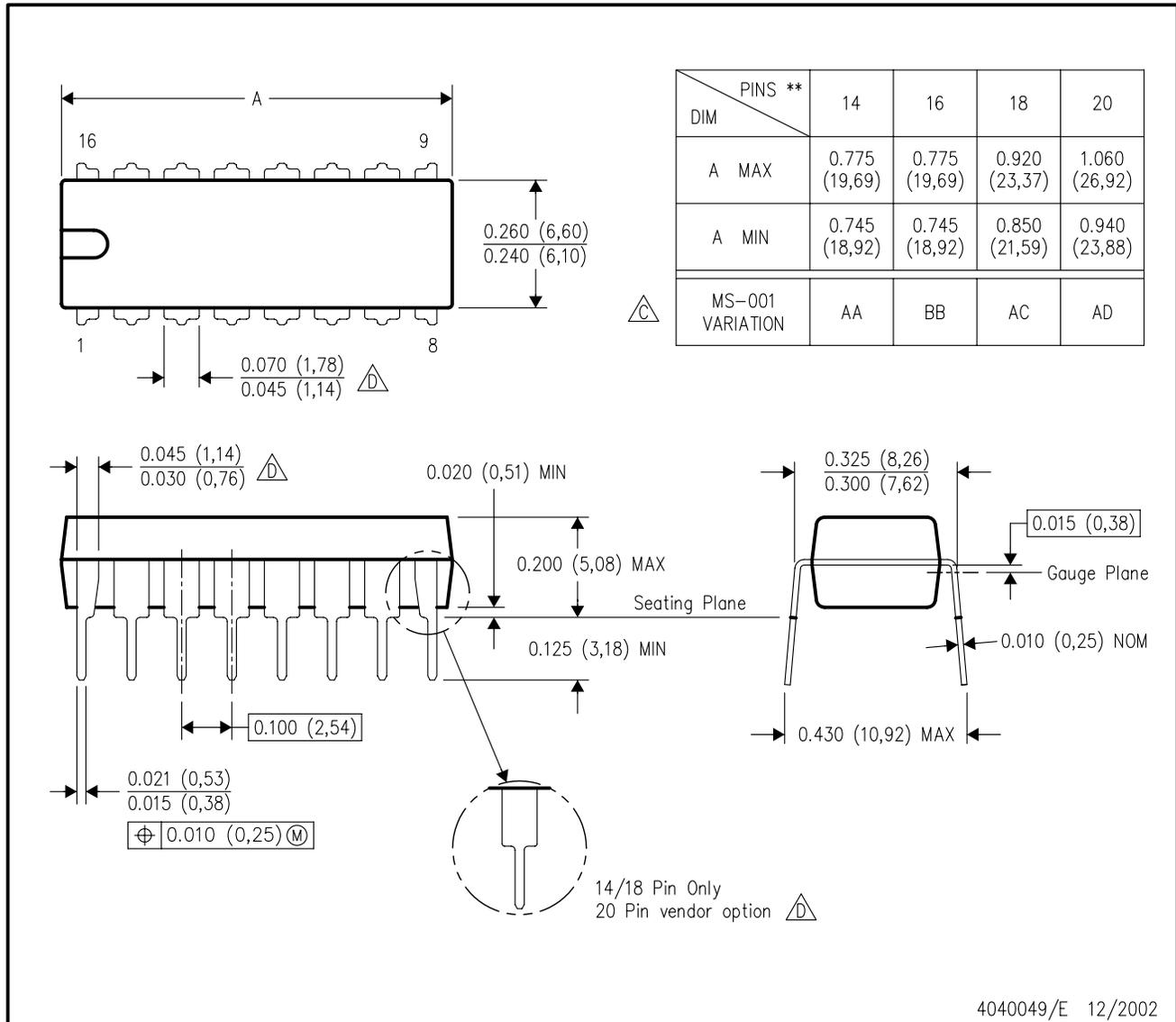**(4)** Only one of markings shown within the brackets will appear on the physical device.

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N (R−PDIP−T**)

16 PINS SHOWN

PLASTIC DUAL−IN−LINE PACKAGE

PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION	AA	BB	AC	AD

0.260 (6,60)
0.240 (6,10)

0.070 (1,78)
0.045 (1,14)

0.045 (1,14)
0.030 (0,76)

0.020 (0,51) MIN

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.010 (0,25) NOM

0.100 (2,54)

0.430 (10,92) MAX

0.021 (0,53)
0.015 (0,38)

$\oplus$ 0.010 (0,25) Ⓜ

14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
        D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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