

# SN54AHCT594, SN74AHCT594 8-BIT SHIFT REGISTERS WITH OUTPUT REGISTERS

SCLS417H – JUNE 1998 – REVISED SEPTEMBER 2003

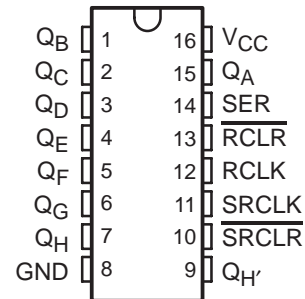
- Inputs Are TTL-Voltage Compatible
- 8-Bit Serial-In, Parallel-Out Shift Registers With Storage
- Independent Direct Overriding Clears on Shift and Storage Registers
- Independent Clocks for Both Shift and Storage Registers
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

## description/ordering information

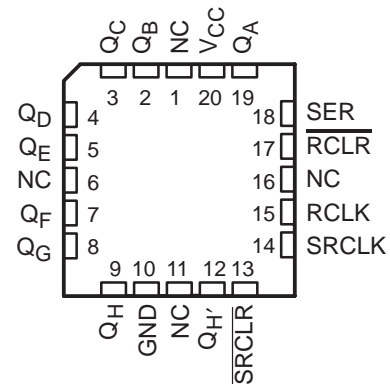
The 'AHCT594 devices contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Separate clocks and direct overriding clear ( $\overline{\text{SRCLR}}$ ,  $\overline{\text{RCLR}}$ ) inputs are provided on both the shift and storage registers. A serial ( $Q_H$ ) output is provided for cascading purposes.

Both the shift register (SRCLK) and storage register (RCLK) clocks are positive edge triggered. If both clocks are connected together, the shift register always is one count pulse ahead of the storage register.

SN54AHCT594 . . . J OR W PACKAGE  
SN74AHCT594 . . . D, DB, N, NS, OR PW PACKAGE  
(TOP VIEW)



SN54AHCT594 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube	SN74AHCT594N	SN74AHCT594N
	SOIC – D	Tube	SN74AHCT594D	AHCT594
		Tape and reel	SN74AHCT594DR	
	SOP – NS	Tape and reel	SN74AHCT594NSR	AHCT594
	SSOP – DB	Tape and reel	SN74AHCT594DBR	HB594
	TSSOP – PW	Tube	SN74AHCT594PW	HB594
Tape and reel		SN74AHCT594PWR		
–55°C to 125°C	CDIP – J	Tube	SNJ54AHCT594J	SNJ54AHCT594J
	CFP – W	Tube	SNJ54AHCT594W	SNJ54AHCT594W
	LCCC – FK	Tube	SNJ54AHCT594FK	SNJ54AHCT594FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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**TEXAS  
INSTRUMENTS**

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**SN54AHCT594, SN74AHCT594**  
**8-BIT SHIFT REGISTERS**  
**WITH OUTPUT REGISTERS**

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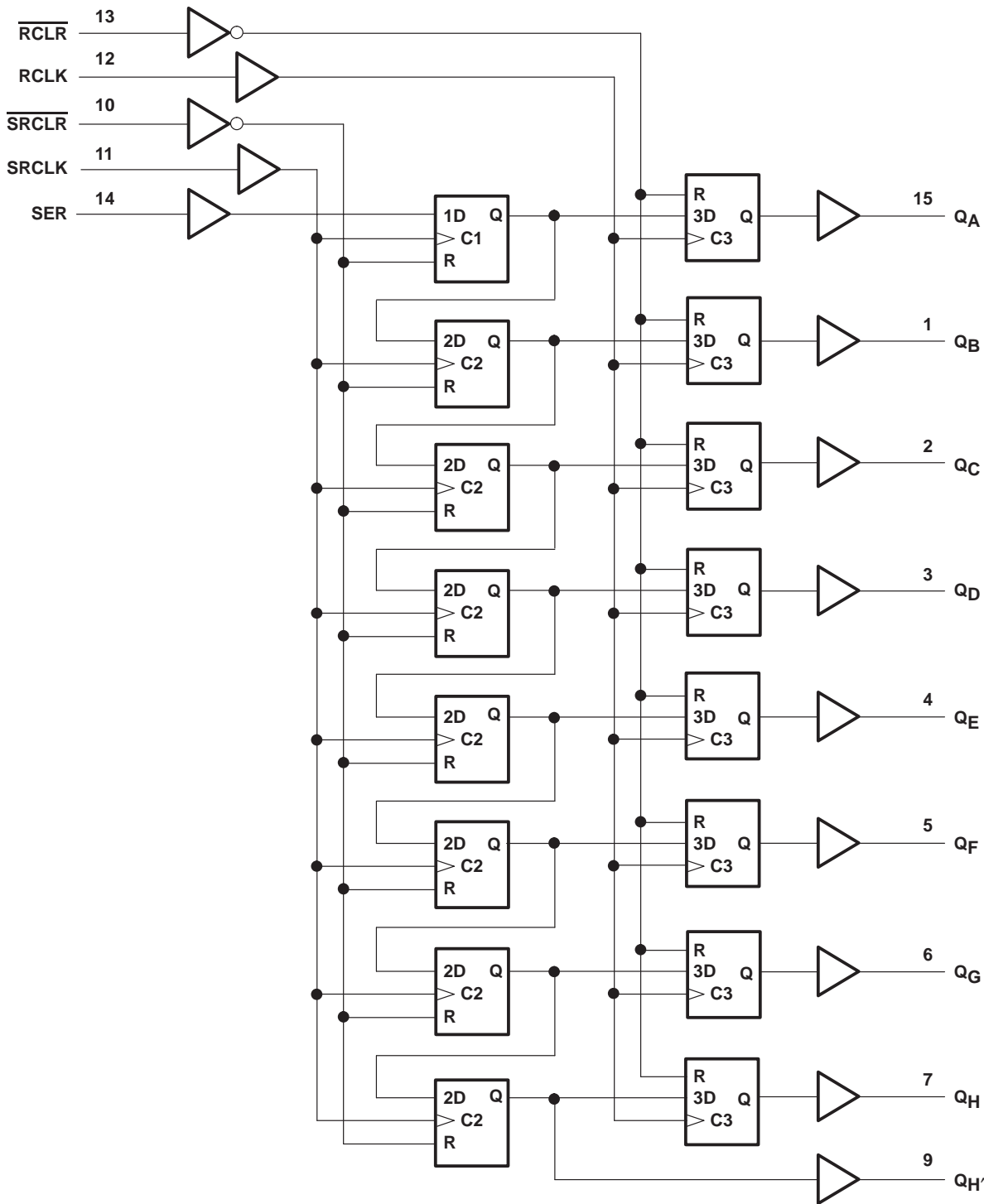
**FUNCTION TABLE**

INPUTS					FUNCTION
SER	SRCLK	SRCLR	RCLK	RCLR	
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of shift register goes low. Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First stage of shift register goes high. Other stages store the data of previous stage, respectively.
L	↓	H	X	X	Shift-register state is not changed.
X	X	X	X	L	Storage register is cleared.
X	X	X	↑	H	Shift-register data is stored in the storage register.
X	X	X	↓	H	Storage-register state is not changed.

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## logic diagram (positive logic)

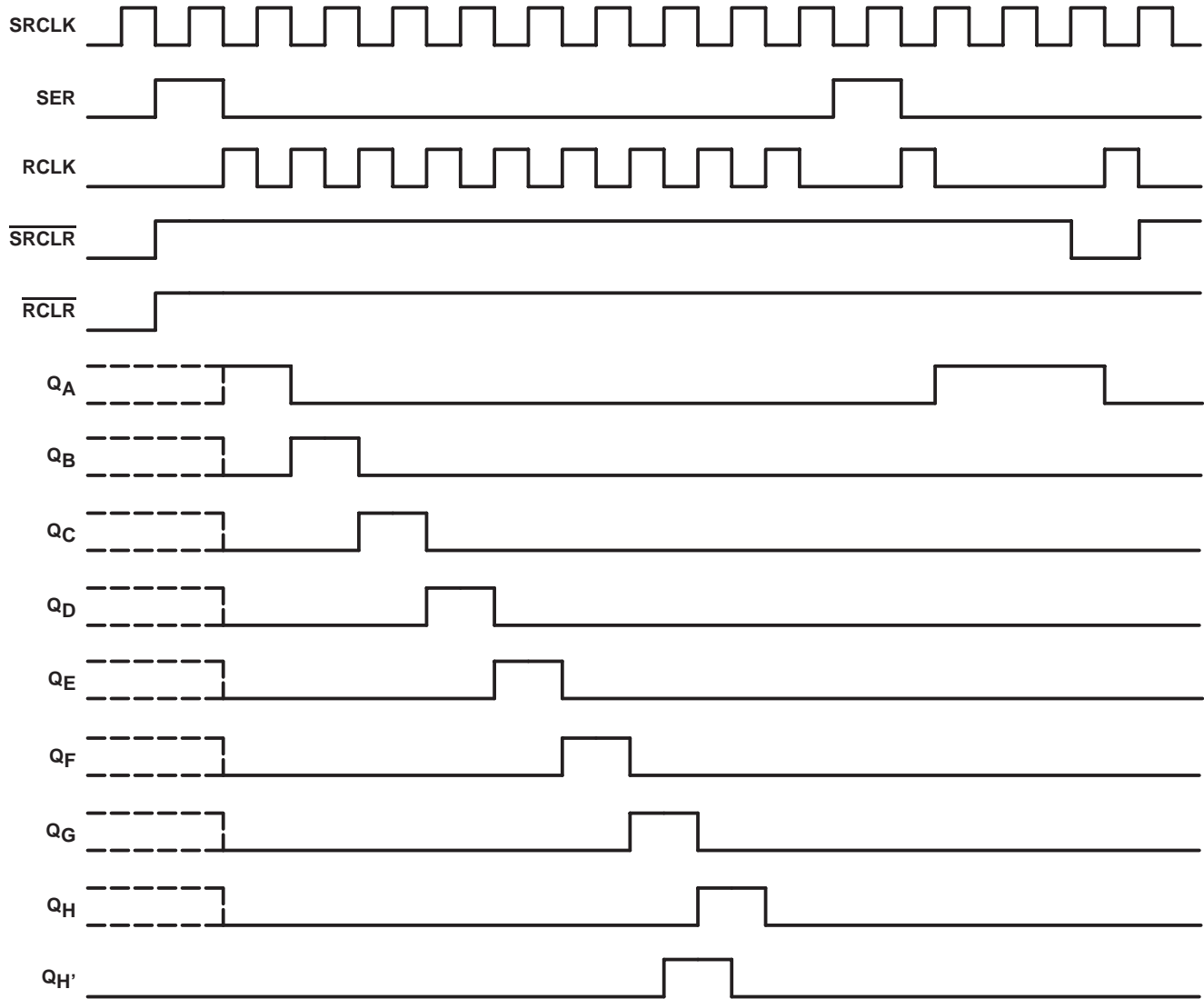


Pin numbers shown are for the D, DB, J, N, NS, PW, and W packages.

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## timing diagram



# SN54AHCT594, SN74AHCT594 8-BIT SHIFT REGISTERS WITH OUTPUT REGISTERS

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through $V_{CC}$ or GND	±75 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2):	
D package	73°C/W
DB package	82°C/W
N package	67°C/W
NS package	64°C/W
PW package	108°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 3)

	SN54AHCT594		SN74AHCT594		UNIT
	MIN	MAX	MIN	MAX	
$V_{CC}$ Supply voltage	4.5	5.5	4.5	5.5	V
$V_{IH}$ High-level input voltage	2		2		V
$V_{IL}$ Low-level input voltage		0.8		0.8	V
$V_I$ Input voltage	0	5.5	0	5.5	V
$V_O$ Output voltage	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$ High-level output current		–8		–8	mA
$I_{OL}$ Low-level output current		8		8	mA
$\Delta t/\Delta v$ Input transition rise or fall rate		20		20	ns/V
$T_A$ Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# SN54AHCT594, SN74AHCT594

## 8-BIT SHIFT REGISTERS

### WITH OUTPUT REGISTERS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54AHCT594		SN74AHCT594		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	4.5 V	4.4	4.5		4.4		4.4	V	
	I <sub>OH</sub> = -8 mA		3.94			3.8		3.8		
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	4.5 V			0.1			0.1	V	
	I <sub>OL</sub> = 8 mA				0.36		0.44	0.44		
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0 V to 5.5 V			±0.1			±1*	μA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			2		20	20	μA	
ΔI <sub>CC</sub> †	One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	5.5 V			2		2.2	2.2	mA	
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		2	10			10	pF	

\* On products compliant to MIL-PRF-38535, this parameter is not production tested at V<sub>CC</sub> = 0 V.

† This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V<sub>CC</sub>.

timing requirements over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

		T <sub>A</sub> = 25°C			SN54AHCT594		SN74AHCT594		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX		
t <sub>w</sub>	Pulse duration	RCLK or SRCLK high or low	5		5.5		5.5		ns
		RCLR or SRCLR low	5.2		5.5		5.5		
t <sub>su</sub>	Setup time	SER before SRCLK↑	3		3		3		ns
		SRCLK↑ before RCLK↑‡	5		5		5		
		SRCLR low before RCLK↑	5		5		5		
		SRCLR high (inactive) before SRCLK↑	2.9		3.3		3.3		
		RCLR high (inactive) before RCLK↑	3.4		3.8		3.8		
t <sub>h</sub>	Hold time	SER after SRCLK↑	2		2		2		ns

‡ This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



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switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHCT594		SN74AHCT594		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{\text{max}}$			$C_L = 15\text{ pF}$	135*	170*		115*		115		MHz
			$C_L = 50\text{ pF}$	120	140		95		95		
$t_{\text{PLH}}$	RCLK	$Q_A-Q_H$	$C_L = 15\text{ pF}$		3.3*	6.2*	1*	6.5*	1	6.5	ns
$t_{\text{PHL}}$					3.7*	6.5*	1*	6.9*	1	6.9	
$t_{\text{PLH}}$	SRCLK	$Q_H'$	$C_L = 15\text{ pF}$		3.7*	6.8*	1*	7.2*	1	7.2	ns
$t_{\text{PHL}}$					4.1*	7.2*	1*	7.6*	1	7.6	
$t_{\text{PHL}}$	$\overline{\text{RCLR}}$	$Q_A-Q_H$	$C_L = 15\text{ pF}$		4.5*	7.6*	1*	8.2*	1	8.2	ns
$t_{\text{PHL}}$	$\overline{\text{SRCLR}}$	$Q_H'$	$C_L = 15\text{ pF}$		4.1*	7.1*	1*	7.6*	1	7.6	ns
$t_{\text{PLH}}$	RCLK	$Q_A-Q_H$	$C_L = 50\text{ pF}$		4.9	7.8	1	8.3	1	8.3	ns
$t_{\text{PHL}}$					5.8	8.9	1	9.7	1	9.7	
$t_{\text{PLH}}$	SRCLK	$Q_H'$	$C_L = 50\text{ pF}$		5.5	8.6	1	9.1	1	9.1	ns
$t_{\text{PHL}}$					6	9.2	1	10.1	1	10.1	
$t_{\text{PHL}}$	$\overline{\text{RCLR}}$	$Q_A-Q_H$	$C_L = 50\text{ pF}$		6.6	10	1	10.7	1	10.7	ns
$t_{\text{PHL}}$	$\overline{\text{SRCLR}}$	$Q_H'$	$C_L = 50\text{ pF}$		6	9.2	1	10.1	1	10.1	ns

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics,  $V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 4)

PARAMETER		SN74AHCT594			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic $V_{OL}$		1		V
$V_{OL(V)}$	Quiet output, minimum dynamic $V_{OL}$		-0.6		V
$V_{OH(V)}$	Quiet output, minimum dynamic $V_{OH}$		3.8		V
$V_{IH(D)}$	High-level dynamic input voltage		2		V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

NOTE 4: Characteristics are for surface-mount packages only.

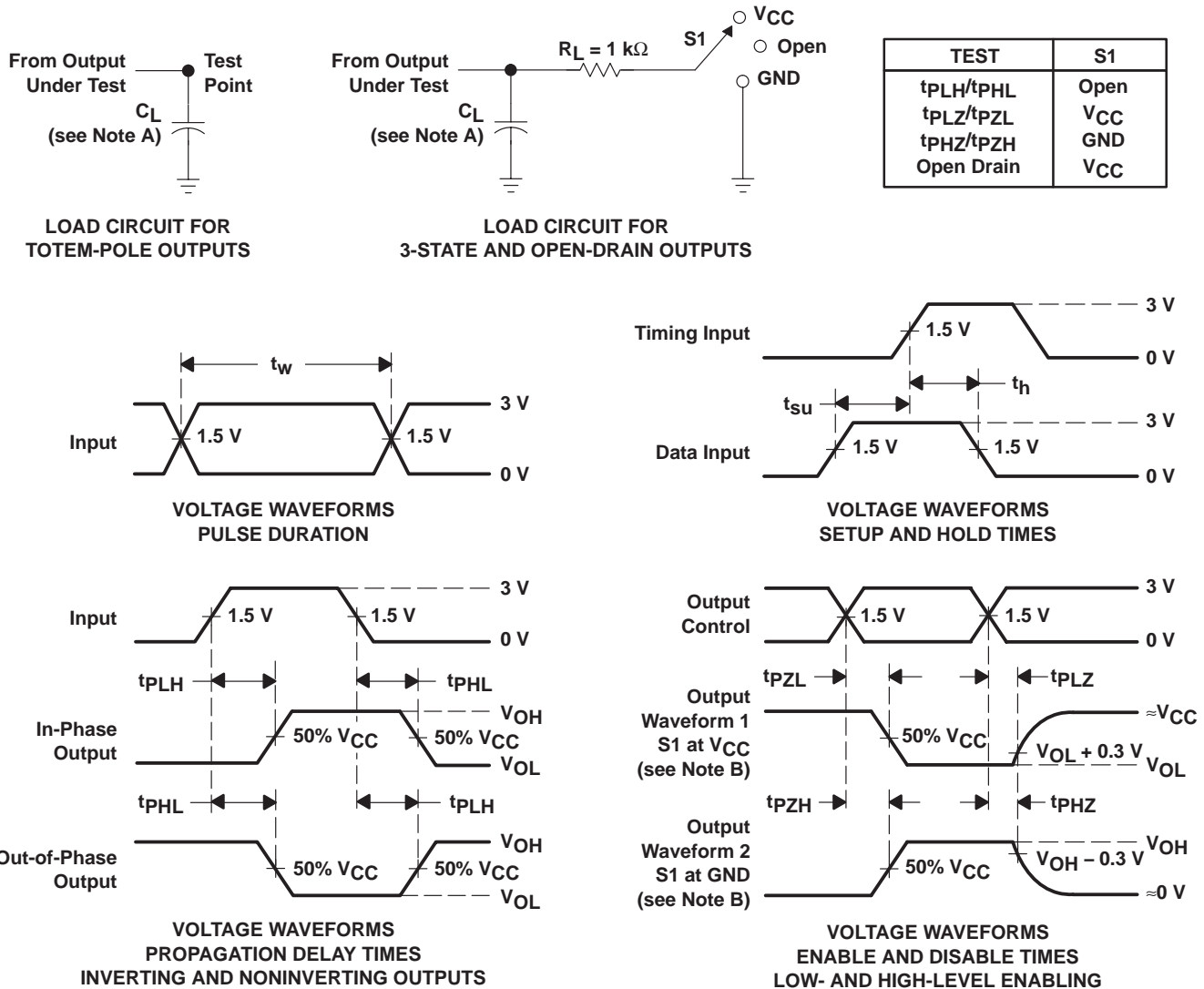
operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
$C_{pd}$	Power dissipation capacitance	No load, $f = 1\text{ MHz}$	112	pF

# SN54AHCT594, SN74AHCT594 8-BIT SHIFT REGISTERS WITH OUTPUT REGISTERS

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## PARAMETER MEASUREMENT INFORMATION



- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .
  - The outputs are measured one at a time with one input transition per measurement.
  - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74AHCT594D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT594DBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT594DBRE4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT594DBG4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT594DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT594DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT594DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT594DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT594DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT594N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74AHCT594NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74AHCT594NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT594NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT594NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT594PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT594PWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT594PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT594PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT594PWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT594PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHCT594DBR	SSOP	DB	16	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74AHCT594DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74AHCT594NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74AHCT594PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHCT594DBR	SSOP	DB	16	2000	367.0	367.0	38.0
SN74AHCT594DR	SOIC	D	16	2500	333.2	345.9	28.6
SN74AHCT594NSR	SO	NS	16	2000	367.0	367.0	38.0
SN74AHCT594PWR	TSSOP	PW	16	2000	367.0	367.0	35.0

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4211283-4/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



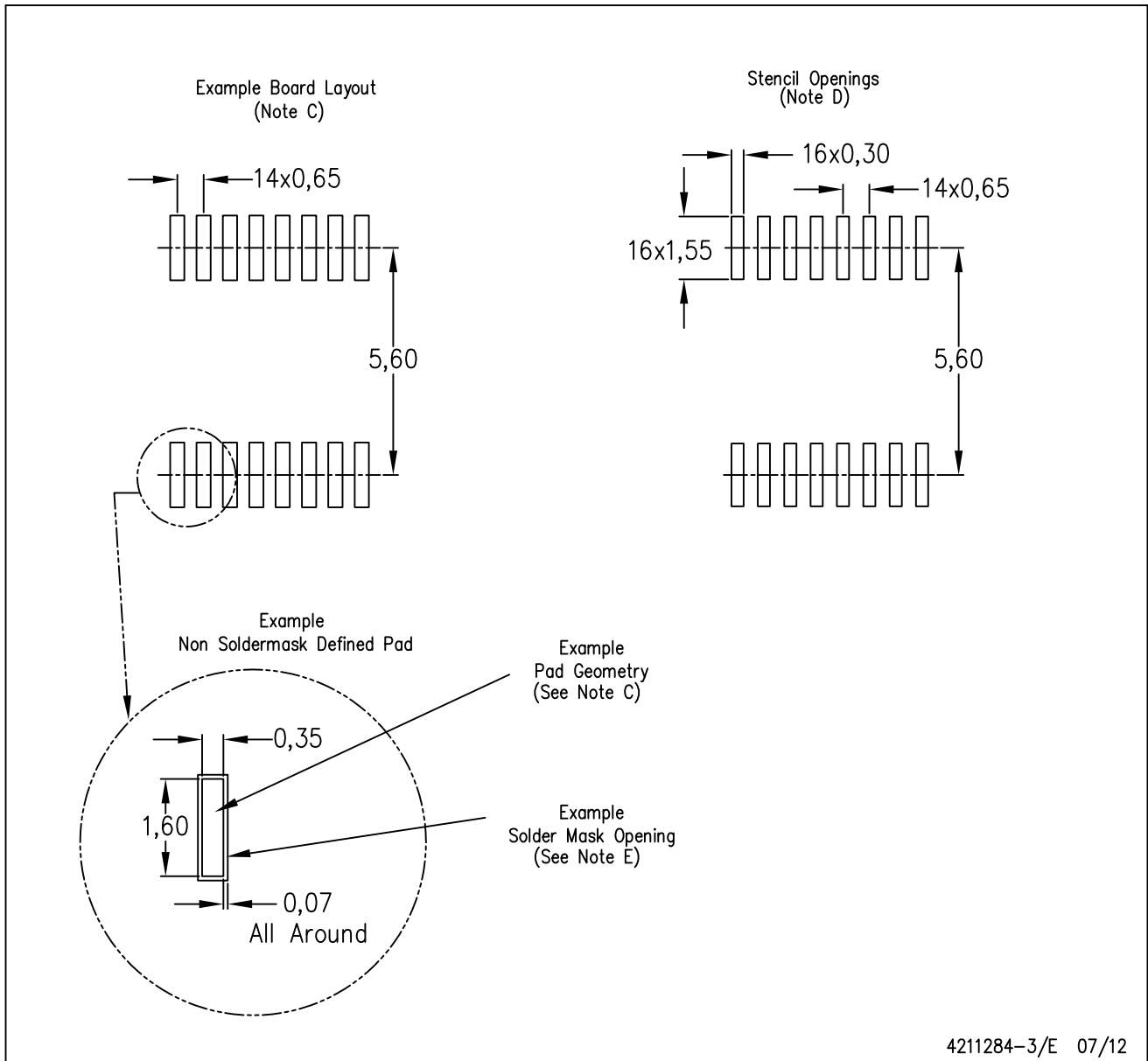
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- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153



PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

## IMPORTANT NOTICE

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