#### SN54ABT16827, SN74ABT16827 20-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS SCBS220C - JUNE 1992 - REVISED MAY 1997

SN54ABT16827 . . . WD PACKAGE Members of the Texas Instruments SN74ABT16827 . . . DL PACKAGE Widebus<sup>™</sup> Family (TOP VIEW) State-of-the-Art *EPIC-*II*B*<sup>™</sup> BiCMOS Design Significantly Reduces Power Dissipation 56 10E2 10E1 Latch-Up Performance Exceeds 500 mA Per 55 **1**A1 1Y1 2 **JEDEC Standard JESD-17** 1Y2 3 54 🛛 1A2 Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V GND 4 53 GND 1Y3 5 52 1A3 at V<sub>CC</sub> = 5 V, T<sub>A</sub> =  $25^{\circ}$ C 1Y4 6 51 1A4 **High-Impedance State During Power Up** V<sub>CC</sub> 7 50 VCC and Power Down 1Y5 8 49 1A5 • Distributed V<sub>CC</sub> and GND Pin Configuration 1Y6[]9 48 🛛 1A6 Minimizes High-Speed Switching Noise 1Y7 10 47 🛛 1A7 Flow-Through Architecture Optimizes PCB • GND 🚺 11 46 GND Layout 1Y8 12 45 **1**A8 • High-Drive Outputs (-32-mA IOH, 64-mA IOI) 1Y9 13 44 🛛 1A9 1Y10 14 43 🛛 1A10 Package Options Include Plastic 300-mil Shrink Small-Outline (DL) Package and 2Y1 11 15 42 2A1 2Y2 16 41 1 2A2 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings ( description The 'ABT16827 are noninverting 20-bit buffers composed of two 10-bit sections with separate output-enable signals. For either 10-bit buffer section, the two output-enable  $(1\overline{OE1} \text{ and } 1\overline{OE2})$ G

or 20E1 and 20E2) inputs must both be low for the corresponding Y outputs to be active. If either output-enable input is high, the outputs of that 10-bit buffer section are in the high-impedance state.

2124	10		
2Y3[	17	40	] 2A3
GND[	18	39	] GND
2Y4[	19	38	] 2A4
2Y5[	20	37	] 2A5
2Y6[	21	36	] 2A6
00-		35	] v <sub>cc</sub>
2Y7[	23	34	] 2A7
2Y8[	24	33	] 2A8
GND[	25	32	] GND
2Y9[	26	31	] 2A9
2Y10[	27	30	]2A10
20E1	28	29	] 2 <mark>0E</mark> 2

When V<sub>CC</sub> is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V,  $\overline{OE}$  should be tied to V<sub>CC</sub> through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT16827 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ABT16827 is characterized for operation from -40°C to 85°C.



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#### **FUNCTION TABLE** (each 10-bit section)

	OUTPUT								
OE1	OE2	Α	Y						
L	L	L	L						
L	L	Н	н						
н	Х	Х	Z						
Х	Н	Х	Z						

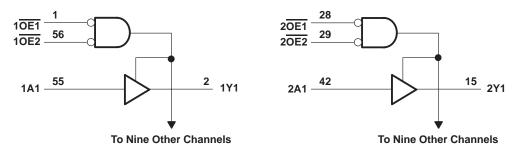
## logic symbol<sup>†</sup>

$1\overline{OE1}$ $1$ $8$ EN1 $1\overline{OE2}$ $28$ $8$ EN1 $2\overline{OE2}$ $29$ $8$ EN2 $1A1$ $55$ $1$ $1\nabla$ $2$ $1A3$ $51$ $6$ $1Y3$ $1A4$ $52$ $5$ $1Y3$ $1A4$ $51$ $6$ $1Y4$ $1A5$ $52$ $5$ $1Y3$ $1A4$ $49$ $8$ $1Y4$ $1A5$ $48$ $9$ $1Y4$ $1A5$ $48$ $9$ $1Y6$ $1A7$ $45$ $12$ $1Y7$ $1A8$ $44$ $13$ $1Y9$ $1A10$ $42$ $1$ $2\nabla$ $15$ $2A1$ $41$ $16$ $2Y2$ $2Y1$ $2A4$ $37$ $20$ $2Y4$ $2Y4$ $2A4$ $31$ $226$ $212$ $2Y6$ $2A4$ $31$ $226$ $2Y9$ $2X10$ $2A4$ $31$ $226$ $2Y9$						
$1\overline{OE2}$ $56$ $EN1$ $2\overline{OE1}$ $28$ $8$ $EN2$ $1A1$ $55$ $1$ $1 \nabla$ $2$ $1A1$ $55$ $1$ $1 \nabla$ $2$ $1A2$ $52$ $5$ $1Y2$ $1A3$ $51$ $6$ $1Y3$ $1A4$ $49$ $8$ $1Y2$ $1A3$ $51$ $6$ $1Y4$ $1A5$ $48$ $9$ $1Y6$ $1A7$ $45$ $12$ $1Y7$ $1A8$ $44$ $13$ $1Y9$ $1A10$ $42$ $1$ $2\nabla$ $15$ $1A10$ $42$ $1$ $2\nabla$ $15$ $2Y11$ $2A1$ $41$ $12$ $17$ $2Y2$ $2Y3$ $2A4$ $37$ $20$ $2Y5$ $2A6$ $36$ $211$ $2Y6$ $2A7$ $33$ $224$ $2Y6$ $277$ $2Y9$	10E1	1	&			
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	10F2	56	<b>_</b>	EN1		
2OE1       29       a       EN2         1A1 $55$ 1 $1 \bigtriangledown 7$ 2 $1Y1$ 1A2 $52$ 5 $1Y3$ $1Y2$ 1A3 $51$ 6 $1Y3$ 1A4 $49$ 8 $1Y3$ 1A4 $49$ 8 $1Y4$ 1A5 $48$ 9 $1Y6$ 1A6 $47$ 10 $1Y7$ 1A8 $44$ 13 $1Y9$ 1A7 $45$ 12 $1Y8$ 1A9 $43$ 14 $1Y10$ 2A1 $41$ $1 2 \bigtriangledown 15$ $2Y1$ 2A2 $40$ $177$ $2Y3$ 2A4 $37$ $20$ $2Y5$ 2A6 $36$ $211$ $2Y6$ 2A7 $33$ $226$ $2Y7$ 2A8 $31$ $226$ $2Y9$	IULZ	29	<u> </u>			
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	20E1		&	ENIO		
1A1 $55$ 1       1 $\bigtriangledown$ 2       1Y1         1A2 $54$ 1       1 $\bigtriangledown$ 3       1Y2         1A3 $52$ 5       1 Y3       1Y3         1A4 $49$ 6       1Y4         1A5 $48$ 9       1Y5         1A6 $47$ 10       1Y7         1A8 $44$ 13       1Y9         1A7 $45$ 12       1Y8         1A9 $43$ 14       1Y10         2A1 $42$ 1 $2 \bigtriangledown$ 15         2A3 $38$ 19       2Y1         2A4 $37$ 20       2Y4         2A5 $36$ 21       2Y6         2A6 $34$ 23       2Y7         2A8 $31$ 226       2Y9         30 $277$ 209       277	20E2	29	4	LINZ		
1A1       1		55		·	2	
$1A2$ $52$ $5$ $1Y2$ $1A3$ $51$ $6$ $1Y3$ $1A4$ $49$ $8$ $1Y4$ $1A5$ $48$ $9$ $1Y5$ $1A6$ $47$ $10$ $1Y7$ $1A6$ $47$ $10$ $1Y7$ $1A8$ $44$ $13$ $1Y9$ $1A7$ $45$ $12$ $1Y8$ $1A9$ $43$ $14$ $1Y10$ $2A1$ $42$ $1$ $2 \bigtriangledown$ $15$ $2A1$ $41$ $12 \lor$ $172$ $2Y12$ $2A3$ $38$ $199$ $2Y4$ $2A4$ $37$ $200$ $2Y5$ $2A6$ $34$ $233$ $2Y7$ $2A8$ $31$ $226$ $2Y8$ $2A9$ $30$ $277$ $2Y9$	1A1			1 1 ▽		1Y1
1A3 $51$ 6       1Y3         1A4 $49$ $8$ 1Y4         1A5 $49$ $8$ 1Y4         1A5 $48$ $9$ 1Y5         1A6 $47$ $10$ 1Y7         1A8 $44$ $11$ $10$ 1A7 $45$ $12$ $1Y8$ 1A9 $43$ $11$ $1Y9$ 1A10 $42$ $1$ $2 \lor$ 2A1 $41$ $11$ $2 \lor$ 2A2 $40$ $17$ $2Y2$ 2A3 $38$ $19$ $2Y4$ 2A4 $37$ $20$ $2Y4$ 2A5 $36$ $211$ $2Y6$ 2A6 $34$ $233$ $2Y7$ 2A8 $31$ $226$ $2Y9$ 2A9 $30$ $277$ $279$	1A2		1			1Y2
$1A4$ $49$ $8$ $1Y4$ $1A5$ $49$ $8$ $1Y5$ $1A6$ $47$ $10$ $1Y7$ $1A7$ $45$ $12$ $1Y6$ $1A7$ $45$ $12$ $1Y7$ $1A8$ $44$ $13$ $1Y9$ $1A9$ $43$ $14$ $1Y9$ $1A10$ $42$ $1 2 \bigtriangledown$ $15$ $2Y1$ $2A1$ $41$ $112 \lor$ $177$ $2Y3$ $2A4$ $37$ $20$ $2Y4$ $2Y4$ $2A5$ $36$ $211$ $2Y6$ $2Y7$ $2A8$ $31$ $226$ $2Y9$ $2Y8$ $2A9$ $30$ $277$ $2Y9$ $2Y9$	1A3		-			1Y3
1A5 $\frac{49}{48}$ 8       1Y5         1A6 $\frac{47}{45}$ 10       1Y7         1A7 $\frac{45}{45}$ 12       1Y7         1A8 $\frac{44}{44}$ 13       1Y7         1A8 $\frac{44}{44}$ 13       1Y9         1A10 $\frac{42}{42}$ 1 $2 \lor$ 15         2A1 $\frac{41}{41}$ 1 $2 \lor$ 16         2A2 $\frac{40}{37}$ 17 $2Y2$ $2Y3$ 2A4 $\frac{37}{36}$ 20 $2Y4$ $2Y5$ 2A6 $\frac{34}{24}$ 23 $2Y7$ $2X8$ 2A9 $\frac{31}{30}$ $227$ $2Y9$ $2Y8$	1A4	51	-		6	1Y4
1A6 $\frac{48}{47}$ 9       1Y6         1A7 $\frac{45}{47}$ 10       1Y7         1A8 $\frac{44}{44}$ 12       1Y8         1A9 $\frac{43}{43}$ 14       1Y9         1A10 $\frac{42}{42}$ 1 $2\nabla$ 15         2A1 $\frac{41}{41}$ 1 $2\nabla$ 16         2A2 $\frac{40}{37}$ 17 $2Y3$ 2A4 $\frac{37}{36}$ 20 $2Y5$ 2A6 $\frac{34}{34}$ 23 $2Y7$ 2A8 $\frac{31}{30}$ $226$ $2Y9$		49			8	
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$		48			9	
1A8 $45$ 12       1Y8         1A9 $44$ 13       1Y9         1A10 $43$ 14       1Y10         2A1 $42$ 1 $2 \bigtriangledown$ 15         2A1 $41$ 1 $2 \lor$ 16 $2 Y2$ 2A3 $38$ 19 $2 Y4$ 2A4 $37$ 20 $2 Y4$ 2A5 $36$ 21 $2 Y5$ 2A6 $34$ 23 $2 Y7$ 2A8 $31$ 26 $2 Y9$ 30 $277$ $277$		47			10	
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$		45			12	
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	1 <b>A</b> 8	44	1		13	1Y8
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	1 <b>A9</b>					1Y9
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	1A10					1Y10
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	2A1			1 2 ▽		2Y1
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	2A2		-			2Y2
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	2A3	40			17	2Y3
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$		38			19	
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$		37			20	
2A7     34     23     2Y7       2A8     33     24     2Y8       2A9     30     27     2Y9		36	┣───		21	
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$		34			23	
2A8         2Y8           2A9         31         26         2Y9           30         27         2Y9		33	1		24	
2A9 2Y9			1			2Y8
2A10 2Y10	2A9					2Y9
	2A10				21	2Y10

<sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, V <sub>CC</sub> Input voltage range, V <sub>I</sub> (see Note 1) Voltage range applied to any output in the high or power-off state, V <sub>O</sub>	–0.5 V to 7 V
Current into any output in the low state, I <sub>O</sub> : SN54ABT16827	
SN74ABT16827	128 mA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DL package	
Storage temperature range, T <sub>stg</sub>	

<sup>+</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

#### recommended operating conditions (see Note 3)

			SN54AB	Г16827	SN74AB	Г16827	UNIT
			MIN	MAX	MIN	MAX	UNIT
VCC	Supply voltage	4.5	5.5	4.5	5.5	V	
VIH	High-level input voltage		2		2		V
VIL	Low-level input voltage		0.8		0.8	V	
VI	Input voltage	0	Vcc	0	VCC	V	
ЮН	High-level output current		.4	-24		-32	mA
IOL	Low-level output current		(C)	48		64	mA
A #/ A	logut transition rise or fall rate	Control pins	20	4		4	ns/V
$\Delta t/\Delta v$	Input transition rise or fall rate Data pins		8	10		10	115/ V
$\Delta t / \Delta V_{CC}$	Power-up ramp rate		200		200		μs/V
T <sub>A</sub>	Operating free-air temperature		-55	125	-40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.



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#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST C	Т	A = 25°C	;	SN54AB	T16827	SN74AB1	16827	UNIT		
			MIN	TYP <sup>†</sup>	MAX	MIN	MAX	MIN MAX		UNIT		
VIK		V <sub>CC</sub> = 4.5 V,	lj = -18 mA			-1.2		-1.2		-1.2	V	
		V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -3 mA	2.5			2.5		2.5			
Vari		V <sub>CC</sub> = 5 V,	$I_{OH} = -3 \text{ mA}$	3			3		3		v	
∨он		V <sub>CC</sub> = 4.5 V	I <sub>OH</sub> = -24 mA	2			2				v	
		VCC = 4.5 V	I <sub>OH</sub> = -32 mA	2*					2			
VOL		V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 48 mA			0.55		0.55			V	
VOL		VCC = 4.5 V	I <sub>OL</sub> = 64 mA			0.55*				0.55	v	
V <sub>hys</sub>					100						mV	
II		$V_{CC} = 0$ to 5.5 $V_I = V_{CC}$ or GN				±1		±1		±1	μΑ	
I <sub>OZPU</sub> ‡	:	$V_{CC} = 0 \text{ to } 2.1$ $V_{O} = 0.5 \text{ V to } 2$				±50		±50		±50	μΑ	
I <sub>OZPD</sub> ‡	:	$V_{CC} = 2.1 V to$ $V_{O} = 0.5 V to 2$	0, 7 V, <del>OE</del> = X			±50	40	±50		±50	μΑ	
IOZH		$V_{CC} = 2.1 \text{ V}$ to $V_{O} = 2.7 \text{ V}$ , OE				10	Pool	10		10	μΑ	
I <sub>OZL</sub>		$V_{CC} = 2.1 \text{ V} \text{ to}$ $V_{O} = 0.5 \text{ V}, \text{ OE}$				-10	Q	-10		-10	μA	
loff		$V_{CC} = 0,$	VI or VO $\leq 4.5$ V			±100				±100	μA	
ICEX	Outputs high	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 5.5 V			50		50		50	μA	
ΙΟ§		V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V	-50	-100	-180	-50	-180	-50	-180	mA	
	Outputs high					2		2		2		
ICC	Outputs low	V <sub>CC</sub> = 5.5 V, I <sub>C</sub> V <sub>I</sub> = V <sub>CC</sub> or GN				32		32		32	mA	
	Outputs disabled					2		2		2		
${}^{\Delta I}CC^{\P}$		$V_{CC} = 5.5 V, O$ Other inputs at	ne input at 3.4 V, V <sub>CC</sub> or GND			1.5		1.5		1.5	mA	
Ci		V <sub>I</sub> = 2.5 V or 0.	5 V		3						pF	
Co		$V_{O} = 2.5 V \text{ or } C$	0.5 V		7.5						pF	

\* On products compliant to MIL-PRF-38535, this parameter does not apply.

<sup>†</sup> All typical values are at  $V_{CC} = 5$  V.

<sup>‡</sup> This parameter is characterized, but not production tested.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

 $\P$  This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

#### switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			SN54ABT16827		SN74ABT16827	
			MIN	TYP	MAX	MIN	ΜΑΧ	MIN	MAX	
<sup>t</sup> PLH	٨	Y	1	1.9	3.1	1	3.6	1	3.4	
<sup>t</sup> PHL	A		1	2.1	3.7	1	4.5	1	4.2	ns
<sup>t</sup> PZH		V	1	2.8	5	1 L	5.9	1	5.6	20
<sup>t</sup> PZL	OE	Y	1	2.8	4.9	377	5.8	1	5.5	ns
<sup>t</sup> PHZ	OE	Y	2.4	4.5	6.5	2.4	6.8	2.4	6.6	20
<sup>t</sup> PLZ	UE		1.6	3.7	5.7	<b>X</b> 1.6	7.1	1.6	6.1	ns

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### SN54ABT16827, SN74ABT16827 20-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS SCBS220C - JUNE 1992 - REVISED MAY 1997

7 V **S1** O Open **500** Ω From Output  $\Lambda \Lambda A$ TEST **S**1 **Under Test** GND С Open tPLH/tPHL  $C_L = 50 \text{ pF}$ tPLZ/tPZL 7 V **500** Ω (see Note A) tPHZ/tPZH Open LOAD CIRCUIT 3 V **Timing Input** 1.5 V 0 V tw th t<sub>su</sub> 3 V 3 V 1.5 V Input 1.5 V 1.5 V 1.5 V **Data Input** 0 V 0 V **VOLTAGE WAVEFORMS VOLTAGE WAVEFORMS** PULSE DURATION SETUP AND HOLD TIMES 3 V 3 V Output 1.5 V 1.5 V 1.5 V 1.5 V Input Control 0 V 0 V <sup>t</sup>PZL <sup>t</sup>PHL **tPLH** <sup>t</sup>PLZ Output 3.5 V ۷он Waveform 1 1.5 V 1.5 V 1.5 V Output V<sub>OL</sub> + 0.3 V S1 at 7 V VOL VOL (see Note B) <sup>t</sup>PHZ **t**PLH tPHL tp7H Output VOH ۷он V<sub>OH</sub> – 0.3 V Waveform 2 1.5 V 1.5 V 1.5 V Output S1 at Open 0 V VOL (see Note B) **VOLTAGE WAVEFORMS VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES** ENABLE AND DISABLE TIMES INVERTING AND NONINVERTING OUTPUTS LOW- AND HIGH-LEVEL ENABLING

## PARAMETER MEASUREMENT INFORMATION

NOTES: A. CL includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>O</sub> = 50  $\Omega$ , t<sub>f</sub>  $\leq$  2.5 ns, t<sub>f</sub>  $\leq$  2.5 ns.

D. The outputs are measured one at a time with one transition per measurement.

#### Figure 1. Load Circuit and Voltage Waveforms



### PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74ABT16827DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT16827DLG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT16827DLR	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT16827DLRG4	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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## TAPE AND REEL INFORMATION





# QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal	

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT16827DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1



# PACKAGE MATERIALS INFORMATION

11-Mar-2008



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT16827DLR	SSOP	DL	56	1000	346.0	346.0	49.0

# **MECHANICAL DATA**

MSSO001C - JANUARY 1995 - REVISED DECEMBER 2001

#### PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

DL (R-PDSO-G\*\*)



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MO-118



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