NIPPON PRECISION CIRCUITS INC.

SM8224C

Dual-Tone Receiver IC

OVERVIEW

The SM8224C is a receiver and decoder that supports the Bellcore TR-NWT-000030 and SR-TSV-002476 standards calling number identification (caller ID) and call waiting dual-tone signals. It has separate caller ID signal and call waiting signal inputs, which allows the gain for each input to be adjusted independently. It is fabricated in CMOS and features a power-down function, realizing low power dissipation operation.

FEATURES

- TR-NWT-000030 and SR-TSV-002476 standards (Bellcore)
- Call waiting
- FSK decoder
- High input sensitivity
- Independent input gain adjustment for caller ID signal and call waiting signal inputs
- Power-down mode
- Crystal oscillator circuit built-in
- Single supply operation:4.5 to 5.5V
- Molybdenum-gate CMOS process
- Package: 20-pin SSOP

APPLICATIONS

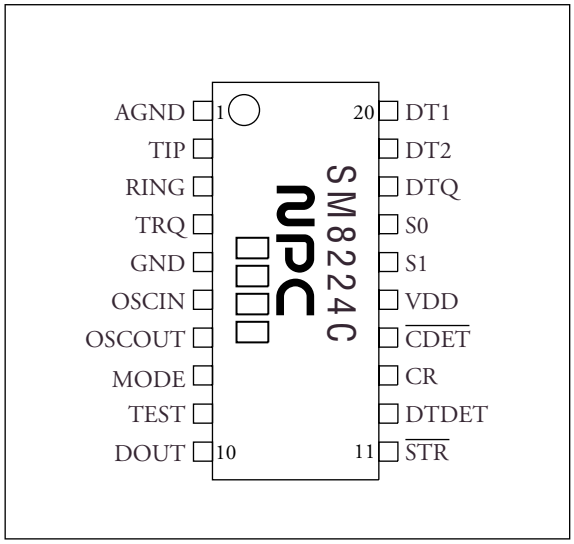
- Telephones, fax machines and modems that support pre- and mid-conversation information services
- Adapters for pre- and mid-conversation information service functions
- Telephone answering machines
- Facsimile machines
- Computer peripheral equipment

ORDERING INFORMATION

Device	Package
SM8224CM	20-pin SSOP

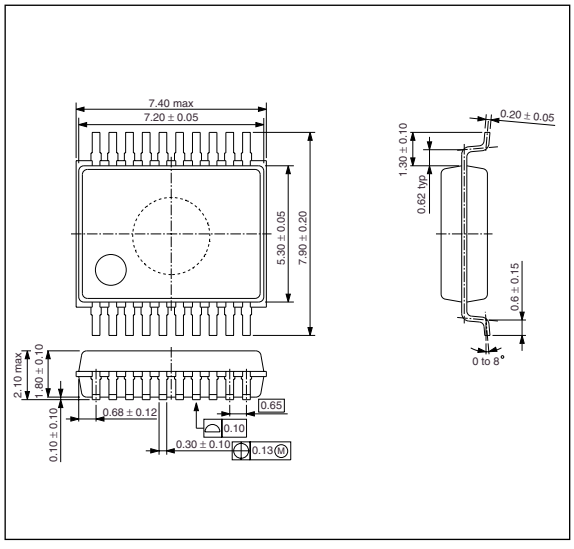
PINOUT

(Top view)

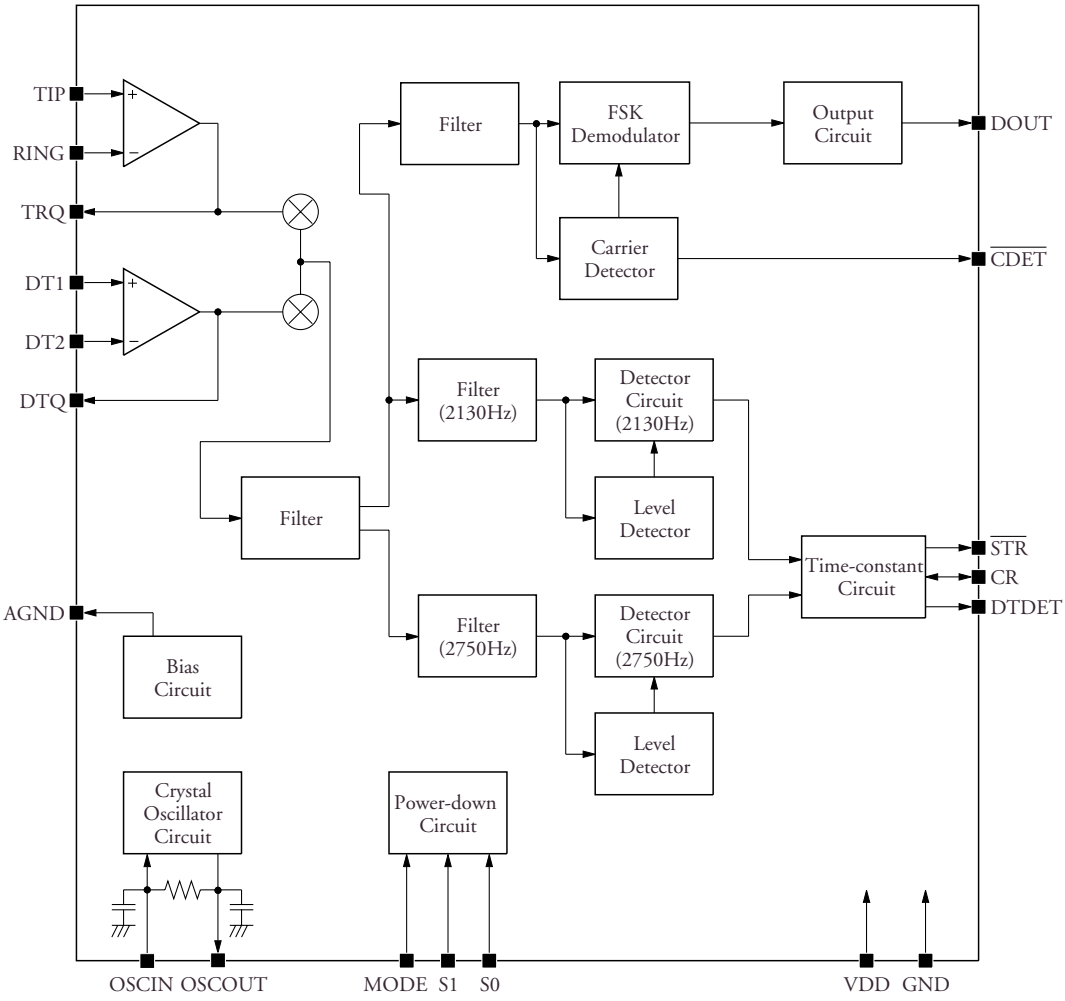


PACKAGE DIMENSIONS

(Unit: mm)



BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	I/O	Function
1	AGND	O	Reference voltage output. Internal reference voltage (V_{DD}/2) output level
2	TIP	I	Tip input. Connected to the telephone line through a protection circuit
3	RING	I	Ring input. Connected to the telephone line through a protection circuit
4	TRQ	O	Input-stage amplifier gain-select output. Used to adjust the gain of the input-stage amplifier.
5	GND	–	Ground. Connected to the system ground potential.
6	OSCIN	I	Crystal oscillator input. The crystal oscillator element is connected between this pin and OSCOUT.
7	OSCOUT	O	Crystal oscillator output. The crystal oscillator element is connected between this pin and OSCIN.
8	MODE	I	When MODE is HIGH, and S1 and S0 are both LOW, the device is in power-down state. See table 2.
9	TEST	–	TEST pin. Set OPEN when normal using.
10	DOUT	O	Data output. Demodulated FSK signal output. HIGH level output when $\overline{\text{CDET}}$ goes HIGH.
11	$\overline{\text{STR}}$	O	Dual-tone confirmation output. Function is selected by S0 and S1. See table 2. Dual-tone confirmation: Active-LOW output when dual tone detection signal passes through RC time constant delay circuit.
12	DTDET	O	Dual-tone detector output. HIGH-level output when dual tone is detected.
13	CR	I/O	Dual tone RC time constant circuit connection. The dual tone detection signal passes through the RC network to generate the $\overline{\text{STR}}$ signal.
14	$\overline{\text{CDET}}$	O	FSK signal carrier detector output. LOW-level when active carrier is detected.
15	VDD	–	Supply
16	S1	I	Function select bit 1. Selects the device mode in combination with S0 and MODE. See table 2.
17	S0	I	Function select bit 1. Selects the device mode in combination with S1 and MODE. See table 2.
18	DTQ	O	Dual-tone signal input-stage amplifier output. Used to adjust the gain of the input-stage amplifier.
19	DT2	I	Dual-tone signal input-stage operational amplifier inverting input
20	DT1	I	Dual-tone signal input-stage operational amplifier non-inverting input

SPECIFICATIONS

Absolute Maximum Ratings

GND = 0V

Parameter	Symbol	Condition	Rating	Unit
Supply voltage range	V_{DD}		– 0.5 to 7.0	V
Input voltage range	V_{IN}		– 0.3 to V_{DD} + 0.3	V
Power dissipation	P_D		44	mW
Storage temperature range	T_{stg}		–40 to 125	°C

Recommended Operating Conditions

GND = 0V

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Supply voltage	V_{DD}		4.5	–	5.5	V
Clock frequency	f_{CLK}		–	3.579545	–	MHz
Clock frequency accuracy	Δf_C		–0.1	–	+0.1	%
Operating temperature	T_{opr}		–20	–	85	°C

Electrical Characteristics

V_{DD} = 5.0V ± 0.5V, GND = 0V, f_{CLK} = 3.579545MHz, T_a = –20 to 85°C unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Supply current consumption	I_{DD}	No analog signal input, no output load, S1 = 0V, S0 = V_{DD}, MODE = 0V	–	–	8.0	mA
Power-down current	I_{DPD}	No analog signal input, other inputs = V_{DD} or 0V, no output load, S1 = 0V, S0 = 0V, MODE = V_{DD}	–	–	15	µA
MODE, S0, S1 LOW-level input voltage	V_{IL1}		–	–	$0.3V_{DD}$	V
MODE, S0, S1 HIGH-level input voltage	V_{IH1}		$0.7V_{DD}$	–	–	V
OSCIN LOW-level input voltage	V_{IL2}		–	–	$0.3V_{DD}$	V
OSCIN HIGH-level input voltage	V_{IH2}		$0.7V_{DD}$	–	–	V
DOUT, $\overline{\text{STR}}$, DTDET, CR, $\overline{\text{CDET}}$ LOW-level output current	I_{OL}		2	–	–	mA
DOUT, $\overline{\text{STR}}$, DTDET, CR, $\overline{\text{CDET}}$ HIGH-level output current	I_{OH}		–	–	–0.8	mA
TIP, RING, DT1, DT2, MODE, S1, S0 input leakage current	I_{IN}		–1	–	1	µA

AC Electrical Characteristics

Measurement conditions: R1 = 430kΩ, R2 = 34kΩ, R3 = 390kΩ, C1= 0.22μF

FSK decoder

V_{DD} = 5.0V ± 0.5V, GND = 0V, f_{CLK} = 3.579545MHz, T_a = –20 to 85°C unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Input sensitivity			–	–43	CD_{ON}	dBm
S/N ratio[1]	FSKSNR		20	–	–	dB
Carrier detection sensitivity	CD_{ON}		–	–43	–37.78	dBm
Carrier non-detection sensitivity	CD_{OFF}		–50	–46	–	dBm
Oscillator frequency	f_{CLK}		typ – 0.1%	3.579545	typ + 0.1%	MHz

1. Mark signal and SPACE signal are same level.
   Noise: Random noise from 200Hz to 3400Hz.

Dual tone detector

V_{DD} = 5.0V ± 0.5V, GND = 0V, f_{CLK} = 3.579545MHz, T_a = –20 to 85°C unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Frequency (low frequency)	f_L		–	2130	–	Hz
Frequency (high frequency)	f_H		–	2750	–	Hz
Detection frequency deviation			1.1	–	–	%
Non-detection frequency deviation			3.5	–	–	%
Detection sensitivity			–37.78	–	–	dBm
Non-detection sensitivity			–	–	–43.78	dBm
Signal level deviation			–	–	6	dB

Note: (S0, S1, MODE) = (V_{DD}, 0V, 0V)

Input-stage amplifier Characteristics

V_{DD} = 5.0V ± 0.5V, GND = 0V, f_{CLK} = 3.579545MHz, T_a = –20 to 85°C unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Input leakage current	I_{IN}		–	–	1	μA
DC open-loop voltage gain	G_{OL}		30	–	–	dB
Unity gain frequency	f_C		80	–	–	kHz
Load capacitance	C_L		–	–	100	pF
Load resistance	R_L		50	–	–	kΩ

Timing Characteristics

FSK decoder

V_{DD} = 5.0V ± 0.5V, GND = 0V, f_{CLK} = 3.579545MHz, T_a = −20 to 85°C unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Power-down release to start-up time	t_{DOSC}		–	5	–	ms
Carrier detection ON time	t_{DAQ}		2.5	–	10	ms
Final data to carrier detection OFF time	t_{DCH}		3	–	15	ms

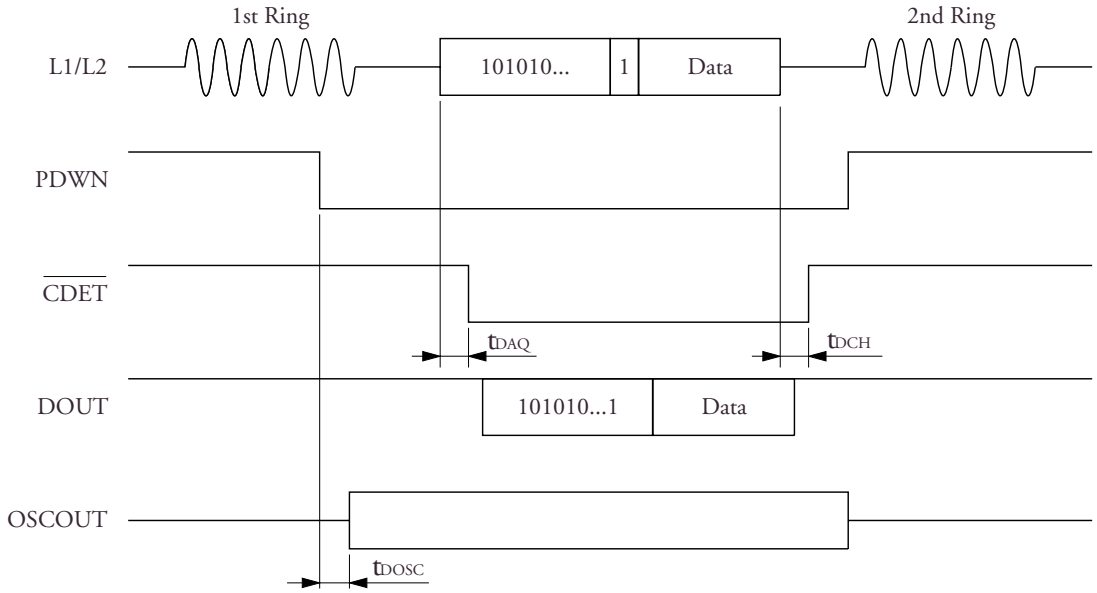
Output timing

V_{DD} = 5.0V ± 0.5V, GND = 0V, f_{CLK} = 3.579545MHz, T_a = −20 to 85°C, FSK input data = 1200 ± 12 baud unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
$\overline{STR}$, DOUT rise time	t_{r0}		–	–	200	ns
$\overline{STR}$, DOUT fall time	t_{f0}		–	–	200	ns
Input/output delay	t_{IDD}	Input to DOUT	–	–	5	ms
DOUT data rate			1188	1200	1212	baud

TIMING DIAGRAMS

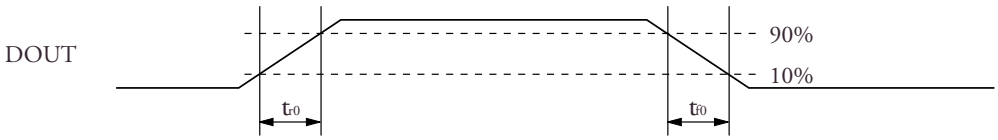
FSK demodulator timing



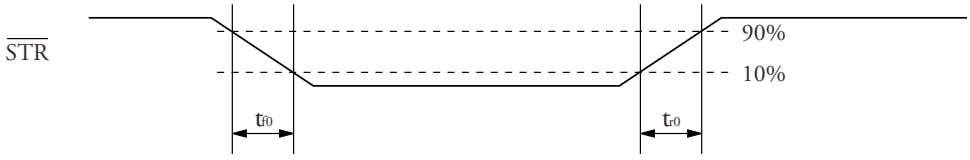
PDWN is an internal signal (set by S0, S1, MODE)

Output timing

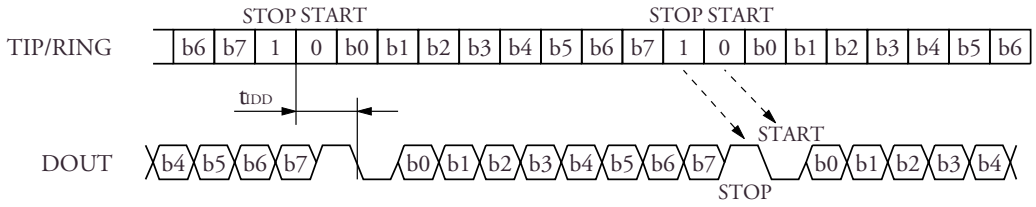
DOUT



$\overline{STR}$



Data timing



FUNCTIONAL DESCRIPTION

The SM8224C receiver with caller ID service conforms to the Bellcore standards. It incorporates FSK demodulator and dual-tone detection functions in a single chip. It has a dedicated dual-tone signal input so that the FSK signal input amplification and dual-tone signal input amplification can be set independently. This allows systems can be easily constructed that provide pre- and mid-conversation information services.

FSK Demodulator

Calling number identification service is sent as an FSK signal, and the SM8224C FSK demodulator processes this signal.

The FSK signal conforms to the following Bellcore standard.

Table 1. FSK signal

Parameter	Description
Modulation type	Continuous-phase binary frequency-shift-keying
Logic “1” data (mark)	1200 ± 12 Hz
Logic “0” data (space)	2200 ± 22 Hz
Signal level (mark)	−32 to −12 dBm
Signal level (space)	−36 to −12 dBm
Data transfer rate	1200 ± 12 baud

Table 2. Function select

S1	S0	MODE	Function	$\overline{\text{STR}}$
LOW	LOW	HIGH	Power-down	HIGH
HIGH	LOW	LOW	Dual-tone detection from DT1/DT2[1]	LOW (dual tone confirmation)
LOW	HIGH	LOW	FSK and dual-tone detection from TIP/RING	LOW (dual tone confirmation)
HIGH	HIGH	LOW	FSK detection from TIP/RING	HIGH
LOW	LOW	LOW	Test mode[2]	

1. DT1, DT2, DTQ are active in this mode only.
2. Test mode should not be used.

Note: S1, S0, MODE setting should be used from above combination except Test mode.

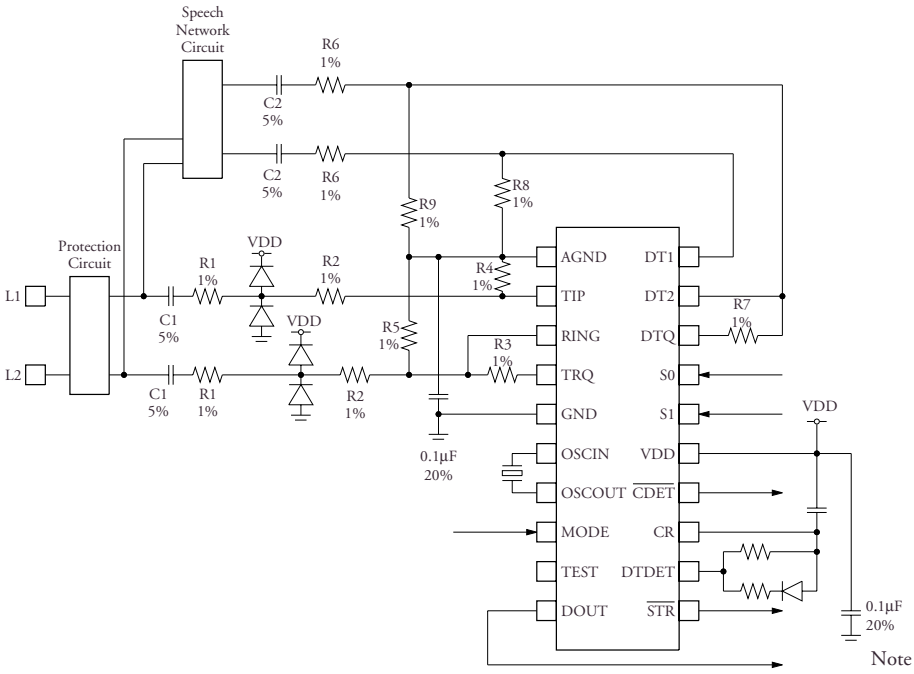
Dual Tone Detector

When using mid-conversation information services, 2 mixed signals of 2130Hz and 2750Hz are sent on lines L1 and L2. The SM8224C detects the 2 signals from the background noise. It uses 2 separate high-order filters with center frequencies of 2130Hz and 2750Hz to detect the presence of the signal frequencies.

In series with the filters are level detectors. When the input level exceeds the preset rating, the signal is detected. When the input level is below the rating, the signal is not detected.

If both the 2130Hz and 2750Hz signals are simultaneously detected, DTDET goes HIGH and starts charging the time constant circuit comprised by an external capacitor and external resistor. When the time constant circuit voltage rises above a fixed voltage level, $\overline{\text{STR}}$ signal goes LOW to indicate dual tone detection.

TYPICAL APPLICATION CIRCUIT



Note : Please set this capacitor nearby IC pin.

Symbol	Rating[1]	Unit
R_1	330	kΩ
R_2	27	kΩ
R_3	220	kΩ
C_1	0.001	µF
R_4	47.5	kΩ
R_5	60.4	kΩ
R_6	430 + 34	kΩ
R_7	390	kΩ
C_2	0.22	µF
R_8	52.3	kΩ
R_9	60.4	kΩ

1. Circuit values are preliminary.

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