MOS IC

Type	Ordering code	Package
SDA 2010	Q67120–C74	DIP 40

Features

- 8-bit CPU, ROM, RAM, I/O in a DIP 40 package
- 4 analog outputs with 6 bit resolution
- 30 digital I/O lines
  two serial interfaces
  two 8-bit interfaces
  two 4-bit interfaces
  two test inputs
- 2 Kbyte ROM
- 64 byte RAM
- 7.5 µs cycle time at 4 MHz crystal frequency – 1 or 2 cycles per instruction
- Zero passage detector
- Interface for modulated digital signal
- Interval timer/counter
- 5 V supply voltage
- SAB 8048 instruction subset

Circuit description[1)]

The SDA 2010 stresses application-specific control functions surpassing the former purely numeric computation performance. As a result, the use of additional hardware could be reduced and software operations have been simplified, optimizing cost savings during the developmental and production stages. Although the SDA 2010 was designed for electronic entertainment devices, it is equally suitable for mass-produced applications requiring highly economic components.

The SDA 2010 includes a 2 Kbyte program memory (ROM), a 64 byte data memory (RAM) and four 6-bit D/A converters. The 30 digital I/O lines are comprised of two 4 and 8-bit ports each, two test inputs and 2 serial interfaces consisting of one data and one clock line each. Test input T0 processes signals modulated with approx. 30 kHz and is equipped with a digital demodulator, which derives the envelope curve from the modulated digital signal. Since the digital demodulator forwards an unmodulated signal without changing it, test input T0 can also function as a normal digital input during operations with standard H/L levels. Test input T1 includes a zero passage detector and can also serve as a normal digital input. The SDA 2010 is equipped with its own oscillator and timer/counter.

1) Detailed description is available upon request

The instruction set includes 65 instructions (1-2 bytes), which can be processed in max. 2 cycles. Numerical problems can be processed in either binary or BCD arithmetic modes. The large number of available bit-handling instructions increases the efficiency of the controller functions.

Program development and system testing for the SDA 2010 are carried out on the SME development system in conjunction with the SDA 2010 emulator board EMB U2. The EMB U2 emulator consists of one 2 K EPROM (SAB 2716) as well as a 40 pin socket which is used to insert an SAB 8035 type microprocessor or an ICE 48 plug. In addition, the EMB U2 contains all the necessary hardware to simulate the four analog outputs and the serial and parallel interfaces of the SDA 2010. A 40 wire cable is used to connect the U2 emulator with the user system.

A version without the ROM (SDA 3010) is available for in-house software development on an SME system.

Maximum ratings

Supply voltage range	V_{CC}	−0.5 to 7	V
Voltage between any pin and ground	V	−0.5 to 7	V
Total power dissipation	P_{tot}	1	W
Storage temperature range	T_{stg}	−40 to 125	°C

Operating range

Supply voltage	V_{CC}	5 ± 10%	V
Ambient temperature	T_A	0 to 70	°C

DC characteristics

$T_A = 0\,°C$ to $70\,°C$, $V_{CC} = 5\,V \pm 10\%$; $V_{SS} = 0\,V$

			min	max	
L input voltage	(Ports, SS0, SS1, RESET, T0, T1, X1)	V_{iL}	−0.5	0.8	V
H input voltage	(Ports, SS0, SS1) $V_{CC} = 5.0\,V \pm 10\%$	V_{iH}	2.0	V_{CC}	V
H input voltage	(Ports, SS0, SS1) $V_{CC} = 6.0\,V \pm 0.5\,V$	V_{iH1}	2.4	V_{CC}	V
H input voltage	(RESET, X1, T0, T1)	V_{iH2}	3.5	V_{CC}	V
L output voltage	(Ports, ALE) $I_{qL} = 1.6\,mA$	V_{qL}		0.45	V
L output voltage	(SS0, SS1, SCP0, SCP1) $I_{qL} = 4\,mA$	V_{qL1}		0.45	V
L output voltage	(A00-A03) $I_{qL} = 4\,mA$	V_{qL2}		0.45	V
H output voltage	(Ports, ALE) $I_{qH} = 50\,\mu A$	V_{qH}	2.4		V
H output voltage	(SS0, SS1, SCP1) $I_{qH} = 150\,\mu A$	V_{qH1}	2.4		V
H output voltage	(A00-A03) $I_{qH} = 4\,mA$	V_{qH2}	V_{CC}−0.45		V
H input current	(T0, T1) $V_{iH} = V_{CC}$	I_{iH}		10	µA
L input current	(Ports, SS0, SS1) $V_{iL} = 0.45\,V$	$-I_{iL}$	30	340	µA
Input voltage at T1	($C_i = 1\,\mu F$) (peak-to-peak)	V_{T1}	1	3	V
Zero passage detector current consumption		I_{CC}		80	mA

AC characteristics

$T_A = 0\,°C$ to $70\,°C$, $V_{CC} = 5\,V \pm 10\%$; $V_{SS} = 0\,V$

		min	max	
Cycle time 3 MHz crystal; = 10 µs	t_C	10	50	µs
ALE pulse width $t_C = 10\,\mu s$	t_{ALE}	1.3		µs
Oscillator frequency deviation $f = 2.5\,MHz$, $R = 15\,k\Omega$	Δf_{OSC}	−20	+20	%
Length of an unmodulated signal at the T0 test input 3 MHz crystal	t_{MT0}	60	—	µs
Frequency of a modulated signal at the T0 test input 3 MHz crystal	f_{TR}	30	35	kHz
Frequency range of the zero passage detector (input T1)	f_{T1}	0.03	1	kHz

Pin description

Pin	Symbol	Function
40	V_{CC}	+ 5 V
20	V_{SS}	GND 0 V
21, 22	X1, X2	Connection for crystal or similar
10–17	P0 0–7	Quasi-bidirectional 8-bit port
24–31	P1 0–7	Quasi-bidirectional 8-bit port
32–35	P2 0–3	Quasi-bidirectional 4-bit port
7–4	P3 0–3	Quasi-bidirectional 4-bit port
38, 39, 1, 2	A00–A0–A3	4 analog outputs. The analog values are output as rectangular signals with a frequency of approx. 2 kHz, during which the duty cycle corresponds to the analog value.
37, 8	SS0, SS1	Serial interface I/O pin
36, 9	SCP0, SCP1	Serial interface clock pulse
23	RESET	Reset input for the initialization of the computer. Resets program counter, erases the status FFs. Sets all digital outputs to the H state (active H).
3	T0	Input that can be tested with the conditional jump instructions JT0 and JNT0. The input contains a digital demodulator and can be used for the separation of the envelope curve from a modulated signal.
19	T1	Input that can be tested with the conditional jump instructions JT1 and JNT1. Serves simultaneously as an external counter input. (Selection of functions with instruction STRT CNT). The input can also be used for zero passage recognition of low frequency alternating voltages.
18	ALE	This output generates one clock pulse signal per cycle.

SDA 2010 instruction set

	Mnemonic	Description	Bytes	Cycles	Hexadecimal opcode
Accumulator	ADD A, Rr	Add register to A	1	1	68–6F
	ADD A, @ R	Add data memory to A	1	1	60–61
	ADD A, #data	Add immediate to A	2	2	03
	ADDC A, Rr	Add register with carry	1	1	78–7F
	ADDC A, @ R	Add data memory with carry	1	1	70–71
	ADDC A, #data	Add immediate with carry	2	2	13
	ANL A, Rr	And register to A	1	1	58–5F
	ANL A, @ R	And data memory to A	1	1	50–51
	ANL A, #data	And immediate to A	2	2	53
	ORL A, Rr	Or register to A	1	1	48–4F
	ORL A, @ R	Or data memory to A	1	1	40–41
	ORL A, #data	Or immdediate to A	2	2	43
	XRL A, Rr	Exclusive Or register to A	1	1	D8–DF
	XRL A, @ R	Exclusive Or data memory to A	1	1	D0–D1
	XRL A, #data	Exclusive Or immediate to A	2	2	D3
	INC A	Increment A	1	1	17
	DEC A	Decrement A	1	1	07
	CLR A	Clear A	1	1	27
	CPL A	Complement A	1	1	37
	DA A	Decimal adjust A	1	1	57
	SWAP A	Swap nibbles of A	1	1	47
	RL A	Rotate A left	1	1	E7
	RLC A	Rotate A left through carry	1	1	F7
	RR A	Rotate A right	1	1	77
	RRC A	Rotate A right through carry	1	1	67

SDA 2010 instruction set

	Mnemonic	Description	Bytes	Cycles	Hexadecimal opcode
I/O	IN A, Pp	Input port to A	1	2	08, 09, OC, OD
	OUT Pp, A	Output A to port	1	2	90, 39, 3C, 3D
	IN A, Sn	Input serial port to A0	1	2	OE–OF
	OUT Sn, A	Output A0 to serial port	1	2	3E–3F
Registers	INC Rr	Increment register	1	1	18–1F
	INC @ R	Increment data memory	1	1	10–11
Sub-routines	CALL	Jump to subroutine	1	2	14, 34, 54, 74, 94, B4, D4, F4,
	RET	Return	1	2	83
Branches	JMP adr	Jump unconditional	2	2	04, 24, 44, 64, 84, A4, C4, E4
	JMPP @ A	Jump indirect	1	2	B3
	DJNZ Rr, adr	Decrement register and jump on R not zero	2	2	E8–EF
	JC adr	Jump on carry = 1	2	2	F6
	JNC adr	Jump on carry = 0	2	2	E6
	JZ adr	Jump on A zero	2	2	C6
	JNZ adr	Jump on A not zero	2	2	96
	JT0 adr	Jump on T0 = 1	2	2	36
	JNT0 adr	Jump on T0 = 0	2	2	26
	JT1 adr	Jump on T1 = 1	2	2	56
	JNT1 adr	Jump on T1 = 0	2	2	46
	JTF adr	Jump on timer flag	2	2	16
Flags	CLR C	Clear carry	1	1	97
	CPL C	Complement carry	1	1	A7

SDA 2010 instruction set

	Mnemonic	Description	Bytes	Cycles	Hexadecimal opcode
Transfer instructions	MOV A, Rr	Move register to A	1	1	F8–FF
	MOV A, @ R	Move data memory to A	1	1	F0–F1
	MOV A, #data	Move immediate to A	2	2	23
	MOV Rr, A	Move A to register	1	1	A8–AF
	MOV@ R, A	Move A to data memory	1	1	A0–A1
	MOV Rr # data	Move immediate to register	2	2	B8–BF
	MOV @ R, # data	Move immediate to data memory	2	2	B0–B1
	XCH A, Rr	Exchange A and register	1	1	28–2F
	XCH A, @R	Exchange A and data memory	1	1	20–21
	XCHD A,@ R	Exchange nibble of A and register	1	1	30–31
	MOVP A, @ A	Move to A from current page	1	2	A3
Timer/Counter	MOV A, T	Read timer/counter	1	1	42
	MOV T, A	Load timer/counter	1	1	62
	STRT T	Start timer	1	1	55
	STRT CNT	Start counter	1	1	45
	STOP TCNT	Stop timer/counter	1	1	65
	MOV DA, A	Move A to DA – converter	1	2	91
	NOP	No operation	1	1	00

Symbols and abbreviations

A	Accumulator
adr	11-bit program memory address
CNT	Event counter
DA	D/A converter
data	8-bit binary number
P	Mnemonic for "in page" operation
Pp	Port. label (p = 0–3)
Rr	Register label (r = 0–7)
Sn	S interface label (n = 0; 1)
T	Timer
T0, T1	Test 0, Test 1
#	Refers to immediate data
@	Refers to indirect addressing