Signetics

SAA9001
317k Bit CCD Memory

Product Specification

Linear Products

DESCRIPTION

The SAA9001 is a 1-bit wide, 317,520-bit long, charge-coupled shift register, organized in 294 blocks of 1080 bits each. It is intended for use in a TV field memory at a maximum frequency of 21.3MHz.

Control is performed by two external signals, memory clock (MC), and memory gating (MG). The circuit has two data inputs (MI_1 and MI_2) and the data may be internally recirculated. An adjustable delay of 0 to 7 bits is incorporated at the output to increment the total delay on a bit-by-bit basis, as programmed by the inputs A0, A1, and A2. All inputs, outputs, and controls are TTL-compatible.

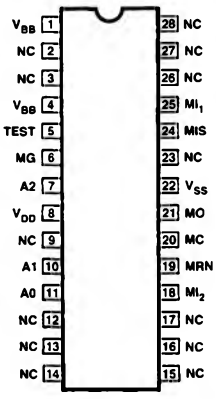
FEATURES

- **317k bits (294 × 1080)**
- **21.3MHz toggle frequency**
- **TTL-compatible**
- **28-pin DIP package**

APPLICATIONS

- **TV field memory**
- **Digitizing images**

PIN CONFIGURATION



TOP VIEW

CD12780S

PIN NO.	SYMBOL	DESCRIPTION
1	V_{BB}	Back-bias supply voltage (to be connected to Pin 4)
4	V_{BB}	Back-bias supply voltage (to be connected to Pin 1)
5	TEST	Control input for testing purposes only. It is internally connected to V_{SS} via a 1kΩ (approx.) resistor and needs no external connection
6	MG	Memory gating input
7	A2	Control input for additional internal delay
8	V_{DD}	Positive supply voltage
10	A1	Control input for additional internal delay
11	A0	Control input for additional internal delay
18	MI_2	Memory input 2
19	MRN	Memory recirculate control. Recirculation is activated when MRN is Low
20	MC	Memory clock input
21	MO	Memory output
22	V_{SS}	Negative supply voltage (ground)
24	MIS	Memory input select; selects MI_1 or MI_2
25	MI_1	Memory input 1

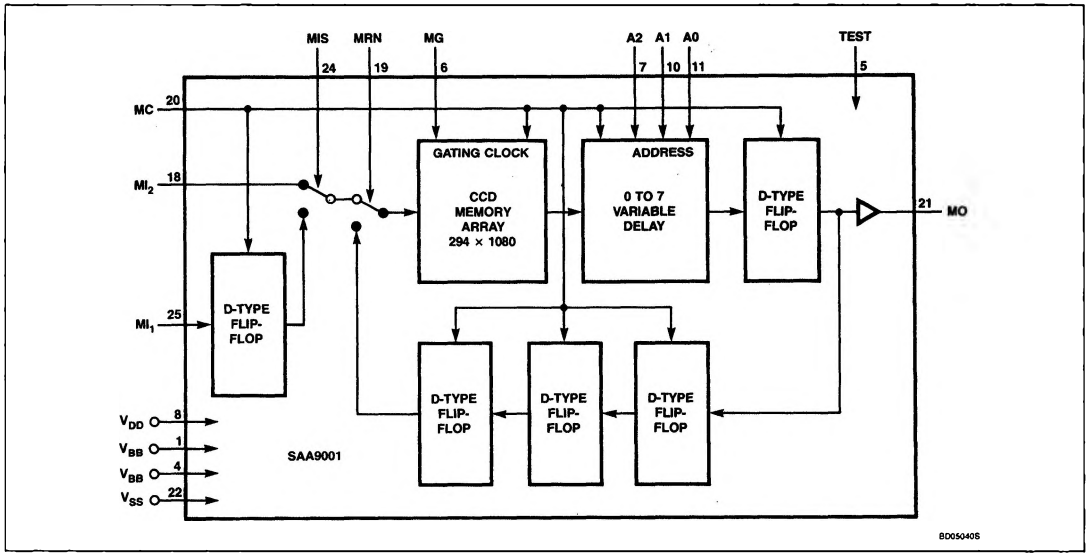
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
28-Pin Plastic DIP (SOT-117)	0 to +60°C	SAA9001N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_I, V_O	Voltage on any pin, except V_{BB} (Pin 4) and MO (Pin 21), with respect to V_{SS}	7	V
V_{BB}	Back-bias voltage	min. −7	V
I_O	DC output current (sink or source)	10	mA
T_A	Operating ambient temperature range (under DC operating conditions)	0 to 60	°C
T_{STG}	Storage temperature range	−65 to +150	°C
P_{TOT}	Total power dissipation per package	1	W

BLOCK DIAGRAM



CAPACITANCE

SYMBOL	PARAMETER	MAX	UNIT
C_I	Data inputs MI_1, MI_2 (Pins 25 and 18)	9	pF
C_C	Clock input MC (Pin 20)	9	pF
C_G	Gating input MG (Pin 6)	9	pF
C_O	Data output MO (Pin 21)	9	pF
C_{RN}	Recirculation control MRN (Pin 19)	9	pF
C_{IS}	Input select control MIS (Pin 24)	9	pF
C_A	Delay program inputs A0, A1, A2 (Pins 11, 10, and 7)	9	pF

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V_{DD}	Supply voltage range	4.75		5.25	V
V_{BB}	Back-bias supply range	−3.65		−3.35	V
V_{IL}	Input voltage Low	−1.0		+0.8	V
V_{IH}	Input voltage High	2.0		6.0	V

DC ELECTRICAL CHARACTERISTICS

$T_A = 0$ to $+60°C$; $V_{DD} = 4.75$ to $5.25V$; $V_{BB} = -3.5 \pm 0.15V$; output not loaded, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
I_{LI}	Input leakage current at V_I = GND to V_{DD}: MI_1; MI_2; MC; MG; A0; A1; A2; MRN; MIS			10	μA
I_{DD}	Power supply current from V_{DD} at f = 21.3MHz			70	mA
V_{OL}	Output voltage Low at $I_{OL} = 4mA$			0.4	V
V_{OH}	Output voltage High at $I_{OH} = -1mA$	2.4			V

AC TEST CONDITIONS

PARAMETER	LIMIT	UNIT
Input pulse levels	0.6 and 2.4	V
Rise and fall times between 0.8 and 2.0V (t_R, t_F) clock input MC data inputs MI_1, MI_2; gating input MG; control inputs A0, A1, A2, MIS, MRN	 $\leqslant 3$ $\geqslant 3$	 ns ns
Timing reference levels clock input MC data inputs MI_1, MI_2; gating input MG data output MO	 1.5 0.8 or 2.0 0.8 or 2.0	 V V V
Output load	see Figure 4	

AC ELECTRICAL CHARACTERISTICS $T_A = 0$ to $+60°C$; $V_{DD} = 4.75$ to $5.25V$; $V_{BB} = -3.5 \pm 0.15V$.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
f_{CL}	Clock frequency[1]			21.3	MHz
t_{CL}	Clock Low time	18			ns
t_{CH}	Clock High time	18			ns
t_R	Recirculation time[1]			27	ms
t_{GW}	Waiting time (gating Low/High time)[2]			1100	μs
t_{GC}	Gating setup time	7.5			ns
t_{CG}	Gating hold time	0.5			ns
t_{IC}	Data setup time	7.5			ns
t_{CI}	Data hold time	0.5			ns
t_{OH}	Output hold time	5.0			ns
t_{OD}	Output delay time			23.5	ns
t_{AH}	Output invalid after address change	0			μs
t_{AD}	Address valid after address change[3]			7 clock pulses + 1	μs
t_{MRNSU}	Recirculation setup time[4]	0		1	μs
t_{MISSU}	Input select setup time[5]	0		1 clock pulse + 1	μs

NOTES:

1. The maximum recirculation time must never be exceeded by any combination of low frequency gating and/or waiting time.
2. Every $1300\mu s$, at least three blocks of 1080 bits must be transferred to the output. This means that immediately after a wait of $1100\mu s$, three blocks must be shifted out.
3. A change in delay will cause invalid data at the output for the time t_{AD}.
4. After a change of MRN, the signal recirculation path is not switched before t_{MRNSU}.
5. After a change of MIS, data at the input is invalid for t_{MISSU}.

FUNCTIONAL DESCRIPTION

Operation

The memory array is organized to handle data in blocks of 1080 bits and has a capacity of 294 data blocks. The structure of the memory array provides fast, serial data input and output, with parallel transfer of data blocks through the memory. Memory input and output are controlled by the memory gating (MG); the serial output is initiated by the rising edge of MG, and the storage of the data present in the memory's input register is performed on the falling edge of MG. In normal operation, one cycle of MG is an uninterrupted High level of at least 1080 clock periods (−4 or +3 clock periods) followed by a Low level of at least 32 clock periods. Input, output, and gating signals are all referred to the rising edge of the memory clock (MC).

The internal recirculation facility is activated when the control input MRN is Low.

Memory output

Output is enabled when MG is High and data is clocked serially from the memory. Referring to Figure 1, the first rising clock edge after the positive transition of MG is defined as clock pulse "0". If the delay control address is A2 = A1 = A0 = 0, then the first bit of the output is valid at clock pulse "17" (the delay of 17 clock periods is due to internal multiplexing of the data in the memory).

The output delay can be increased by the values shown in Table 1 using the internal delay line controlled by A0, A1, and A2.

Table 1. Additional Delay Control

DELAY ADDRESS			ADDITIONAL DELAY (CLOCK PERIODS)
A2	A1	A0	
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Data Input

Data to be stored is directed to the memory from either MI_1 or MI_2 as selected by the control input MIS (see Table 2). The MI_1 input is delayed by one clock period.

Table 2. Input Selection

CONTROL INPUT	MEMORY INPUT
MIS = 0	MI_1
MIS = 1	MI_2

Input data is clocked serially into the input register of the CCD memory. When the negative transition of MG occurs, the 1080 bits of data present in the input register are entered into the memory array. If the interval of MG = High is not an exact multiple of eight clock periods, the timing of the negative transition of MG is internally rounded to be an exact multiple of eight clock periods. Note that the data path from input MI_1 has a delay of one clock period and the path from MI_2 is direct.

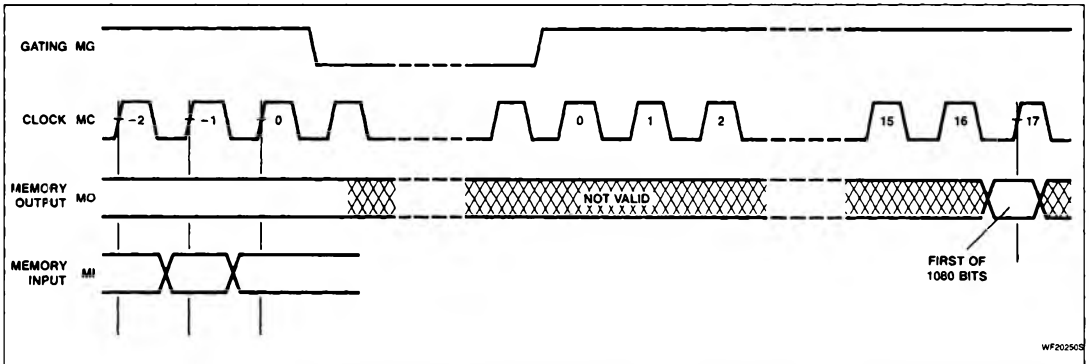


Figure 1. Memory Input and Output Data Timings With Respect to the Memory Clock (MC) for a Memory Gating (MG) High Period that is a Multiple of 8 Clock Periods (no Internal Rounding of Gating Period)

The length of the MG = High interval required for internal and external recirculation of data is determined as shown in Figure 2. The positive transition of MG (waveform 1) initiates the serial transfer of data from the output register. Due to multiplexing in the memory, valid data is available after 16 clock periods (waveform 2). After a delay of "A" clock periods, determined by A0, A1, and A2 (waveform 3), and a one-clock period delay via a D-type flip-flop, the valid data is available at the output pin MO (waveform 4).

Incoming data can be delayed by two amounts: RP (waveform 5), a phase shift introduced when the data is recirculated through an external processing circuit, and ID (waveform 6), a one-clock period delay when input MI_1 is selected. The negative transition of MG, internally rounded to a multiple of eight clock periods (waveform 7), initiates storage of the last 1080 bits presented at the memory input (waveform 6). Therefore, the MG = High interval is 16 + A + 1 + RP + ID + 1080 clock periods, and this figure is rounded to a multiple of eight. From this, (A + 1 + RP + ID) modulo 8 = 0.

During internal recirculation of the data (MRN = Low), the three D-type flip-flops in the recirculation path give RP a value of three clock periods and ID will be zero. Consequently, the variable delay should be programmed for a delay of A = 4 for proper data retention, i.e., (4 + 1 + 3 + 0) modulo 8 = 0.

In conclusion, to store 1080 bits of valid data and to retrieve at the output 1080 valid data bits, the MG = High interval must be at least 1076 clock periods followed by an MG = Low interval of at least 32 clock periods. The MG = Low interval can be reduced to a minimum of 24 clock periods when MG = High is a multiple of eight clock periods.

Fast Gating

Fast gating is a method of accelerating the internal transfer of data through the memory at the expense of valid data, and is therefore useful for skipping unwanted data blocks. The MG = High interval for fast gating is less than 1076 clock periods to a minimum of 360 clock periods. If the MG = High interval is a multiple of eight clock periods during fast gating, the MG = Low interval can be reduced to 24 clock periods (min.); otherwise, the MG = Low interval must be at least 32 clock periods. The output data is not valid during fast gating and during the first two data blocks at the output after fast gating has ceased. No valid data is clocked into the input register of the CCD memory during fast gating.

Slow Gating

The transfer of data can be decelerated by using slow gating. For this, the MG = High or MG = Low interval is extended to the maximum waiting time (t_{GW}).

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

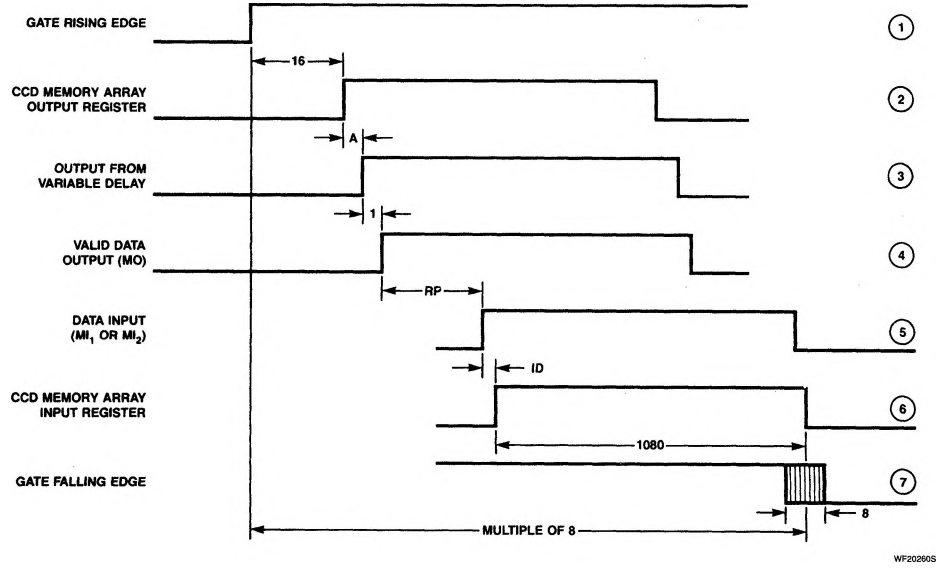


Figure 2. Determination of Memory Gating High Period

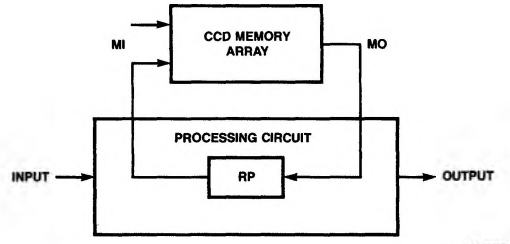


Figure 3. Recirculation via an External Circuit

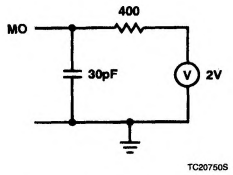


Figure 4. Output Load

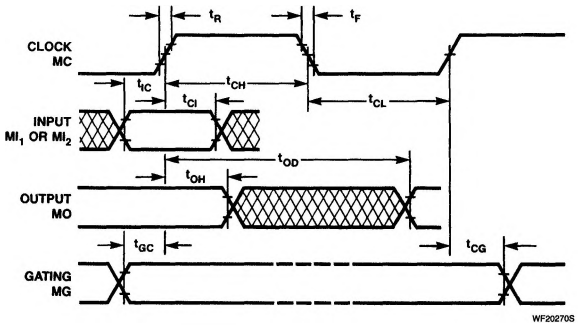


Figure 5. Timing Waveforms for Gating and I/O

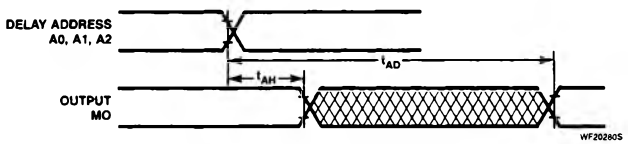


Figure 6. Timing Waveforms for Address Setup and Hold