DATA SHEET

SAA7348GP
All Compact Disc Engine (ACE)

Preliminary specification
File under Integrated Circuits, IC22

1997 Jul 11

Philips
Semiconductors

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CONTENTS

1 FEATURES

- Focus servo loop
- Radial servo loop
- Built-in access procedure with fast track count possibilities
- Sledge motor servo loop with pulsed sledge support
- High speed error correction, up to sixteen times over-speed
- Supports three different over-speed ranges with only one external crystal
- Lock-to-disc mode
- Full turntable motor control
- Full error correction strategy, t = 2 and e = 4
- All standard decoder functions implemented digitally
- Adaptive digital HF equalizer
- FIFO overflow concealment for rotational shock resistance
- Digital audio interface (EBU), audio and data
- 2 and 4 times oversampling integrated digital filter, including f_s mode
- Audio data peak level detection
- Kill interface for DAC deactivation during digital silence
- All TDA1301 (DSIC2) digital servo functions
- Low focus noise
- Improved playability on ABEX TCD-721R, TCD-725 and TCD-714 discs
- Automatic closed loop gain control available for focus and radial loops
- On chip clock multiplier allows the use of 8.4672 MHz crystal
- S2B serial interface with host controller
- Double speed servo
- Integrated engine controller (high speed embedded 80C51)
- External program support.

2 GENERAL DESCRIPTION

The SAA7348 All Compact Disc Engine (ACE) combines the functionality of a CD decoder (LO9585), a digital servo (OQ8868) and a microcontroller core (80C51 based) on a single chip. It was developed for high speed CD-ROM applications but, due to the large scale integration, can also be used in other CD applications. The internal microcontroller makes it possible to develop other applications quickly. The microcontroller can operate with internal or external ROM.

Additional features include:

- High level integration
- Improved communication speed.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAG0E		
	NAME	DESCRIPTION	VERSION
SAA7348GP	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1

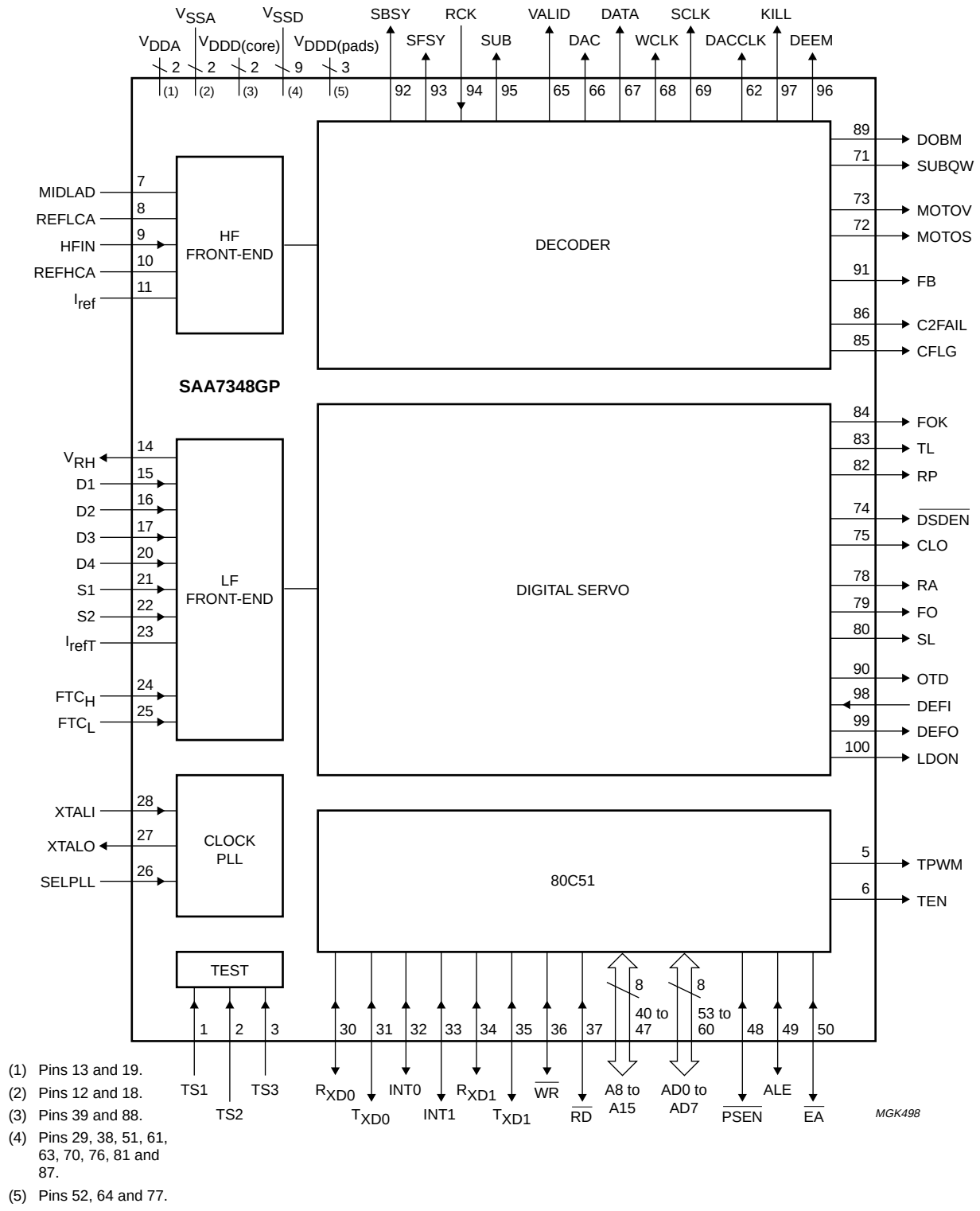
4 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{DDD(pads)}$	digital supply voltage for pad cells		4.5	5.0	5.5	V
$V_{DDD(core)}$	digital supply voltage for the core	note 1	3.0	3.3	3.6	V
V_{DDA}	analog supply voltage	note 1	3.0	3.3	3.6	V
I_{DD}	supply current	n = 8 mode	–	90	–	mA
f_{xtal}	crystal frequency		8	8.4672	35	MHz
T_{amb}	operating ambient temperature		0	–	70	°C
T_{stg}	storage temperature		–55	–	+125	°C

Note

1. The analog and digital core supply pins (V_{DDA} and $V_{DDD(core)}$) must be connected to the same external supply. The core and pads can operate at different voltages and should never be connected together directly.

5 BLOCK DIAGRAM



(1) Pins 13 and 19.
(2) Pins 12 and 18.
(3) Pins 39 and 88.
(4) Pins 29, 38, 51, 61, 63, 70, 76, 81 and 87.
(5) Pins 52, 64 and 77.

Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN	TYPE[1]	DESCRIPTION
TS1	1	I	test control input; this pin should be tied LOW
TS2	2	I	test control input; this pin should be tied LOW
TS3	3	I	test control input; this pin should be tied LOW
RST	4	I	power-on reset input
TPWM	5	O	tray PWM output
TEN	6	O	tray enable output
MIDLAD	7	A	ladder middle decoupling of High Frequency (HF) ADC
REFLCA	8	A	ladder low decoupling of HF ADC
HFIN	9	A	HF input
REFHCA	10	A	ladder high decoupling of HF ADC
I_{ref}	11	A	reference current input
V_{SSA1}	12	S	analog ground 1 for HF front-end
V_{DDA1}	13	S	analog supply voltage 1 for HF front-end (3.3 V)
V_{RH}	14	A	calibrated reference voltage output from ADC
D1	15	A	unipolar current input (central diode signal input)
D2	16	A	unipolar current input (central diode signal input)
D3	17	A	unipolar current input (central diode signal input)
V_{SSA2}	18	S	analog ground 2 for LF front-end
V_{DDA2}	19	S	analog supply voltage 2 for LF front-end (3.3 V)
D4	20	A	unipolar current input (central diode signal input)
S1	21	A	unipolar current input (satellite diode signal input)
S2	22	A	unipolar current input (satellite diode signal input)
I_{refT}	23	A	current reference, for input range of LF front-end ADCs
FTC_H	24	A	fast track counter comparator (+) input
FTC_L	25	A	fast track counter comparator (–) input
SELPLL	26	I	enables internal clock multiplier PLL
XTALO	27	A	crystal output
XTALI	28	A	crystal input
V_{SSD1}	29	S	digital ground 1
R_{XD0}	30	B	P3.0
T_{XD0}	31	B	P3.1
INT0	32	B	P3.2 (interrupt 0)
INT1	33	B	P3.3 (interrupt 1)
R_{XD1}	34	B	P3.4
T_{XD1}	35	B	P3.5
$\overline{WR}$	36	B	P3.6; active LOW
$\overline{RD}$	37	B	P3.7; active LOW
V_{SSD2}	38	S	digital ground 2
$V_{DDD1(core)}$	39	S	digital supply voltage 1 for the core (3.3 V)
A8	40	B	P2.0 (address or I/O)

SYMBOL	PIN	TYPE[1]	DESCRIPTION
A9	41	B	P2.1 (address or I/O)
A10	42	B	P2.2 (address or I/O)
A11	43	B	P2.3 (address or I/O)
A12	44	B	P2.4 (address or I/O)
A13	45	B	P2.5 (address or I/O)
A14	46	B	P2.6 (address or I/O)
A15	47	B	P2.7 (address or I/O)
$\overline{PSEN}$	48	B	program store enable (pull-up; active LOW)
ALE	49	B	address latch enable (pull-up)
$\overline{EA}$	50	B	external ROM select (active LOW); enhanced hooks
V_{SSD3}	51	S	digital ground 3
$V_{DDD1(pads)}$	52	S	digital supply voltage 1 for the pads (5 V); pins 26 to 60
AD0	53	B	P0.0 (data, address or I/O)
AD1	54	B	P0.1 (data, address or I/O)
AD2	55	B	P0.2 (data, address or I/O)
AD3	56	B	P0.3 (data, address or I/O)
AD4	57	B	P0.4 (data, address or I/O)
AD5	58	B	P0.5 (data, address or I/O)
AD6	59	B	P0.6 (data, address or I/O)
AD7	60	B	P0.7 (data, address or I/O)
V_{SSD4}	61	S	digital ground 4
DACCLK	62	T	BCC-DAC clock output
V_{SSD5}	63	S	digital ground 5
$V_{DDD2(pads)}$	64	S	digital supply voltage 2 (level shifter) for the pads (5 V)
VALID	65	T	data validity flag; C2 error flag; (3-state)
DAC	66	T	serial audio data output to DAC (3-state)
DATA	67	T	serial data output to block decoder (3-state)
WCLK	68	T	word clock output (3-state)
SCLK	69	T	serial bit clock output (3-state)
V_{SSD6}	70	S	digital ground 6
SUBQW	71	O	subcode output; Q to W subcode bits
MOTOS	72	T	motor output, sign
MOTOV	73	T	motor output, value
$\overline{DSDEN}$	74	O	DSD enable output (active LOW)
CLO	75	O	clock output
V_{SSD7}	76	S	digital ground 7
$V_{DDD3(pads)}$	77	S	digital supply voltage 3 for the pads (5 V); pins 1 to 6 and 65 to 100
RA	78	T	radial actuator output
FO	79	T	focus actuator output
SL	80	T	sledge control output
V_{SSD8}	81	S	digital ground 8

SYMBOL	PIN	TYPE[1]	DESCRIPTION
RP	82	OD	radial polarity signal (open drain)
TL	83	OD	track loss signal (open drain)
FOK	84	OD	focus OK signal or decoder measurement signal (open drain)
CFLG	85	OD	correction flag output (open drain)
C2FAIL	86	OD	indication of correction failure (open drain)
V_{SSD9}	87	S	digital ground 9
$V_{DDD2(core)}$	88	S	digital supply voltage 2 for the core (3.3 V)
DOBM	89	T	EBU bi-phase mark output (externally buffered) (3-state)
OTD	90	O	off-track detect
FB	91	OD	FIFO boundary, motor overflow (open drain)
SBSY	92	T	subcode block sync (3-state)
SFSY	93	T	subcode frame sync (3-state)
RCK	94	I	subcode clock input
SUB	95	T	P to W subcode bits (3-state)
DEEM	96	O	deemphasis active output
KILL	97	OD	kill output (open drain)
DEFI	98	I	defect detector input
DEFO	99	O	defect detector output
LDON	100	OD	laser drive on output (open drain)

Note

1. Pin type abbreviations: O = Output, I = Input, S = power Supply, A = Analog function, OD = Open Drain, B = Bidirectional, T = 3-state output. All supply pins must be connected directly to their respective external power supply voltages.

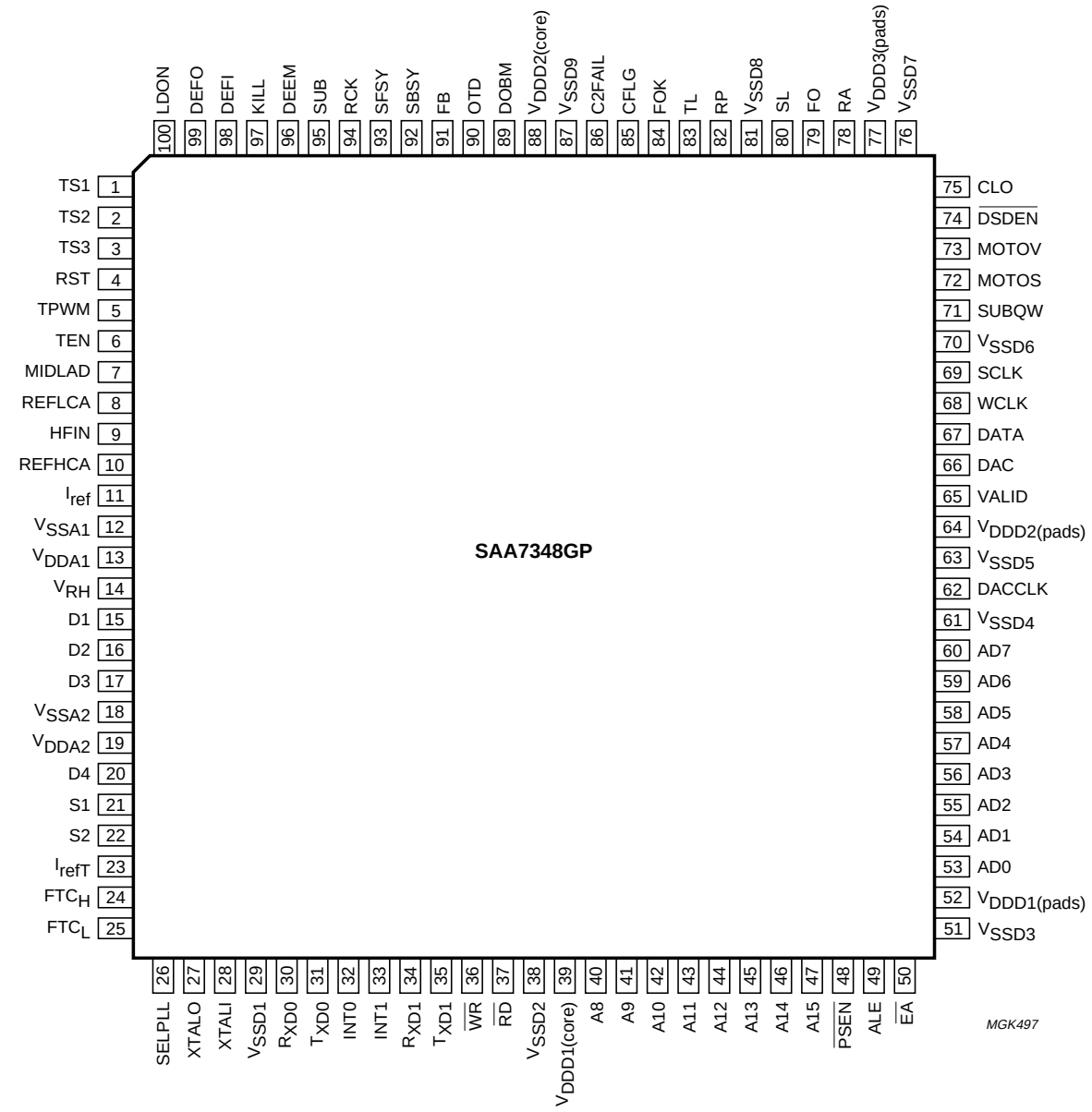


Fig.2 Pin configuration.

7 FUNCTIONAL DESCRIPTION

The ACE combines the functionality of a DSICS (OQ8868), a CD65 (LO9585) and an 80C51-based microcontroller (83C654). In addition, a large part of the glue logic has been integrated to help minimize the number of external components required in CD-ROM applications.

7.1 Analog front-end

The front-end circuit can be split into two parts:

1. The decoder input (HF front-end)
2. The servo input (LF front-end).

Each is powered by a separate power supply pin pair.

7.1.1 DECODER FRONT-END

The EFM signal is fed to the decoder through an ADC, which is preceded by an AGC stage. In order to make full use of the digital front-end resolution, the gain control amplifier should deliver a constant 1.4 V p-p output signal. The gain range of the AGC is 16 dB and is controlled in steps of 1.0 dB. The gain of the variable gain amplifier is controlled by an on-chip digital gain control block. This block allows for both automatic and microcontroller gain control.

The internal HF detector is sensitive to any disturbance on the HF signal; a clean (good signal-to-noise ratio) EFM signal is necessary since high frequency components can disturb the HF detector. The input range of the HF front-end varies from 2.3 V p-p down to 0.35 V p-p. If in the lower range the signal level is between 25% and 75% of the ADC range, the HF detector will signal NO HF (In this range an ADC LSB translates into 5.5 mV, so half the range equals 175 mV. If the total offset was equal to 6 LSBs, the signal range would be reduced by 2×33 mV. In this case a signal of less than 109 mV would signal NO HF). To ensure the AGC offset is minimized when the AGC gain is high, it is necessary to connect a resistor divider to MIDLAD, as shown in Fig.3.

The SAA7348 contains an on-chip digital equalizer and data slicer. The equalizer is adaptive; actual equalization depends on the disc speed. The data slicer has a microcontroller programmable bandwidth. A fully digital internal PLL is used to regenerate the bit clock. The bandwidth and equalization of the PLL can be programmed by the microcontroller. An off-track input is necessary for certain applications. If the off-track input flag is HIGH, the SAA7348 will assume that the servo is following on the wrong track, and will flag all incoming HF data as incorrect. The off-track input is connected internally to the servo section.

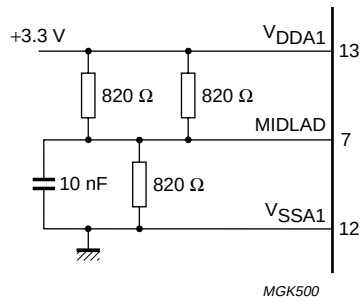


Fig.3 Front-end offset compensation.

7.1.2 SERVO FRONT END

The servo front end contains six current-input ADCs (four for focus and two for the radial signals). The ADCs do not require external capacitors, unlike the OQ8868 or CD7 (SAA7370). For high performance radial access, a comparator input is available for the FTC (Fast Track Count) signal.

The dynamic range of the ADC input currents can be adjusted over a range dependent on the value of an external resistor connected to I_{refT}. The maximum input current for the central and satellite diodes, respectively, is given below:

$$I_{i(central)(max)} = \frac{2.4 \times 10^6}{R_{IrefT}} (\mu A)$$

$$I_{i(satellite)(max)} = \frac{1.2 \times 10^6}{R_{IrefT}} (\mu A)$$

V_{RH} is generated internally. The value of V_{RH} is dependent upon the spread of internal capacitors and on the value of the reference current generated by the external resistor on I_{refT}. Typical input currents for a range of resistance values are given in Table 1.

Table 1 Typical input currents for a range of values of R_{IrefT}

R_{IrefT} (kΩ)	TYPICAL CURRENT INPUT RANGE					
	f_{sys}[1] = 4.2336 MHz			f_{sys}[1] = 8.4672 MHz		
	D1, D2, D3, D4 (μA)	S1, S2 (μA)	V_{RH} (V)	D1, D2, D3, D4 (μA)	S1, S2 (μA)	V_{RH} (V)
200	12.000	6.000	1.891	12.000	6.000	0.946
220	10.909	5.455	1.719	10.909	5.455	0.860
240	10.000	5.000	1.576	10.000	5.000	0.788
270	8.889	4.444	1.396	8.889	4.444	0.698
300	8.000	4.000	1.261	8.000	4.000	0.631
330	7.273	3.636	1.146	7.273	3.636	0.573
360	6.667	3.333	1.051	6.667	3.333	0.526
390	6.154	3.077	0.970	6.350	3.175	0.500
430	5.581	2.791	0.880	–	–	–
470	5.106	2.553	0.805	–	–	–
510	4.706	2.353	0.742	–	–	–
560	4.286	2.143	0.675	–	–	–
620	3.871	1.935	0.610	–	–	–
680	3.529	1.765	0.556	–	–	–
750	3.200	1.600	0.504	–	–	–

Note

1. f_{sys} is always equal to $\frac{\text{servo clock}}{2}$; see Table 9.

The preset latch command can be used to select this method of V_{RH} automatic adjustment.

Alternatively, the dynamic range of the input currents can be made dependent on the ADC reference voltage, V_{RH}. In this case, the maximum input current for the central and satellite diodes, respectively, is:

$$I_{i(central)(max)} = f_{sys} \times V_{RH} \times 1.10 \times 10^{-6} (\mu A)$$

$$I_{i(satellite)(max)} = f_{sys} \times V_{RH} \times 0.55 \times 10^{-6} (\mu A)$$

where f_{sys} = 4.2336 MHz.

V_{RH} can be set to any one of 32 pre-defined levels, selectable under software control. V_{RH} is initially set to 2.5 V using the preset latch command, then incremented or decremented one level at a time by repeatedly resending the same commend.

7.2 Decoder functions

The SAA7348 is a multi-speed decoding device with an internal phase locked loop clock multiplier. Several playback speeds can be selected, depending on the crystal frequency and the internal clock settings; see Table 2.

The following functions are performed in the decoder block:

- Demodulation (includes sync protection circuit); converts the 14-bit EFM data and subcode words into 8-bit symbols.
- Subcode data processing.
- Error correction; a t = 2, e = 4 type is used on both C1 (32 symbol) and C2 (28 symbol) frames. The error corrector can correct up to 2 errors on the C1 level and up to 4 errors on the C2 level. The error corrector also contains a flag processor. Flags are assigned to symbols when the error corrector cannot ascertain if the symbols are definitely good. C1 generates output flags that are used by C2. The C2 output flags are used by the interpolator to conceal uncorrectable errors for audio output; they are also output via the EBU signal (DOBM) and the VALID output with I^2S for CD-ROM applications.

- Motor control; the spindle motor is controlled by a fully integrated digital servo. Address information from the internal 8 frame FIFO and disc speed information are used to calculate the motor control output signals. Several output modes are supported:
  - Pulse density, 2-line (true complement output), $1 \times n$ MHz sample frequency
  - PWM-output, 2-line, $22.05 \times n$ kHz modulation frequency
  - CDV motor mode
  - Brushless motor control mode.

A simplified illustration of the data flow through the decoder is shown in Fig.4.

Table 2 Decoder playback speeds; note 1

REGISTER B	REGISTER E	INTERNAL FREQUENCY (MHz)			
		67.7376(2)	**50.8032**(2)	**33.8688**(2)(3)	**16.9344**(4)
00XX	0XXX	n = 2	n = 1.5	n = 1	–
00XX	1XXX	n = 8	n = 6	n = 4	n = 2
01XX	0XXX	–	–	–	n = 1
01XX	1XXX	–	–	–	n = 4
10XX	0XXX	n = 4	n = 3	n = 2	–
10XX	1XXX	n = 16	n = 12	n = 8	–
11XX	0XXX	–	–	–	n = 2

Notes

1. X = don’t care.
2. With an 8.4672 MHz crystal, and only if SELPLL = 1 (i.e. clock multiplier enabled; see also Section 8.1.1).
3. Can use external 33.8688 MHz crystal.
4. Can use external 16.9344 MHz crystal.

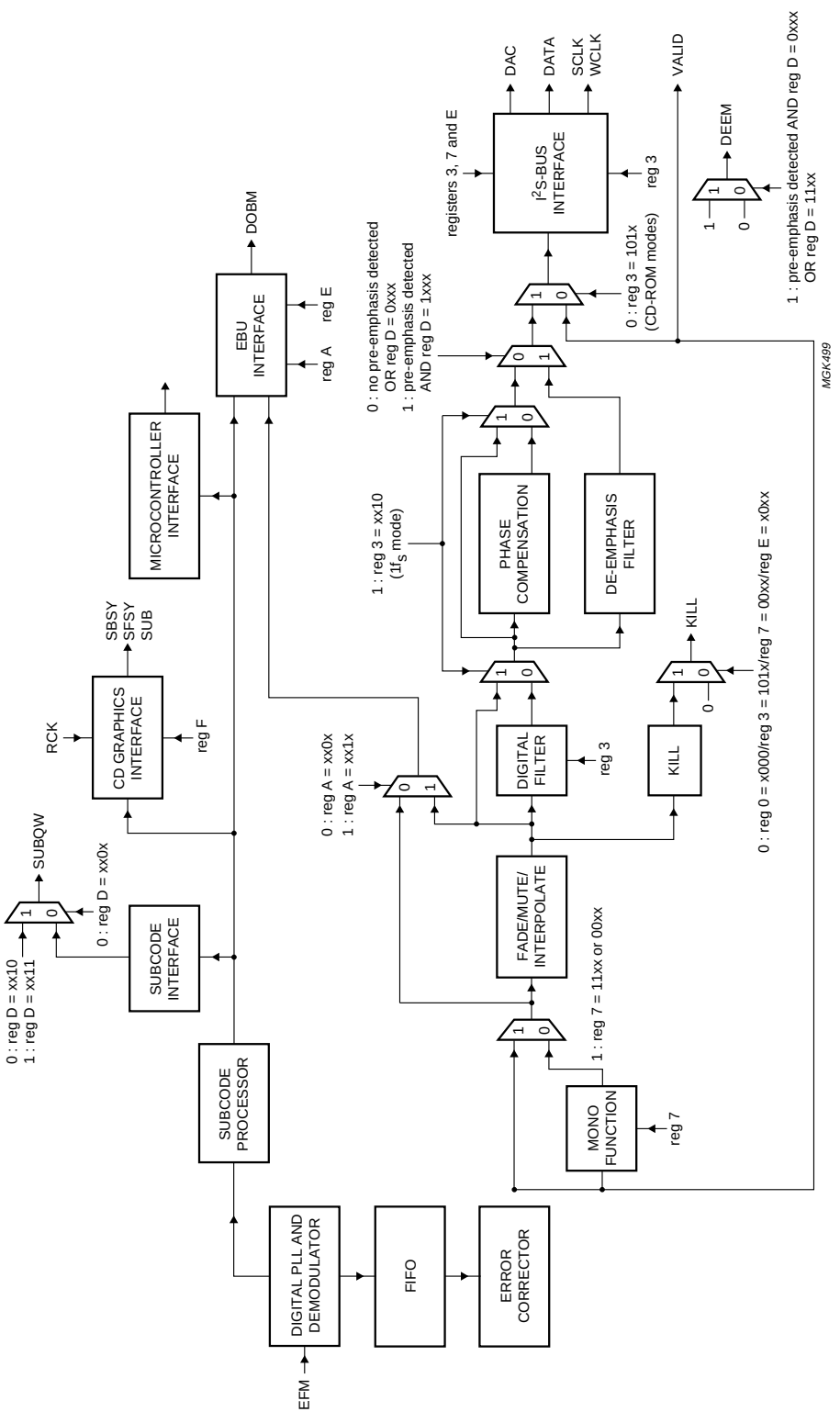


Fig.4 SAA7348 decoder function: simplified data flow.

7.3 Servo functions

7.3.1 SIGNAL CONDITIONING

The digital codes retrieved from the ADCs are applied to logic circuitry to obtain various control signals. The signals from the central aperture diodes are processed to obtain a normalised focus error signal:

$$FE_n = \frac{D1 - D2}{D1 + D2} - \frac{D3 - D4}{D3 + D4}$$

where the detector set-up illustrated in Fig.5 is assumed.

For single Foucault focusing, signal conditioning can be switched under software control such that:

$$FE_n = 2 \times \frac{D1 - D2}{D1 + D2}$$

The error signal, FE_n, is further processed by a Proportional Integral and Differential (PID) filter section.

A Focus OK (FOK) flag is generated by means of the central aperture signal and an adjustable reference level. This signal is used to provide extra protection for Track-Loss (TL) generation, drop out detection and the focus start-up procedure.

The radial or tracking error signal is generated by the satellite detector signals R1 and R2. The radial error signal can be formulated as follows:

$RE_s = (R1 - R2) \times re\_gain + (R1 - R2) \times re\_offset$

where the index ‘s’ indicates the automatic scaling operation performed on the radial error signal. This scaling is necessary to avoid non-optimal dynamic range usage in the digital representation and to reduce the radial bandwidth spread. Furthermore, the radial error signal will be free of offset during disc start-up.

The four signals from the central aperture detectors, together with the satellite detector signals, generate a track position signal (TPI), which can be formulated as follows:

$TPI = sign\ [(D1 + D2 + D3 + D4) - (R1 + R2) \times sum\_gain]$

where the weighting factor sum_gain is generated internally by the SAA7348 during initialization.

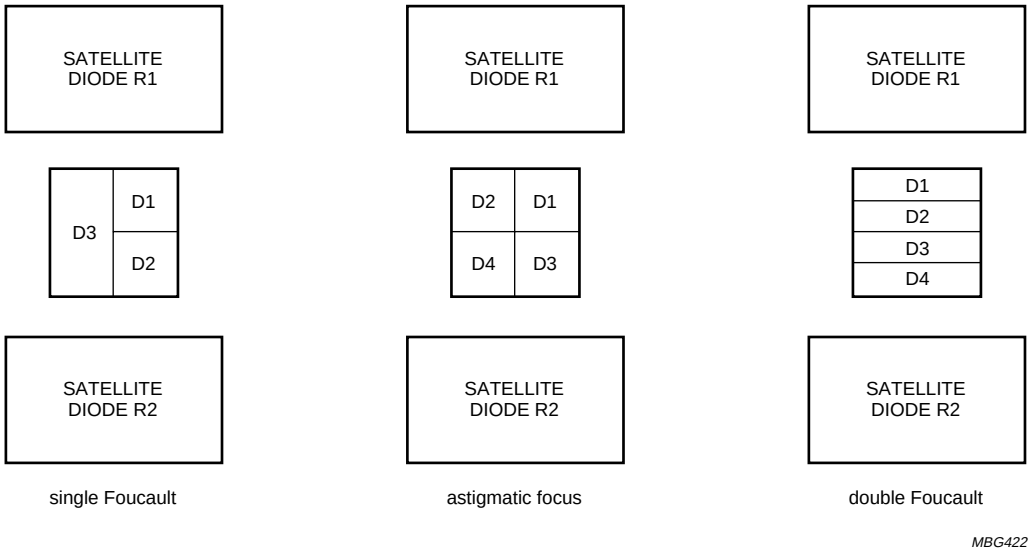


Fig.5 Detector arrangement.

7.3.2 Focus control

The SAA7348 performs the following focus servo function:

- Focus start-up
- Focus position control loop
- Drop-out detection
- Focus loss detection and fast restart
- Focus loop gain switching
- Focus automatic gain control loop.

7.3.3 RADIAL CONTROL

The SAA7348 performs the following radial servo functions:

- Level initialization
- Radial position control loop
- Sledge control
- Tracking control
- Access with or without track loss information
- Radial automatic gain control loop.

7.3.4 OFF-TRACK COUNTING

The track position signal (TPI) is a flag used to indicate whether the radial spot is positioned on the track with a margin of ±0.25 of the track pitch. One of the following three counting states is selected:

- Protected state
- Slow counting state
- Fast counting state.

7.3.5 OFF-TRACK DETECTION

The Off-Track Detection (OTD) signal flags off-track conditions; the polarity of this signal is programmable.

7.3.6 SHOCK DETECTION

A shock detector can be switched on during normal track following. Within an adjustable frequency range, it detects whether disturbances in the radial spot relative to the track exceed a programmable level. Every time the Radial tracking Error (RE) exceeds this level, the radial control bandwidth is switched to twice its original bandwidth and the loop gain is increased by a factor of 4.

7.3.7 DEFECT DETECTION

A defect detection circuit is incorporated into the SAA7348. If a defect is detected, the circuit can hold all radial and focus controls. The defect detector can be switched off, applied only to focus control, or applied to both focus and radial controls under software control. The actions of the circuit can be monitored on the DEFO pin (active HIGH).

An external defect detector can be added by removing the connection between DEFO and DEFI (normal operation) and inserting the necessary circuitry.

7.3.8 DRIVER INTERFACE

The control signals (pins RA, FO and SL) for the mechanism actuators are pulse density modulated. The modulating frequency can be set to either $\frac{\text{servo clock}}{8}$ or $\frac{\text{servo clock}}{4}$ MHz. An analog representation of the output signals can be generated by connecting a first order low-pass filter to the outputs.

During reset (i.e. RST pin held HIGH) the RA, FO and SL pins are high impedance.

7.3.9 LASER INTERFACE

The LDON pin (open-drain output) is used to turn the laser on and off. When the laser is on, the output is high impedance. The action of the LDON pin is controlled by the xtra_preset parameter; the pin is automatically driven if the focus control loop is active.

7.4 Subcode interface

There are two subcode interfaces:

- One which conforms to *"EIAJ CP-2401"* (using SBSY, SFSY, RCK and SUB) and can be configured as either a 3- or 4-wire interface. The interface formats are illustrated in Fig.6.
- An RS232 like format on SUBQW as illustrated in Fig.7.

  The subcode sync word is formed by a pause of $\frac{200}{n}$ µs minimum. Each subcode byte starts with a 1 followed by 7 bits (Q to W). The gap between bytes can vary between $\frac{11.3}{n}$ and $\frac{90}{n}$ µs. Note that SUBQW is not valid in lock-to-disc mode (includes QLLV).

The subcode data is also available at the EBU output (DOBM).

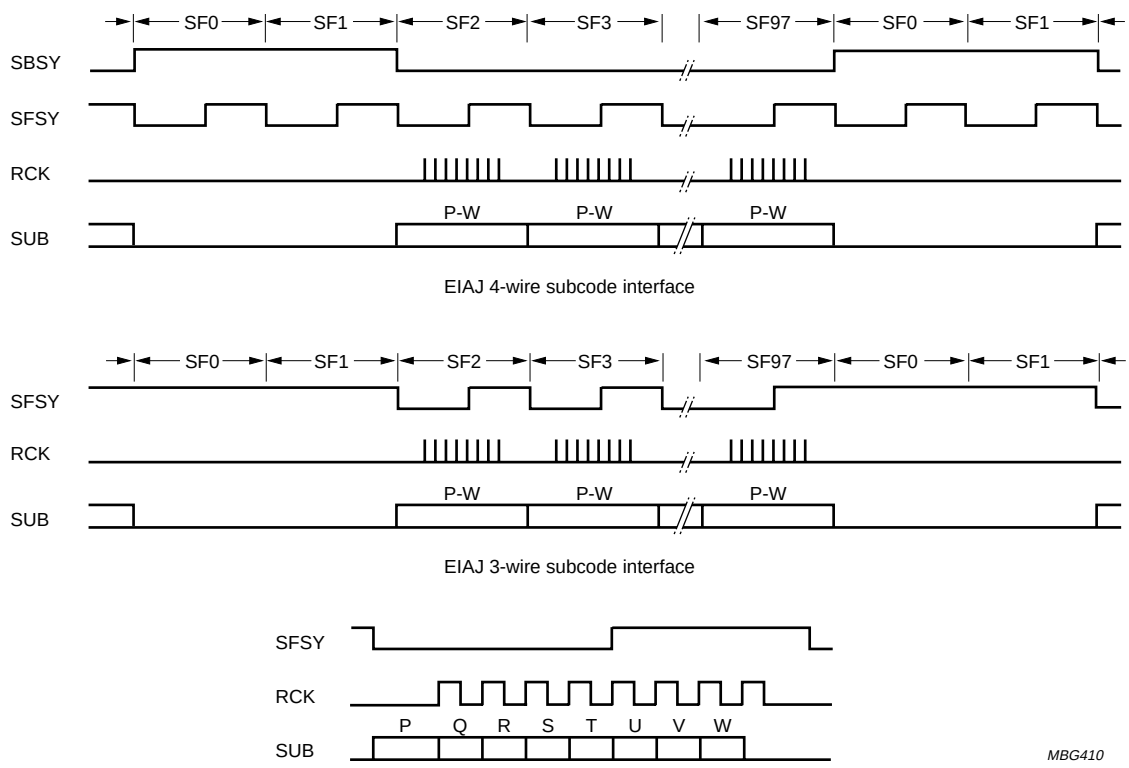
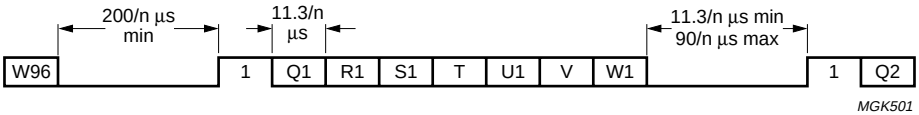


Fig.6 EIAJ subcode (CD graphics) interface format.



(1) n = disc speed.

Fig.7 Subcode format and timing on SUBQW pin.

7.5 Digital output

The AES/EBU signal on pin DOBM is in accordance with the format defined in *"IEC 958"*. This signal is only available in the decoder's CLV modes if audio features are enabled (not in QCLV modes). Three different modes can be selected:

- DOBM pin held LOW
- Data taken before concealment, mute and fade (must always be used for CD-ROM modes)
- Data taken after concealment, mute and fade (can only be used for audio modes).

7.5.1 FORMAT

The digital audio output consists of 32-bit words ('subframes') transmitted in bi-phasemark code (two transitions for a logic 1 and one transition for a logic 0). Words are transmitted in blocks of 384.

Table 3 32-bit digital audio output format

FUNCTION	BITS	DESCRIPTION
Sync	0 to 3	note 1
Auxiliary	4 to 7	not used; normally zero
Error flags	4	CFLG error and interpolation flags when selected by register A
Audio sample[2]	8 to 27	first 4 bits not used (always zero); two's complement; LSB = bit 12, MSB = bit 27
Validity flag[3]	28	valid = logic 0
User data[4]	29	used for subcode data (Q to W)
Channel status[5]	30	control bits and category code
Parity bit	31	even parity for bits 4 to 30

Notes

1. The sync word is formed in violation of the bi-phase rule and, therefore, does not contain any data. Its length is equivalent to 4 data bits. The 3 different sync patterns indicate the following situations:
   a) Sync B: word contains left sample (start of a block, 384 words).
   b) Sync M: word contains left sample (no block start).
   c) Sync W: word contains right sample.
2. Left and right samples are transmitted alternately.
3. Audio samples are flagged (bit 28 = 1) if an error was detected but could not be corrected. This flag remains the same even if data is taken after concealment.
4. Subcode bits Q to W from the subcode section are transmitted via the user data bit. This data is asynchronous with the block rate.
5. The channel status bit is the same for both left and right words. Therefore, a block of 384 words contains 192 channel status bits. The category code is always CD. The bit assignment is shown in Table 4.

Table 4 Channel status bit assignment

FUNCTION	BIT	DESCRIPTION
Control	0 to 3	copy of CRC checked Q-channel control bits 0 to 3; bit 2 is logic 1 when copy permitted; bit 3 is logic 1 when recording has pre-emphasis
Reserved mode	4 to 7	always zero
Category code	8 to 15	CD: bit 8 = logic 1, all other bits = logic 0
Clock accuracy	28 and 29	set by register A: 10 = class 1 crystal (<50 ppm) 00 = class 2 crystal (<1000 ppm) 01 = class 3 crystal (>1000 ppm)
Remaining	16 to 27 and 30 to 191	always zero

7.6 S2B interface

This interface is in accordance with the *"S2B Interface Description"*. It's a serial interface with a high level command set for controlling a CD-ROM engine.

7.7 Audio support

Audio support consists of several parts:

- Serial data interface.
- Deemphasis control (DEEM). This signal is HIGH if the subcode info of a track defines it to be recorded with deemphasis.
- Kill control (KILL). This signal tests for digital silence in the right and left channel before the digital filter. The output is switched active LOW if silence has been detected for at least 250 ms, if mute is active, or in CD-ROM modes.
- Output clock for BCC-DAC applications (DACCLK).
- Oversampled output. The SAA7348 contains a 2 to 4 times oversampling IIR (Infinite Impulse-Response) filter, and a selectable deemphasis filter (if the de-emphasis signal is selected to come out of DEEM then the filter is bypassed; see Table 31).
- Concealment, mute, attenuation and fade. In audio modes a 1-sample linear interpolator becomes active if a single sample is flagged as erroneous; left and right channels have independent interpolators. A digital level converter performs the following functions:
  - soft mute (signal reduced to 0 in a maximum of 128 steps)
  - full-scale (signal ramped back to 0 dB level)
  - attenuation (signal scaled by –12 dB)
  - fade (activates a 128 stage counter which allows the signal to be scaled up or down in 0.07 dB steps)
  - peak detector (measures highest audio level; absolute level for left and right channels; the 8 MSBs of each are output in the Q-channel data).
- Mono output selection. Either channel can be selected to be output over both left and right channels.

7.7.1 Serial audio data interface

The serial data interface can be switched between two modes: Philips I^2S and the EIAJ format.
In each case, the serial data is transferred through a 3-wire interface. The I^2S signal contains three components: WCLK (word select), SCLK (serial clock) and DAC (serial data). The polarity of WCLK and of the data can be inverted.

The oversampling frequency and format are selected as shown in Table 5. The serial data output is separate from the CD-ROM output. In CD-ROM mode the DAC serial data output pin will be muted.

Table 5 Oversampling frequency select

MODE	NUMBER OF BITS	SAMPLE FREQUENCY
I^2S	18	$4f_s$
	18	$2f_s$
	16	f_s
EIAJ	18	$4f_s$
	18	$2f_s$
	18	f_s
	16	$4f_s$
	16	$2f_s$
	16	f_s

7.8 CD-ROM support

The principle difference between the ACE and its predecessors with regard to CD-ROM support is the provision of a separate serial data pin, which removes the need for external components. The format can be I^2S or EIAJ.

7.8.1 SERIAL CD-ROM DATA INTERFACE

The serial data signal contains three components: WCLK (word select), SCLK (serial clock) and DATA (serial data). The polarity of WCLK and of the data can be inverted. WCLK and SCLK are common with the audio serial data output. The VALID signal is used to flag errors in either the LSB or MSB of the 16-bit data word.

7.9 Reset

The RST pin on the SAA7348 is an active HIGH Schmitt trigger. For a valid reset, the signal should be HIGH for a period of 12 XTALI clock cycles, during which time the power supply must be within specification on all power supply pins. To ensure that the SAA7348 resets fully it is necessary to do one of the following:

- Connect SELPLL to $\overline{\text{DSDEN}}$ (rather than V_{DD}). This allows the internal clock multiplier to start immediately after reset. Note that the internal clocks are not guaranteed to operate at the correct frequencies for the first 200 μs after reset. Note also that the operating speed of the microcontroller is reduced in Idle mode (and that baud rates change with the processor clock).
- Connect SELPLL to an inverted reset signal.
  The internal clock multiplier starts after reset, but during Idle mode the microcontroller speed is normal.

7.10 External ROM support

Since the ACE incorporates an 80C51 core it can, like any microcontroller, run a program from external ROM.
The $\overline{\text{EA}}$ pin should be tied to V_{SS} in this case. For security reasons, this pin is only sampled during reset, so a program cannot be run partly from external ROM. Signal relationships for external program execution are shown in Fig.8. Timing specification can be found in Table 6.

Table 6 Timing specifications for external program memory search

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{LHLL}	ALE pulse width	60	–	ns
t_{AVLL}	address valid to ALE LOW	15	–	ns
t_{LLAX}	address hold after ALE LOW	21	–	ns
t_{LLPL}	ALE LOW to $\overline{PSEN}$ LOW	25	–	ns
t_{PLPH}	$\overline{PSEN}$ pulse width	80	–	ns
t_{PLIV}	$\overline{PSEN}$ LOW to valid instruction in	–	65	ns
t_{PXIX}	input instruction hold after $\overline{PSEN}$	0	–	ns
t_{PXIZ}	input instruction float after $\overline{PSEN}$	–	30	ns
t_{AVIV}	address to valid instruction in	–	130	ns
t_{PLAZ}	$\overline{PSEN}$ LOW to address float	–	6	ns
t_{RLRH}	read pulse width	170	–	ns
t_{WLWH}	write pulse width	170	–	ns
t_{RLDV}	$\overline{RD}$ LOW to valid data in	–	135	ns
t_{RHDX}	data hold after $\overline{RD}$	–	50	ns
t_{RHDZ}	data float after $\overline{RD}$	0	–	ns
t_{LLDV}	ALE LOW to valid data in	–	235	ns
t_{AVDV}	address to valid data in	–	260	ns
t_{LLWL}	ALE LOW to $\overline{RD}$ or $\overline{WR}$ LOW	80	115	ns
t_{AVWL}	address valid to $\overline{RD}$ or $\overline{WR}$ LOW	115	–	ns
t_{QVWX}	data valid to $\overline{WR}$ transition	20	–	ns
t_{WHQX}	data hold to $\overline{WR}$	20	–	ns
t_{RLAZ}	$\overline{RD}$ LOW to address float	–	0	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ HIGH to ALE HIGH	20	40	ns

In addition to external program memory, external RAM and I/O can be accessed. Timing relationships for an external data read are shown in Fig.9, and for an external data write in Fig.10.

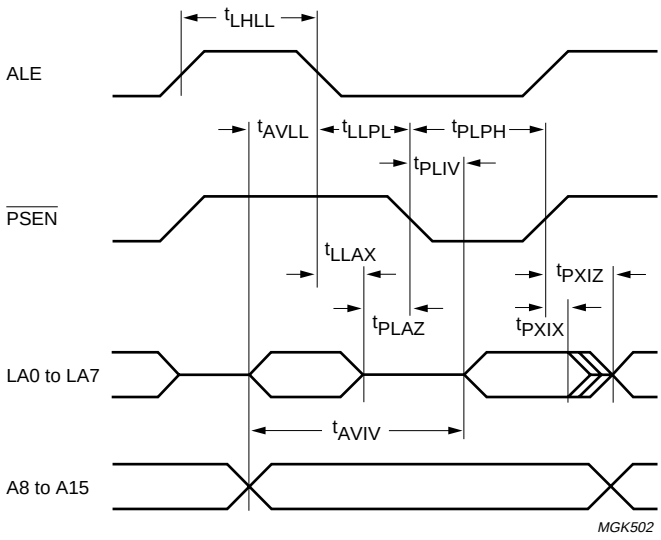


Fig.8 Timing for an external program memory fetch.

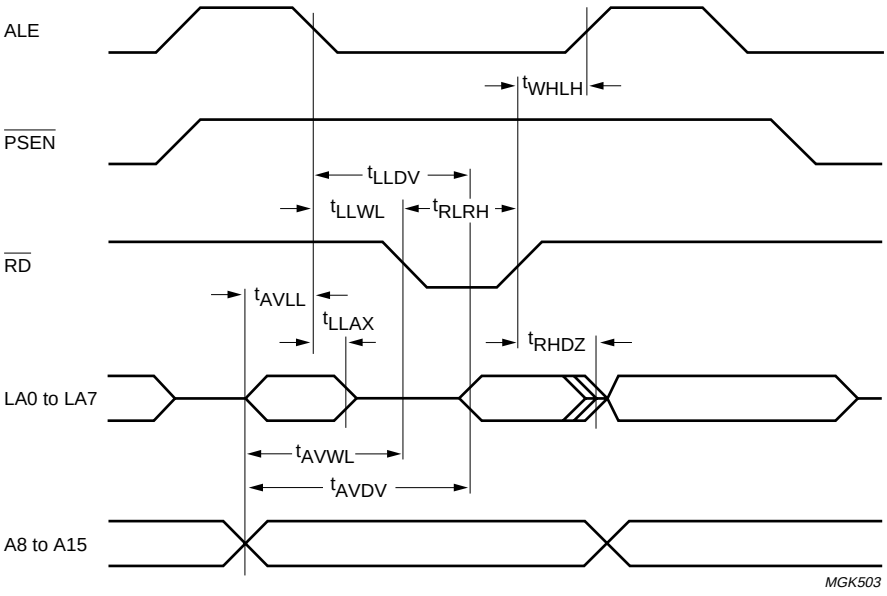


Fig.9 Timing for an external data read.

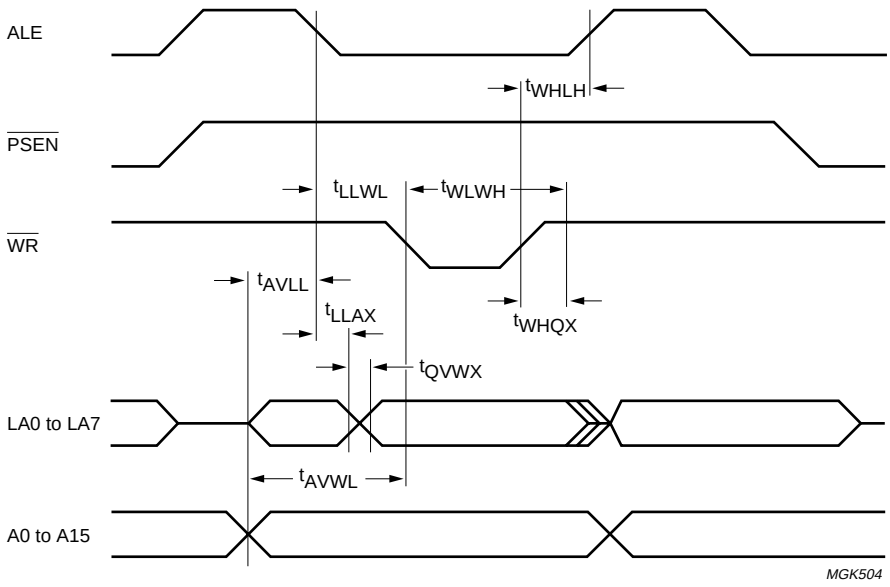


Fig.10 Timing for an external data write.

8 MICROCONTROLLER INTERFACE

This section describes the microcontroller application registers, the memory map, the decoder registers and the servo commands.

8.1 Microcontroller applications registers

8.1.1 CLK GENERATE REGISTER (CLKgen)

The CLK generate register is used to select clock multiplier PLL frequencies and dividers and to switch the servo clock between single and double frequency. The register is byte addressable; R/W.

The on-chip clock multiplier (programmable: 4×, 6× or 8×) allows an external 8.4672 MHz crystal to be used. This generates a single internal master clock from which all other clock signals are derived.

Note that both the microcontroller and the servo are designed for a 50% duty factor input clock.

For a 16× decoder speed, the internal master clock must be 67.7376 MHz (i.e. clock multiplier set to 8×).
The 16.9344 MHz signal can be generated by setting the clock divider to 4, resulting in a standard 50% duty factor clock. For a 12× decoder speed, the internal master clock must be 50.8032 MHz (i.e. clock multiplier set to 6×).
A divide factor of 3 will generate the 16.9344 MHz signal, resulting in a 66% duty factor clock.

The clock divider values set by means of the CLKgen register are shown in Table 9.

Table 7 CLK generate register (address 0X9EH)

7	6	5	4	3	2	1	0
CLKgen.7	CLKgen.6	CLKgen.5	clock_servohi	clock_seldiv2	clock_seldiv1	clock_selpll2	clock_selpll1

Table 8 Description of CLKgen bits

BIT	SYMBOL	DESCRIPTION
7	CLKgen.7	not used
6	CLKgen.6	
5	CLKgen.5	
4	clock_servohi	selects single or 2 × servo clock
3	clock_seldiv2	these bits select the clock divider for the 80C51 core and servo; see Table 9
2	clock_seldiv1	
1	clock_selpll2	these bits select the clock multiplier frequency; see Table 9
0	clock_selpll1	

Table 9 Divider selection

MASTER CLOCK (MHz)	µP CLOCK (MHz)	REGISTER CLKgen BIT					SERVO CLOCK (MHz)	DIVIDE FACTOR	OVER-SPEED SERVO (%)
		0	1	2	3	4			
33.8688	16.9344	0	0	0	0	0	8.4672	4	100
						1	16.9344	2	200
50.8032	16.9344	0	1	0	1	0	8.4672	6	100
						1	16.9344	3	200
67.7376	16.9344	1[1]	0[1]	1	0	0	8.4672	8	100
						1	16.9344	4	200
33.8688	16.9344	1[1]	1[1]	1	0	0	8.4672	4	100
						1	16.9344	2	200

Note

1. The internal clock multiplier PLL operates at the same frequency for both these options.

8.1.2 PORT SERVO REGISTER (PSR)

The Port Servo Register is the internal bus used to communicate with the servo. The register is bit addressable; R/W. The operation of the handshake bits used for serial communications with the servo is outlined in Table 12.

Table 10 Port servo register (address 0XD8H to 0XDFH)

7	6	5	4	3	2	1	0
Tray_en	Tray_pwm	Srv_rdy	Srv_dacc	Srv_sild	Srv_sicl	Srv_sida	Srv_intreqn

Table 11 Description of PSR bits

BIT	SYMBOL	ADDRESS	DESCRIPTION
7	Tray_en	0XDFH	signal to enable tray driver
6	Tray_pwm	0XDEH	PWM signal to tray driver
5	Srv_rdy	0XDDH	RDY; see Table 12
4	Srv_dacc	0XDCH	DAC; see Table 12
3	Srv_sild	0XDBH	SILD
2	Srv_sicl	0XDAH	SICL
1	Srv_sida	0XD9H	SIDA
0	Srv_intreqn	0XD8H	INTREQN

Table 12 Servo serial communication handshake signals

DAC	RDY	DESCRIPTION
0	0	transmit register full; the microcontroller can read a byte or send a new command
0	1	idle state, transmit register empty; the microcontroller can transmit a parameter relating to the new command
1	0	received one byte, waiting for EOT
1	1	receive register full

8.1.3 SERVO CONTROL REGISTER (SCR)

The Servo Control Register is used for reading and writing internal control signals. The register is byte addressable; R/W.

Table 13 Servo control register (address 0XD9H)

7	6	5	4	3	2	1	0
Srv_frc_flock	Srv_frc_lock	Srv_otd	Srv_da	Srv_cl	Srv_rab	Srv_startup	Serv_halt

Table 14 Description of SCR bits

BIT	SYMBOL	DESCRIPTION
7	Srv_frc_flock	force_flock: coarse PLL lock indicator control; a HIGH indicates ±6% of disc speed
6	Srv_frc_lock	force_lock; a HIGH indicates frequency lock
5	Srv_otd	OTD controller: off-track signal generated by the controller input for the OTD multiplexer; a HIGH indicates laser is off track
4	Srv_da	DA (used only with direct decoder communication)
3	Srv_cl	CL (used only with direct decoder communication)
2	Srv_rab	RAB (used only with direct decoder communication)
1	Srv_startup	16 kHz pulse (start new servo processor execution sequence); pulse is latched; latch is cleared by a write operation
0	Serv_halt	servo halt; halts servo processor execution

8.1.4 SERVO STATUS REGISTER (STR)

The Servo Status Register holds high level status information on the servo system. The information is latched into a register and cleared whenever the register is read. This information could be a trigger to initiate a recovery. The register is byte addressable; read only.

Table 15 Servo status register (address 0XE9H)

7	6	5	4	3	2	1	0
Srv_tl1	Srv_tl0	Srv_shock	Srv_hf_present	Srv_FIFO_ov	Srv_fock	Srv_otd_inp	Srv_subc

Table 16 Description of STR bits

BIT	SYMBOL	DESCRIPTION
7	Srv_tl1	internal servo signal; see Table 17
6	Srv_tl0	internal servo signal; see Table 17
5	Srv_shock	shock: decoder status signal; $\overline{\text{Motstart2}}$ + $\overline{\text{PLL\_phase\_lock}}$ + Motor-ov + FOCOK + OTD
4	Srv_hf_present	HF_present: internal decoder signal; indicates if laser spot is in a recorded area
3	Srv_FIFO_ov	FIFO_OV: decoder status signal; FIFO overflow occurred
2	Srv_fock	FOCOK: servo output signal; focus OK/$\overline{\text{OK}}$
1	Srv_otd_inp	OTD: servo output signal; laser spot on/off track
0	Srv_subc	subcode found: decoder status signal; subcode present in servo buffer

The Srv_tl0 and Srv_tl1 signals can be used to determine in which direction the servo is counting during a jump execution.

Table 17 Servo jump modes

Srv_tl1	Srv_tl0	DESCRIPTION
0	0	protected mode
0	1	fast jump_1
1	0	slow jump
1	1	fast jump_2

8.1.5 MOTOR OUTPUT QCLV REGISTER (MOQ; address 0XF2H and 0XF3H)

The Motor Output QCLV register holds the sixteen bits of the filtered (–3 dB, 300 Hz) motor error signal. This signal is updated at a frequency of 16.537 kHz. Address 0XF3H holds the eight most significant bits, address 0XF2H the eight least significant bits. Refreshing rule: if the low byte is read, the high byte is locked to avoid mixing up two successive samples. If the high byte has been read, the low byte will be refreshed. The register is byte addressable; read only.

8.1.6 P3 REGISTER

The P3 register is used in the same way as in the standard 80C51. It contains a second UART, however, whose input and output pins are R_{XD1} and T_{XD1} respectively. Direction control is by DDROUT3 (SFR address 0XFD; see Table 25 and Section 8.1.12). The register is bit addressable; R/W.

Table 18 P3 register (address 0XB0H to 0XB7H)

7	6	5	4	3	2	1	0
WRN	RDN	TXD1	RXD1	INT1	INT0	TXD0	RXD0

Table 19 Description of P3 register bits

BIT	SYMBOL	ADDRESS	DESCRIPTION
7	WRN	0XB7H	WRN
6	RDN	0XB6H	WDN
5	TXD1	0XB5H	TXD1: serial buffer 1; transmit
4	RXD1	0XB4H	RXD1: serial buffer 1; receive
3	INT1	0XB3H	INT1: external Interrupt 1
2	INT0	0XB2H	INT0: external Interrupt 0
1	TXD0	0XB1H	TXD0: serial buffer 0; transmit
0	RXD0	0XB0H	RXD0: serial buffer 0; receive

8.1.7 Decoder Status Register (DSR)

The decoder status register provides decoder status information. The register is byte addressable; read only.

Table 20 Decoder status register (address 0XEBH)

7	6	5	4	3	2	1	0
Decoder_stat.7	TX_full	Dec_motov	Dec_pll_flock	Dec_pll_lock	Dec_motstop	Dec_motstart_2	Dec_motstart_1

Table 21 Description of DSR bits

BIT	SYMBOL	DESCRIPTION
7	Decoder_stat.7	–
6	TX_full	communication buffer to decoder is full
5	Dec_motov	motor-overflow: decoder status signal; motor output saturates
4	Dec_pll_flock	PLL_flock: decoder internal signal; can be forced by μP
3	Dec_pll_lock	PLL_lock: decoder internal signal; can be forced by μP
2	Dec_motstop	motstop: decoder status signal; speed <12%
1	Dec_motstart_2	motstart 2: decoder status signal; speed >50%
0	Dec_motstart_1	motstart 1: decoder status signal; speed >75%

8.1.8 MOTOR SETPOINT REGISTER (MSR; address 0XF9H)

The motor setpoint register is used to set the speed of the motor in Quasi CLV mode. QCLV motor control is switched off by making the setpoint equal 00100000. See Table 22 for setpoint/speed values. Note that these are measured values. They were measured using the motor control bread board. This bread board was hooked onto a ROM 65000 loader 12.66 application. The filter in the config control (Cnf_filter) was switched off. A motor gain of 5 was used. The register is byte addressable; R/W.

Table 22 Speed measurements

SFR SETPOINT	MEASURED SPEED
00100000	1.8
00100010	1.9
00100011	2.0
00100101	2.1
00100111	2.2
00101000	2.3
00101010	2.4
00101100	2.5
00101101	2.6
00101111	2.7
00110000	2.8
00110010	2.9
00110011	3.0
00110101	3.1
00110111	3.2
00111000	3.3
00101010	3.4
00111100	3.5
00111110	3.6
00111111	3.7
01000000	3.8
01000010	3.9
01000011	4.0
01000101	4.1
01000111	4.2
01001001	4.3
01001011	4.4
01001100	4.5
01001110	4.6
01001111	4.7
01010001	4.8
01010010	4.9

SFR SETPOINT	MEASURED SPEED
01010100	5.0
01010110	5.1
01010111	5.2
01011001	5.3
01011011	5.4
01011100	5.5
01011110	5.6
01011111	5.7
01100001	5.8
01100010	5.9
01100100	6.0
01100110	6.1
01100111	6.2
01101001	6.3
01101011	6.4
01101100	6.5
01101110	6.6
01101111	6.7
01110001	6.8
01110010	6.9
01110100	7.0
01110110	7.1
01110111	7.2
01111001	7.3
01111011	7.4
01111100	7.5
01111110	7.6
10000000	7.7
01111111	7.7
10000001	7.8
10000011	7.9
10000100	8.0

8.1.9 MOTOR GAIN QCLV REGISTER (address 0XFAH)

The motor_gain_QCLV register is used to set the gain of the motor control signal. It can be used in quasi as well as in CLV mode. Only the 6 least significant bits are used (see Table 23 for values). The actual gain depends on the filter in the config register (Cnf_filter). If the filtering is switched on, the gain is reduced by a factor of 8. The register is byte addressable; R/W.

Table 23 Loop gain

SFR SETTING	GAIN	
	FILTER ON	FILTER OFF
00000000	1	0.125
00111111	2	0.25
00111110	3	0.375
00111101	4	0.5
00111100	5	0.625
00111011	6	0.75
00111010	7	0.875
00111001	8	1
00111000	9	1.125
00110111	10	1.25
00110110	11	1.375
00110101	12	1.5
00110100	13	1.625
00110011	14	1.75
00110010	15	1.875
00110001	16	2
00110000	17	2.125
00101111	18	2.25
00101110	19	2.375
00101101	20	2.5
00101100	21	2.625
00101011	22	2.75
00101010	23	2.875
00101001	24	3
00101000	25	3.125
00100111	26	3.25
00100110	27	3.375
00100101	28	3.5
00100100	29	3.625
00100011	30	3.75
00100010	31	3.875
00100001	32	4

SFR SETTING	GAIN	
	FILTER ON	FILTER OFF
00100000	33	4.125
00011111	34	4.25
00011110	35	4.375
00011101	36	4.5
00011100	37	4.625
00011011	38	4.75
00011010	39	4.875
00011001	40	5
00011000	41	5.125
00010111	42	5.25
00010110	43	5.375
00010101	44	5.5
00010100	45	5.625
00010011	46	5.75
00010010	47	5.875
00010001	48	6
00010000	49	6.125
00001111	50	6.25
00001110	51	6.375
00001101	52	6.5
00001100	53	6.625
00001011	54	6.75
00001010	55	6.875
00001001	56	7
00001000	57	7.125
00000111	58	7.25
00000110	59	7.375
00000101	60	7.5
00000100	61	7.625
00000011	62	7.75
00000010	63	7.875

8.1.10 Data Direction Registers (DDR0, DDR2 and DDR3)

The data direction registers are used to control the direction of data flow at the port pins (P0, P2 and P3). DDR0 controls P0; DDR2 controls P2; DDR3 controls P3. A logic 0 written to a bit makes the relevant port an input port. A logic 1 makes it an output port. The register is byte addressable; R/W.

Table 24 Data direction registers (address DDR0: 0XFBH; DDR2: 0XFCH; DDR3: 0XFDH); note 1

7	6	5	4	3	2	1	0
Srv_frc_flock	Srv_frc_lock	Srv_otd	Srv_da	Srv_cl	Srv_rab	Srv_startup	Serv_halt

Table 25 Description of DDR bits

BIT	SYMBOL	DESCRIPTION(1)
7	DDROUTX7	controls direction of PX.7
6	DDROUTX6	controls direction of PX.6
5	DDROUTX5	controls direction of PX.5
4	DDROUTX4	controls direction of PX.4
3	DDROUTX3	controls direction of PX.3
2	DDROUTX2	controls direction of PX.2
1	DDROUTX1	controls direction of PX.1
0	DDROUTX0	controls direction of PX.0

Note to Tables 24 and 25

1. X = 0, 2 or 3, depending on register selected (DDR0, DDR2 or DDR3).

8.1.11 Configuration Control Register (CCR)

The Config_cntrl register is used to control internal multiplexers. Note that the motor output configuration register in the decoder is used to choose between the decoder motor control and the QCLV motor control. The register is byte addressable; R/W.

Table 26 Description of CCR bits (address 0XFEH)

BIT POSITION(1)		SYMBOL	FUNCTION
READ	WRITE		
7	7	Config_cntrl.7	not used
6	6	Cnf_dac_clk_sel	selects clock to DAC; Cnf_dac_clk_sel = 1: $\frac{\text{master clock}}{2}$; Cnf_dac_clk_sel = 0: $\frac{\text{master clock}}{3}$
5	1	Cnf_AGC_bypass	AGC decoder bypass; Cnf_AGC_bypass = 1: bypass; Cnf_AGC_bypass = 0: use AGC
4	5	Cnf_lock_over	Lock_over_rule; Cnf_lock_over = 1: overrules the decoder signals force_lock, force_flock
3	4	Cnf_uPotd	selects OTD input; Cnf_uPotd = 1: controller; Cnf_uPotd = 0: DSICS
2	3	Cnf_sign_mag	selects PWM output mode; Cnf_sign_mag = 1: sign magnitude; Cnf_sign_mag = 0: two's complement
1	2	Cnf_filter	selects the filter in the QCLV motor control; Cnf_filter = 1: enable; Cnf_filter = 0: disable
0	0	Cnf_dircom	selects decoder communication mode; Cnf_dircom = 1: direct; Cnf_dircom = 0: indirect (via the servo)

Note

1. Note that the function of bit positions 1, 2, 3, 4 and 5 depends on whether the register is being written to or read from.

8.1.12 A SECOND SERIAL INTERFACE

A second serial interface is implemented using the following registers:

- SCON2: 0XC0
- SBUF2: 0XC1.

This is of course an interrupt function. Bit 6 of the IE register is used to enable this function. Bit 6 of the IP register is used to define this interrupt to the highest priority level. The new vector address of the interrupt could be 0033H.

8.1.13 MEMORY MAP ACCESS TO THE SERVO

Since the performance of a basic engine is largely determined by the subcode retrieval speed, fast access to the subcode buffer is desirable. The servo RAM is mapped onto the AUX RAM of the microcontroller. In this way it is possible to directly access the servo RAM registers; see Table 27.

Table 27 Servo memory map

ADDRESS (HEX)	CONTENTS
0X100	time_keeper
0X101	focus_stat
0X102	rad_stat
0X103	mem_sledge1_hi
0X104	offtrack_hi_rb
0X105	offtrack_lo_rb
0X106	mem_sledge1_lo
0X107	rad_int_hi
0X108	rad_int_lo
0X109	rad_offset_hi
0X10A	rad_error_gain_mem_hi
0X10B	tpi_gain_hi
0X10C	focus_error_mem
0X10D	rad_error_mem
0X10E	speed_hi
0X10F	speed_lo
0X110	focus_int_hi
0X111	focus_int_lo
0X112	drop_out_code
0X113	foc_prop_mem
0X114	FOCUS_PROP_MULT
0X115	FOCUS_INT_GAIN
0X116	RAMP_MEAN_VALUE
0X117	slee_mult_mem
0X118	RAMP_HEIGTH
0X119	FE_LEVEL
0X11A	timer1
0X11B	acc_stat_mem
0X11C	rad_prop_mult_mem
0X11D	rad_error_acc_mem

ADDRESS (HEX)	CONTENTS
0X11E	rad_int_gain_mem
0X11F	speed_mult_mem
0X120	rad_offset_lo
0X121	rad_error_gain_mem_lo
0X122	tpi_gain_lo
0X123	sp_mem_lo
0X124	sp_mem_hi
0X125	speed_setpoint
0X126	tpi_signal_mem
0X127	rad_ctrl_1_mem2
0X128	rad_ctrl_1_mem
0X129	rad_ctrl_2_mem
0X12A	rad_gain_mem
0X12B	stack 5
0X12C	stack 4
0X12D	stack 3
0X12E	stack 2
0X12F	stack 1
0X130	stack 0
0X131	oldcom
0X132	state_mult_mem
0X133	mem_sledge2_lo
0X134	mem_sledge2_h
0X135	RAMP_GAIN
0X136	slede_mult_mem2
0X137	FAST_SPEED
0X138	mem_sledge2_lo_lo
0X139	gain_filter2_mem_lo
0x13A	gain_filter2_mem_hi
0x13B	gain_filter1_mem

ADDRESS (HEX)	CONTENTS
0x13C	low_gain_mem
0x13D	gain_drempel_mem
0x13E	rad_ctrl_1_mem3
0x13F	focus_int_mem1
0x140	interruptreg
0x141	cd6statmem
0x142	HiState
0x143	MotorStatTime
0x144	mem_sledge1_drempel_lo
0x145	mem_sledge1_drempel_hi
0x146	sledge_pulse_mem
0x147	sledge_time_ou
0x148	speed_drempel_mem
0x149	hold_mult_mem
0x14A	xtra_preset
0x14B	cd6subadr
0x14C	cd6cmd1
0x14D	cd6cmd2
0x14E	asec
0x14F	asecold
0x150	aframe
0x151	aframemeold
0x152	playwatchtimer
0x153	interruptmask
0x154	playwatchtimer
0x155	trackcount1
0x156	timer2
0x157	jumpwatchtime
0x158	sledge_long_brake
0x159	radwatchstat
0x15A	sledge_power_mem
0x15B	rad_mem_part1
0x15C	StateTimerHi
0x15D	StateTimerLo

ADDRESS (HEX)	CONTENTS
0x15E	FocusStartTime
0x15F	MotorStartTime1
0x160	MotorStartTime2
0x161	RadInitTime
0x162	BrakeTime
0x163	RadialStartStat
0x164	sledge_pulse_height
0x165	focus_inject
0x166	radial_inject
0x167	detphase
0x168	oscinc
0x169	injectlevel1
0x16A	injectlevel2
0x16B	osc
0x16C	agcgainmem
0x16D	agcgainlo
0x16E	focus_offset
0x16F	inject_lo
0x170	offtrack_hi
0x171	oftrack_lo
0x172	not used
0x173	not used
0x174	subcode byte 0
0x175	subcode byte 1
0x176	subcode byte 2
0x177	subcode byte 3
0x178	subcode byte 4
0x179	subcode byte 5
0x17A	subcode byte 6
0x17B	subcode byte 7
0x17C	subcode byte 8
0x17D	subcode byte 9
0x17E	peak level left
0x17F	peak level right

8.1.14 DIGITAL PLL REGISTERS

The behaviour of the digital PLL can be monitored and controlled using the following registers:

1. PLL Frequency Register (address 0XECH):
   This register holds the 8 MSBs of the PLL frequency. The register is byte addressable; read only.
2. PLL DC Offset Register (address 0XEDH):
   This register holds the 8-bit asymmetry signal in two's complement form. The register is byte addressable; read only.
3. PLL Jitter Register (address 0XEE):
   This register holds the 8 MSBs of the 10 jitter bits. The register is byte addressable; read only.
4. PLL Int Inp Register (address 0XFF):
   Presets the 8 MSBs of the PLL frequency to a certain value. The register is byte addressable; R/W.

8.1.15 DIV17 REGISTER (address 0X9FH)

This register can be used to generate the serial communication baud rate. If this method is chosen, the baud rate will be 62259 × P. The 5 LSBs of DIV17 hold the value of P. The 2 MSBs connect this baud rate generator to UART 1 or UART 2 (see Table 28). The register is byte addressable; R/W.

Table 28 Baud rate to UART connection

BIT 7	BIT 6	DESCRIPTION
0	0	baud rate generator not selected
0	1	select baud rate generator only for UART1
1	0	select baud rate generator only for UART2
1	1	select baud rate generator for UART1 and UART2

Of course in ACE it is still possible to use timers 1 and 2 to generate the baud rate. Table 29 provides an overview of how various baud rates can be generated using timer 1, timer 2, and DIV17.

Table 29 Baud rate selection, timer based; note 1

BAUD RATE kBAUD	μPCLK (MHz)	MODE	SMOD	RELOAD TIMER 1	RELOAD TIMER 2	DIV17 (ACE)
1411.20	16.9344	0	X	X	X	X
996.14	16.9344	X	1	X	X	16
529.20	16.9344	2	1	X	X	X
498.07	16.9344	X	1	X	X	8
373.55	16.9344	X	1	X	X	6
264.60	16.9344	2	0	X	X	X
249.04	16.9344	X	1	X	X	4
186.78	16.9344	X	1	X	X	3
124.52	16.9344	X	1	X	X	2
88.20	16.9344	1	1	0XFF	X	X
66.15	16.9344	1	X	X	0XFFF0	X
62.26	16.9344	X	1	X	X	1
44.10	16.9344	1	0	0XFF	X	X
33.08	16.9344	1	X	X	0XFFE8	X
9.80	16.9344	1	1	0XF7	X	X

Note

1. X = don’t care.

8.2 Memory map

Table 30 Memory map

ADDRESS(1)	**UPPER →**							
LOWER ↓	**8**	**9**	**A**	**B**	**C**	**D**	**E**	**F**
0	PO	P1	P2	P3	SCON2	PSW	ACC	B
1	SP				SBUF2			
2	DPL							MOTQCLVL
3	DPH							MOTQCLVH
4	RSV							
5								
6								
7	PCON			RSV				
8	TCON	SCON1	IE	IP	T2CON	PSR	RSV	RSV
9	TMOD	SBUF	RSV	RSV	T2MOD	SCR	SSR	MOTSETP
A	TL0				RCAP2L			MOTGAIN
B	TL1				RCAP2H		DSR	DDR0
C	TH0				TL2		PLLFREQ	DDR2
D	TH1				TH2		PLLOFS	DDR3
E		CLKgen					PLLJITT	CONFIG
F		DIV17						PLLINT

Note

1. For example, hex address A8 = IE.

8.3 Summary of the functions controlled by decoder registers 0 to F

The decoder uses 16 programmable registers, accessible under internal microcontroller control. The addresses of these registers are given in Table 31, along with a summary of the functions performed. The INITIAL column shows the power-on reset state.

Table 31 Decoder Registers 0 to F

REGISTER	ADDRESS	DATA	FUNCTION	INITIAL[1]
0 (Fade and attenuation)	0000	X000	mute	reset
		X01X	attenuate	–
		X001	full scale	–
		X100	step down	–
		X101	step up	–
		0XXX	DACCLK operating	–
		1XXX	DACCLK 3-stated	reset
1 (Motor mode)	0001	X000	motor off mode	reset
		X001	motor brake mode 1	–
		X010	motor brake mode 2	–
		X011	motor start mode 1	–
		X100	motor start mode 2	–
		X101	motor jump mode	–
		X111	motor play mode	–
		X110	motor jump mode 1	–
		1XXX	anti-windup active	–
		0XXX	anti-windup off	reset
2 (Status control)	0010	0000	status = SUBQREADY-I	reset
		0001	status = MOTSTART1	–
		0010	status = MOTSTART2	–
		0011	status = MOTSTOP	–
		010X	status = PLL lock	–
		011X	status = MOTOR-OV	–
		1X00	status = FIFO overflow	–
		1X01	status = shock detect	–
		1X10	status = latched shock detect	–
		1X11	status = latched shock detect reset	–

REGISTER	ADDRESS	DATA	FUNCTION	INITIAL(1)
3 (DAC output)	0011	1010	I^2S-bus; CD-ROM mode	–
		1011	EIAJ; CD-ROM mode	–
		110X	I^2S-bus; 18-bit; $4f_s$ mode	reset
		1111	I^2S-bus; 18-bit; $2f_s$ mode	–
		1110	I^2S-bus; 16-bit; f_s mode	–
		000X	EIAJ; 16-bit; $4f_s$	–
		0011	EAIJ; 16-bit; $2f_s$	–
		0010	EIAJ; 16-bit; f_s	–
		010X	EIAJ; 18-bit; $4f_s$	–
		0111	EIAJ; 18-bit; $2f_s$	–
		0110	EIAJ; 18-bit; f_s	–
4 (Motor gain)	0100	X000	motor gain G = 3.2	reset
		X001	motor gain G = 4.0	–
		X010	motor gain G = 6.4	–
		X011	motor gain G = 8.0	–
		X100	motor gain G = 12.8	–
		X101	motor gain G = 16.0	–
		X110	motor gain G = 25.6	–
		X111	motor gain G = 32.0	–
		0XXX	new motor control	reset
		1XXX	standard CD6 motor control	–
5 (Motor bandwidth)	0101	XX00	motor f4 = 0.5 × n Hz	reset
		XX01	motor f4 = 0.7 × n Hz	–
		XX10	motor f4 = 1.4 × n Hz	–
		XX11	motor f4 = 2.8 × n Hz	–
		00XX	motor f3 = 0.85 × n Hz	reset
		01XX	motor f3 = 1.71 × n Hz	–
		10XX	motor f3 = 3.42 × n Hz	–
6 (Motor output configuration)	0110	XX00	motor power maximum 37%	reset
		XX01	motor power maximum 50%	–
		XX10	motor power maximum 75%	–
		XX11	motor power maximum 100%	–
		00XX	MOTOS, MOTOV pins 3-state	reset
		01XX	motor PWM mode	–
		10XX	motor PDM mode	–
		11XX	motor CDV mode	–

REGISTER	ADDRESS	DATA	FUNCTION	INITIAL(1)
7 (DAC output control)	0111	xxx0	DAC data normal value	reset
		xxx1	DAC data inverted value	–
		xx0x	left channel first at DAC (WCLK normal)	reset
		xx1x	right channel first at DAC (WCLK inverted)	–
		11xx	stereo output at DAC	reset
		10xx	left mono out at DAC	–
		01xx	right mono out at DAC	–
		00xx	both DAC channels killed	–
8 (PLL loop filter bandwidth)	see Table 32			
9 (PLL equalization)	1001	0111	equalization = –60 ns	–
		0110	equalization = –45 ns	–
		0101	equalization = –30 ns	–
		0100	equalization = –15 ns	–
		0011	equalization = 0 ns	reset
		0010	equalization = 15 ns	–
		0001	equalization = 30 ns	–
		0000	equalization = 45 ns	–
		1111	equalization = 60 ns	–
		1110	equalization = 75 ns	–
		1101	equalization = 90 ns	–
		1100	equalization = 105 ns	–
		1011	equalization = 120 ns	–
		1010	equalization = 135 ns	–
		1001	equalization = 150 ns	–
		1000	equalization = 165 ns	–
A (EBU output)	1010	xx0x	DOBM data before concealment	–
		xx1x	DOBM data after concealment and fade	reset
		x1x1	DOBM off; output LOW	–
		x0x1	class 1 crystal (<50 ppm)	–
		x0x0	class 2 crystal (<1000 ppm)	reset
		x1x0	class 3 crystal (>1000 ppm)	-
		0xxx	flags to DOBM off	reset
		1xxx	flags to DOBM on	–

REGISTER	ADDRESS	DATA	FUNCTION	INITIAL(1)
B (Speed control)	1011	x0xx	33.8688 MHz crystal present, or 8.4672 MHz crystal with SELPLL set HIGH	reset
		x1xx	16.9344 MHz crystal present	–
		0xxx	single speed mode (if register E = 0xxx) four times speed mode (if register E = 1xxx); note 2	reset
		1xxx	double speed mode (if register E = 0xxx) eight times speed mode (if register E = 1xxx); note 2	–
		xx00	standby 1: ‘CD-STOP’ mode	reset
		xx10	standby 2: ‘CD-PAUSE’ mode	–
		xx11	operating mode	–
C (Data slicer and AGC control)	1100	1xxx	slicer bandwidth $\frac{255}{n}$ or $\frac{112}{n}$ Hz	–
		01xx	slicer bandwidth $\frac{112}{n}$ or $\frac{56}{n}$ Hz	–
		00xx	slicer bandwidth $\frac{27}{n}$ or $\frac{13}{n}$ Hz	reset
		xx0x	digital equalizer enabled	–
		xx1x	digital equalizer disabled	reset
		xxx0	AGC active	reset
		xxx1	AGC inactive (on hold)	–
D (Versatile pins interface)	1101	xx01	subcode channels Q-W at SUBQW	–
		xx10	SUBQW = 0	–
		xx11	SUBQW = 1	reset
		01xx	de-emphasis signal at DEEM, no internal de-emphasis filter	–
		10xx	DEEM = 0	–
		11xx	DEEM = 1	reset
E	1110	0xxx	bit controls operating speed mode, see register B	reset
		x0xx	audio features disabled	–
		x1xx	audio features enabled	reset
		xx0x	lock-to-disc mode disabled	reset
		xx1x	lock-to-disc mode enabled	–
		xxx0	low-stop = 0; motor brakes to 12%	reset
		xxx1	low-stop = 1; motor brakes to 6%	–

REGISTER	ADDRESS	DATA	FUNCTION	INITIAL(1)
F (Subcode interface)	1111	x0xx	subcode interface off	reset
		x1xx	subcode interface on	–
		0xxx	4-wire subcode	reset
		1xxx	3-wire subcode	–
		xx10	decrease AGC gain 1 step, when AGC off (register C)	–
		xx10	increase AGC gain 1 step, when AGC off (register C)	–

Notes

1. The initial column shows the power-on reset state.
2. Speed can be set to (1.5×, 3×, 6× and 12×) or (2×, 4×, 8× and 16×) via the microcontroller application register CLKgen.

Table 32 Loop filter bandwidth

REGISTER	ADDRESS	DATA	FUNCTION			INITIAL(1)
			LOOP BANDWIDTH (Hz)	INTERNAL BANDWIDTH (Hz)	LOW-PASS BANDWIDTH (Hz)	
8 (PLL loop filter bandwidth)	1000	0000	1640 × n	525 × n	8400 × n	–
		0001	3279 × n	263 × n	16800 × n	–
		0010	6560 × n	131 × n	33600 × n	–
		0100	1640 × n	1050 × n	8400 × n	–
		0101	3279 × n	525 × n	16800 × n	–
		0110	6560 × n	263 × n	33600 × n	–
		1000	1640 × n	2101 × n	8400 × n	–
		1001	3279 × n	1050 × n	16800 × n	reset
		1010	6560 × n	525 × n	33600 × n	–
		1100	1640 × n	4200 × n	8400 × n	–
		1101	3279 × n	2101 × n	16800 × n	–
		1110	6560 × n	1050 × n	33600 × n	–

Note

1. The initial column shows the power-on reset state.

8.4 Summary of servo commands

The servo commands are listed in Table 33.

Table 33 Servo commands

COMMANDS	CODE	BYTES	PARAMETERS
Write commands			
Preset_Latch	81H	1	<chip_init>
Write_focus_coefs1	17H	7	<foc_parm_3> <foc_int> <ramp_incr> <ramp_height> <ramp_offset> <FE_start> <foc_gain>
Write_focus_coefs2	27H	7	<defect_parm> <rad_parm_jump> <vel_parm2> <vel_parm1> <foc_parm_1> <foc_parm_2> <CA_drop>
Write_focus_command	33H	3	<foc_mask> <foc_stat> <shock_level>
Focus_gain_up	42H	2	<foc_gain> <foc_parm_1>
Focus_gain_down	62H	2	<foc_gain> <foc_parm_1>
Write_radial coefs	57H	7	<rad_length_lead> <rad_int> <rad_parm_play> <rad_pole_noise> <rad_gain> <sledge_parm_2> <sledge_parm_1>
Preset_init	93H	3	<RE_offset> <RE_gain> <sum_gain>
Radial_off	C1H	1	1Ch
Radial_init	C1H	1	3Ch
Short_jump	C3H	3	<offtrack_hi> <offtrack_lo> <rad_stat>
Long_jump	C5H	5	<brake_dist_max> <sledge_U_max> <offtrack_hi> <offtrack_lo> <rad_stat>
Steer_sledge	B1H	1	<sledge_Uout>
Write_decoder_reg	D1H	1	<deccmd>
Write_parameter	A2H	2	<param_ram_addr> <param_data>
Read commands			
Read_status	70H	up to 5	<foc_stat> <rad_stat> <rad_int_lpf> <offtrack_hi> <offtrack_lo>
Read_aux_status	F0H	up to 3	<RE_offset> <RE_gain> <sum_gain> <foc_error> <rad_error>
Read_Q_subcode	0H	up to 12	<Q_sub1 to 10> <peak_l> <peak_r>
Read_hilevel_status	E0H	up to 4	<intreq> <decstat> <seqstat> <motorstarttime>

8.4.1 SUMMARY OF SERVO COMMAND PARAMETERS

Table 34 Servo command parameters

PARAMETER	RAM ADDRESS	AFFECTS	POR VALUE	DETERMINES
foc_parm_1	–	focus PID	–	end of focus lead defect detector enabling OTD polarity
foc_parm_2	–	focus PID	–	focus low-pass focus error normalising
foc_parm_3	–	focus PID	–	focus lead length minimum light level
foc_int	14H	focus PID	–	focus integrator crossover frequency
foc_gain	15H	focus PID	70H	focus PID loop gain
CA_drop	12H	focus PID	–	sensitivity of drop-out detector
ramp_offset	16H	focus ramp	–	asymmetry of focus ramp
ramp_height	18H	focus ramp	–	p-p value of ramp voltage
ramp_incr	–	focus ramp	–	slope of ramp voltage
FE_start	19H	focus ramp	–	minimum value of focus error
RE_offset	–	radial initialization	–	initial value for RE_offset
RE_gain	–	radial initialization	–	initial value for RE_gain
sum_gain	–	radial initialization	–	initial value for sum_gain
rad_parm_play	28H	radial PID	–	end of radial lead
rad_pole_noise	29H	radial PID	–	radial low-pass
rad_length_lead	1CH	radial PID	–	length of radial lead
rad_int	1EH	radial PID	–	radial integrator crossover frequency
rad_gain	2AH	radial PID	70H	radial loop gain
rad_parm_jump	27H	radial jump	–	filter during jump
vel_parm1	1FH	radial jump	–	PI controller crossover frequencies
vel_parm2	32H	radial jump	–	jump pre-defined profile
speed_thres	48H	radial jump	–	maximum speed in fast track mode
act_sled	49H	radial jump	00H	electronic damping of radial actuator sledge bandwidth during jump
brake_dist_max	21H	radial jump	–	max sledge distance allowed in fast actuator steered mode
sledge_brake_dist	58H	radial jump	7FH	brake distance of sledge
offtrack_hi	–	radial jump	–	two’s complement MSB of number of tracks to jump
offtrack_lo	–	radial jump	–	two’s complement LSB of number of tracks to jump
rad_stat	–	radial/sledge	–	radial and sledge control
sledge_Umax	–	sledge	–	voltage on sledge during long jump
sledge_Uout	–	sledge	–	voltage on sledge when steered

PARAMETER	RAM ADDRESS	AFFECTS	POR VALUE	DETERMINES
sledge_parm_1	36H	sledge	–	sledge integrator crossover frequency shock filter
sledge_parm_2	17H	sledge	–	sledge low-pass frequencies sledge gain sledge operation mode
pulse_time	46H	pulsed sledge	–	control pulse width
pulse_height	64H	pulsed sledge	–	control pulse height
defect_parm	–	defect detector	–	defect detector setting
shock_level	–	shock detector	–	shock detector operation
playwatchtime	54H	watchdog	–	radial on-track watchdog time
jumpwatchtime	57H	watchdog	–	radial jump watchdog time-out
wradcontrol	59H	watchdog	–	enable/disable automatic radial off feature
chip_init	–	set-up	–	V_{RH} level setting enable/disable decoder interface decoder interface speed interrupt request polarity fast radial brake
xtra_preset	4AH	set-up	38H	laser on/off RA, FO, SL PDM modulating frequency enable/disable fast brake fast jumping circuit on/off
deccmd	4DH	decoder interface	–	send commands to decoder
interruptmask	53H	STATUS pin	–	enabled interrupts
seq_state	42H	autosequencer	–	autosequencer control
FocusStartTime	5EH	autosequencer	–	focus start time
MotorStartTime1	5FH	autosequencer	–	motorstart1 time
MotorStartTime2	60H	autosequencer	–	motorstart2 time
RadialInitTime	61H	autosequencer	–	radial initialisation time
BrakeTime	62H	autosequencer	–	brake time
RadCmdByte	63H	autosequencer	–	radial command byte
osc_frequency	68H	focus/radial AGC	–	AGC control frequency of injected signal
detect_phase	67H	focus/radial AGC	–	phase shift of injected signal
injectlevel1	69H	focus/radial AGC	–	amplitude of signal injected
injectlevel2	6AH	focus/radial AGC	–	amplitude of signal injected
agc_gain	6CH	focus/radial AGC	–	focus/radial gain

9 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNITS
$V_{DDD(pads)}$	digital supply voltage for pad cells	notes 1 and 2	–0.5	+6.5	V
$V_{DDD(core)}$	digital supply voltage for the core	notes 2 and 3	–0.5	+4.0	V
V_{DDA}	analog supply voltage	notes 2 and 3	–0.5	+4.0	V
V_I	input voltage (any input)		–0.5	V_{DD} + 0.5	V
V_O	output voltage (any output)		–0.5	+6.5	V
$\Delta V_{DDA-DDD(core)}$	supply voltage difference between the analog and digital (core) supply voltages		–	±0.25	V
I_O	output current (continuous)		–	±20	mA
$I_{I(d)}$	diode DC input current (continuous)		–	±20	mA
T_{amb}	operating ambient temperature		0	70	°C
T_{stg}	storage temperature		–55	+125	°C
V_{es}	electrostatic handling	note 4	–2000	+2000	V
		note 5	–200	+200	V

Notes

1. All pad supply pins ($V_{DDDn(pads)}$) must be connected externally to the same power supply.
2. All V_{SS} pins must be connected to the same external voltage.
3. All analog and digital core supply pins (V_{DDA} and $V_{DDDn(core)}$) must be connected externally to the same power supply.
4. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ series resistor with a rise time of 15 ns.
5. Equivalent to discharging a 200 pF capacitor via a 2.5 μH series inductor.

10 CHARACTERISTICS

10.1 General characteristics

$V_{DDD(pads)}$ = 4.5 to 5.5 V; $V_{DDD(core)}$ = 3.0 to 3.6 V; V_{DDA} = 3.0 to 3.6 V; V_{SS} = 0; T_{amb} = 0 to 70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
$V_{DDD(pads)}$	digital supply voltage for pad cells		4.5	5.0	5.5	V
$V_{DDD(core)}$	digital supply voltage for the core		3.0	3.3	3.6	V
V_{DDA}	analog supply voltage		3.0	3.3	3.6	V
I_{DD}	supply current	n = 8 mode	–	90	–	mA
Servo analog section ($V_{DDD(pads)}$ = 5.0 V; $V_{DDD(core)}$ = 3.3 V; V_{DDA} = 3.3 V; V_{SS} = 0; T_{amb} = 25 °C)						
PINS: D1, D2, D3, D4, S1, S2, V_{RH}, I_{refT}, FTC_L AND FTC_H						
C_{int}	internal capacitor D1, D2, D3, D4, S1 and S2		100	–	–	pF
I_{IrefT}	input current for I_{refT}	f_{sys} = 4.2336 MHz; notes 1 and 2	1.99	–	5.95	µA
R_{IrefT}	external resistor on I_{refT}	f_{sys} = 4.2336 MHz; notes 1 and 2	202	–	603	kΩ
I_D	input current for central diode input signal	f_{sys} = 4.2336 MHz; notes 2 and 3	3.97	–	11.91	µA
$I_{S(max)}$	maximum input current for satellite diode input signal	f_{sys} = 4.2336 MHz; notes 2 and 3	1.99	–	5.95	µA
I_{IrefT}	input current for I_{refT}	f_{sys} = 8.4672 MHz; notes 1 and 2	3.97	–	11.91	µA
R_{IrefT}	external resistor on I_{refT}	f_{sys} = 8.4672 MHz; notes 1 and 2	101	–	302	kΩ
I_{cd}	input current for central diode input signal	f_{sys} = 8.4672 MHz; notes 2 and 3	7.94	–	23.81	µA
I_{sd}	input current for satellite diode input signal	f_{sys} = 8.4672 MHz; notes 2 and 3	3.97	–	11.91	µA
V_{IrefT}	voltage on current input I_{refT}		–	virtual V_{GAP}	–	V
$V_{D1\text{-}D4,\ S1,\ S2}$	voltage on current inputs D1, D2, D3, D4, S1 and S2		–	virtual V_{SSA}	–	V
V_{GAP}	band gap voltage		–	1.2	–	V
V_{RH}	HIGH level reference voltage	note 4	0.5	–	2.5	V
$t_{ch(VRH)}$	charge time V_{RH} buffer		–	–	50	ns
(THD+N)/S	total harmonic distortion-plus-noise to signal ratio	at 0 dB; note 5	–	–50	–45	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
S/N	signal-to-noise ratio		–	55	–	dB
PSRR	power supply ripple rejection at V_{DDA}	note 6	–	45	–	dB
G_{tol}	gain tolerance	notes 2 and 7	–12	0	+12	%
ΔG	variation of gain between channels		–	–	2	%
α_{cs}	channel separation		–	60	–	dB
$V_{offset(FTC)}$	comparator FTC offset		–10	–	+10	mV
Decoder analog front-end ($V_{DDD(pads)}$ = 5.0 V; $V_{DDD(core)}$ = 3.3 V; V_{DDA} = 3.3 V; V_{SS} = 0; T_{amb} = 25 °C)						
PINS: MIDLAD, REFLCA, HFIN, REFHCA AND I_{ref}						
f_{clk}	ADC clock frequency	n = 16	67	–	–	MHz
B_{AGC}	AGC bandwidth (–3 dB)	n = 12/16	18/24	–	–	MHz
V_{offset}	total offset voltage		–7	0	+7	lsb
$G_{v(AGC)}$	AGC gain:					
	range		–4.4	–	+12.1	dB
	step		–	1.1	–	dB
$V_{i(AGC)(p-p))}$	AGC input signal range; peak-to-peak value		0.4	–	2.3	V
$V_{i(ADC)}$	input range ADC plus buffer		–	1.4	–	V
THD	total harmonic distortion	f_s = 5 MHz	–	–36	–	dB
		f_s = 10 MHz	–	–30	–	dB
		f_s = 18 MHz	–	–25	–	dB
S/N	signal-to-noise ratio		–	33	–	dB
Z_{in}	input impedance HFIN		–	10	–	kΩ
Digital inputs						
INPUT: DEFI; CMOS INPUT WITH PULL-DOWN						
V_{IL}	LOW-level input voltage		–0.3	–	$0.3 \times V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7 \times V_{DD}$	–	V_{DD} + 0.3	V
$R_{pd(int)}$	internal pull-down resistance	V_I = 0	–	50	–	kΩ
C_i	input capacitance		–	–	10	pF
Input: RST; CMOS input with hysteresis						
$V_{th(r)}$	switching threshold rising		–	–	$0.8 \times V_{DD}$	V
$V_{th(f)}$	switching threshold falling		$0.2 \times V_{DD}$	–	–	V
V_{hys}	hysteresis voltage		–	$0.33 \times V_{DD}$	–	V
C_i	input capacitance		–	–	10	pF
INPUTS: RCK AND SELPLL; CMOS INPUTS						
V_{IL}	LOW-level input voltage		–0.3	–	$0.3 \times V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7 \times V_{DD}$	–	V_{DD} + 0.3	V
I_{LI}	input leakage current	V_I = 0 – V_{DD}	–10	–	+10	μA
C_i	input capacitance		–	–	10	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital output						
OUTPUTS: TPWM, TEN, SUBQW, $\overline{\text{DSDEN}}$, CLO, DEEM, DEFO AND OTD						
V_{OL}	LOW-level output voltage	I_{OL} = 2 mA	0	–	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = –2 mA	V_{DD} – 0.4	–	V_{DD}	V
C_L	load capacitance		–	–	25	pF
$t_{o(r)}$	output rise time	10% to 90% levels; C_L = 20 pF	–	23	–	ns
$t_{o(f)}$	output fall time	90% to 10% levels; C_L = 20 pF	–	27	–	ns
Open drain outputs						
OUTPUTS: RP, FOK, CFLG, C2FAIL, FB, TL, KILL AND LDON; OPEN DRAIN OUTPUTS						
V_{OL}	LOW-level output voltage	I_{OL} = +4 mA	0	–	0.4	V
I_{OL}	LOW-level output current		–	–	4	mA
C_L	load capacitance		–	–	25	pF
$t_{o(f)}$	output fall time	90% to 10% levels; C_L = 20 pF	–	27	–	ns
3-state outputs						
OUTPUTS: DACCLK, VALID, DAC, DATA, WCLK, SCLK, MOTOS, MOTOV, RA, FO, SL, DOBM, SBSY, SFSY AND SUB						
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA	0	–	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = –4 mA	V_{DD} – 0.4	–	V_{DD}	V
C_L	load capacitance		–	–	50	pF
$t_{o(r)}$	output rise time	10% to 90% level; C_L = 20 pF	–	24	–	ns
$t_{o(f)}$	output fall time	90% to 10% levels; C_L = 20 pF	–	28	–	ns
I_{LI}	3-state leakage current	V_I = 0 – V_{DD}	–10	–	+10	µA
Digital Input/Output						
INPUTS/OUTPUTS: $\overline{\text{PSEN}}$, ALE AND $\overline{\text{EA}}$; CMOS INPUT/OUTPUT WITH PULL-UP						
V_{IL}	LOW-level input voltage		–0.3	–	0.3 × V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7 × V_{DD}	–	V_{DD} + 0.3	V
V_{OL}	LOW-level output voltage	I_{OL} = 2 mA	0	–	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = –2 mA	V_{DD} – 0.4	–	V_{DD}	V
$t_{o(r)}$	output rise time	10% to 90% levels; C_L = 20 pF	–	24	–	ns
$t_{o(f)}$	output fall time	90% to 10% levels; C_L = 20 pF	–	28	–	ns
C_L	load capacitance		–	–	50	pF
C_i	input capacitance		–	–	10	pF
R_{pu}	input pull-up resistance	V_I = 0	–	50	–	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
INPUTS/OUTPUTS: AD0 TO AD7, A8 TO A15, R_{XD0}, T_{XD0}, INT0, INT1, R_{XD1}, T_{XD1}, $\overline{WR}$ AND $\overline{RD}$						
V_{IL}	LOW-level input voltage		–0.3	–	$0.3 \times V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7 \times V_{DD}$	–	V_{DD} + 0.3	V
V_{OL}	LOW-level output voltage	I_{OL} = 2 mA	0	–	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = –2 mA	V_{DD} – 0.4	–	V_{DD}	V
I_L	3-state leakage current	V_{IN} = 0 – V_{DD}	–10	–	+10	µA
$t_{o(r)}$	output rise time	10% to 90% levels; C_L = 20 pF	–	24	–	ns
$t_{o(f)}$	output fall time	90% to 10% levels; C_L = 20 pF	–	28	–	ns
C_L	load capacitance		–	–	50	pF
C_i	input capacitance		–	–	10	pF
INPUT: XTALI (EXTERNAL CLOCK)						
V_{IL}	LOW-level input voltage		–0.3	–	+0.5	V
V_{IH}	HIGH-level input voltage		–2.0	–	V_{DD} + 0.3	V
t_{IH}	input HIGH time	relative to period	45	–	55	%
I_{LI}	input leakage current		–10	–	+10	µA
C_i	input capacitance		–	–	10	pF
OUTPUT: XTALO						
f_{xtal}	crystal frequency	note 8	8	8.4672	35	MHz
$g_{m(mutual)}$	mutual transconductance	at 100 kHz	–	10	–	mA/V
G_v	small signal voltage gain	$A_V = g_m \times R_O$	–	18	–	
C_F	feedback capacitance		–	–	5	pF
C_o	output capacitance		–	–	10	pF

Notes

1. f_{sys} is always equivalent to $\frac{\text{servo clock}}{2}$; see Section 10.2.
2. Current input range (resistor range) can be extended by 25% (minimum and maximum) but gain tolerance in this region is 25%.
3. $I_{i(max)} = \frac{V_{GAP} \times C_{DAC}}{R_{ext} \times C_{ref}}$ for unipolar A/D converter. For D1, D2, D3 and D4, $C_{ref} = C_{DAC.}$ For S1 and S2, $C_{ref} = 0.5 \times C_{DAC}$
4. Internal reference source with 32 different output voltages. Selection is made during a calibration period or via the serial interface. The values given are for an unloaded V_{RH}. The output voltage $V_{RH} = 0.5 \times 10^{\frac{v}{44.4}}$, where v = 0 to 31.
5. V_{RH} = 2.5 V, measuring bandwidth: 200 Hz to 20 kHz, $f_{i(ADC)}$ = 1 kHz.
6. f_{ripple} = 1 kHz, V_{ripple} = 0.5 V peak-to-peak.
7. Gain tolerance is determined by the accuracy of the external resistor R_{ext}.
8. It is recommended that the series resistance of the crystal or ceramic resonator is ≤60 Ω.

10.2 Subcode interface timing characteristics

$V_{DDD(pads)}$ = 4.5 to 5.5 V; $V_{DDD(core)}$ = 3.0 to 3.6 V; V_{DDA} = 3.0 to 3.6 V; V_{SS} = 0; T_{amb} = 0 to 70 °C; unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Subcode interface timing (single speed × n); note 1; see Fig.11					
INPUT: RCK					
t_{clkH}	input clock HIGH time	$\frac{2}{n}$	$\frac{4}{n}$	$\frac{6}{n}$	µs
t_{clkL}	input clock LOW time	$\frac{2}{n}$	$\frac{4}{n}$	$\frac{6}{n}$	µs
t_r	input clock rise time	–	–	$\frac{80}{n}$	ns
t_f	input clock fall time	–	–	$\frac{80}{n}$	ns
$t_{d(SFSY-RCK)}$	delay time SFSY to RCK	$\frac{10}{n}$	–	$\frac{20}{n}$	µs
OUTPUTS: SBSY, SFSY AND SUB (C_L = 20 pF)					
$T_{cy(block)}$	block cycle time	$\frac{12.0}{n}$	$\frac{13.3}{n}$	$\frac{14.7}{n}$	ms
$t_{W(SBSY)}$	SBSY pulse width	–	–	$\frac{300}{n}$	µs
$T_{cy(frame)}$	frame cycle time	$\frac{122}{n}$	$\frac{136}{n}$	$\frac{150}{n}$	µs
$t_{W(SFSY)}$	SFSY pulse width (3-wire mode only)	–	–	$\frac{366}{n}$	µs
t_{SFSYH}	SFSY HIGH time	–	–	$\frac{66}{n}$	µs
t_{SFSYL}	SFSY LOW time	–	–	$\frac{84}{n}$	µs
$t_{d(SFSY-SUB)}$	delay time SFSY to SUB (P data) valid	–	–	$\frac{1}{n}$	µs
$t_{d(RCK-SUB)}$	delay time RCK falling to SUB	–	–	0	µs
$t_{h(RCK-SUB)}$	hold time RCK to SUB	–	–	$\frac{0.7}{n}$	µs

Note

1. The subcode timing is directly related to the over-speed factor, n, in normal operating mode; n is replaced by the disc speed factor, d, in lock-to-disc mode.

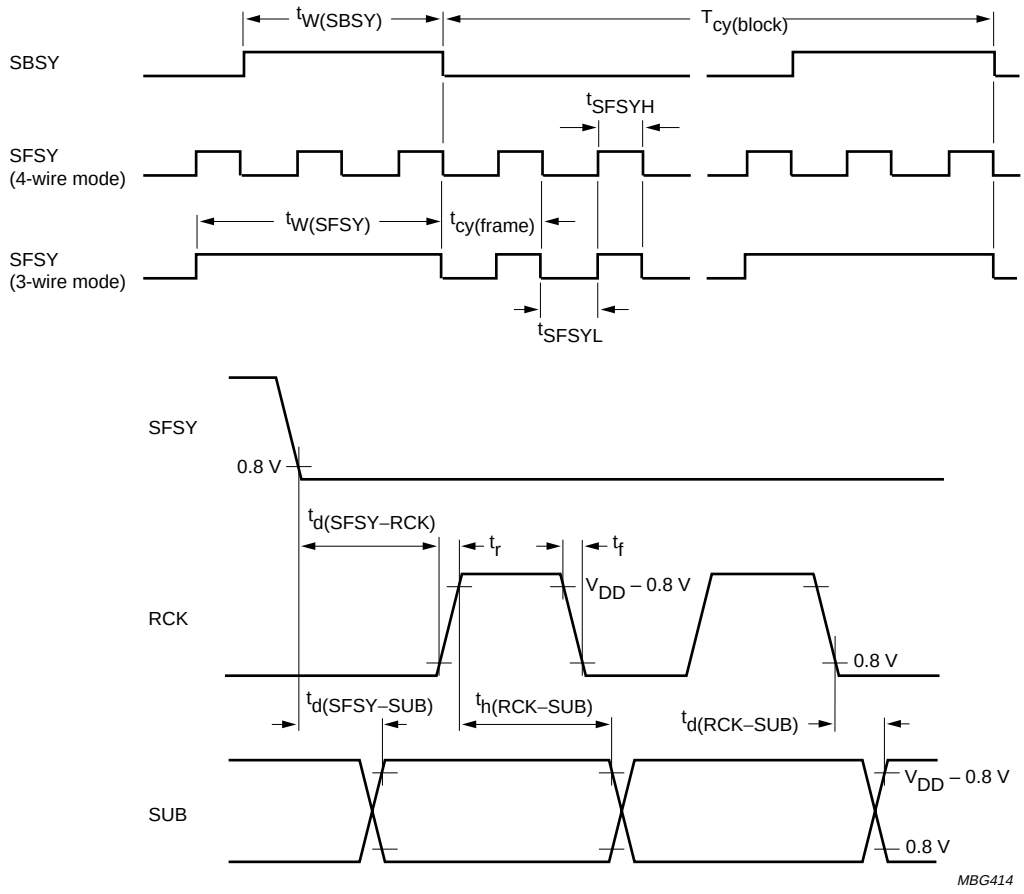


Fig.11 Subcode interface timing.

10.3 I²S timing characteristics

$V_{DDD(pads)}$ = 4.5 to 5.5 V; $V_{DDD(core)}$ = 3.0 to 3.6 V; V_{DDA} = 3.0 to 3.6 V; V_{SS} = 0; T_{amb} = 0 to 70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I²S Timing (single speed × n); note 1; see Fig.12						
CLOCK OUTPUT: SCLK (C_L = 20 pF)						
$T_{cy(clk)}$	output clock period	sample rate = f_s	–	472.4/n	–	ns
		sample rate = $2f_s$	–	236.2/n	–	ns
		sample rate = $4f_s$	–	118.1/n	–	ns
t_{clkH}	clock HIGH time	sample rate = f_s	166/n	–	–	ns
		sample rate = $2f_s$	83/n	–	–	ns
		sample rate = $4f_s$	42/n	–	–	ns
t_{clkL}	clock LOW time	sample rate = f_s	166/n	–	–	ns
		sample rate = $2f_s$	83/n	–	–	ns
		sample rate = $4f_s$	42/n	–	–	ns
OUTPUTS: WCLK, DATA, VALID AND DAC (C_L = 20 pF)						
t_{su}	set-up time	sample rate = f_s	95/n	–	–	ns
		sample rate = $2f_s$	48/n	–	–	ns
		sample rate = $4f_s$	24/n	–	–	ns
t_h	hold time	sample rate = f_s	95/n	–	–	ns
		sample rate = $2f_s$	48/n	–	–	ns
		sample rate = $4f_s$	24/n	–	–	ns

Note

1. I²S timing is directly related to the over-speed factor, n, in normal operating mode; n is replaced by the disc speed factor, d, in lock-to-disc mode.

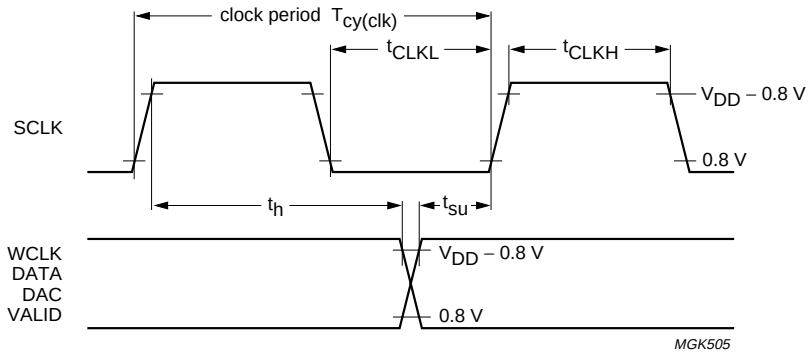
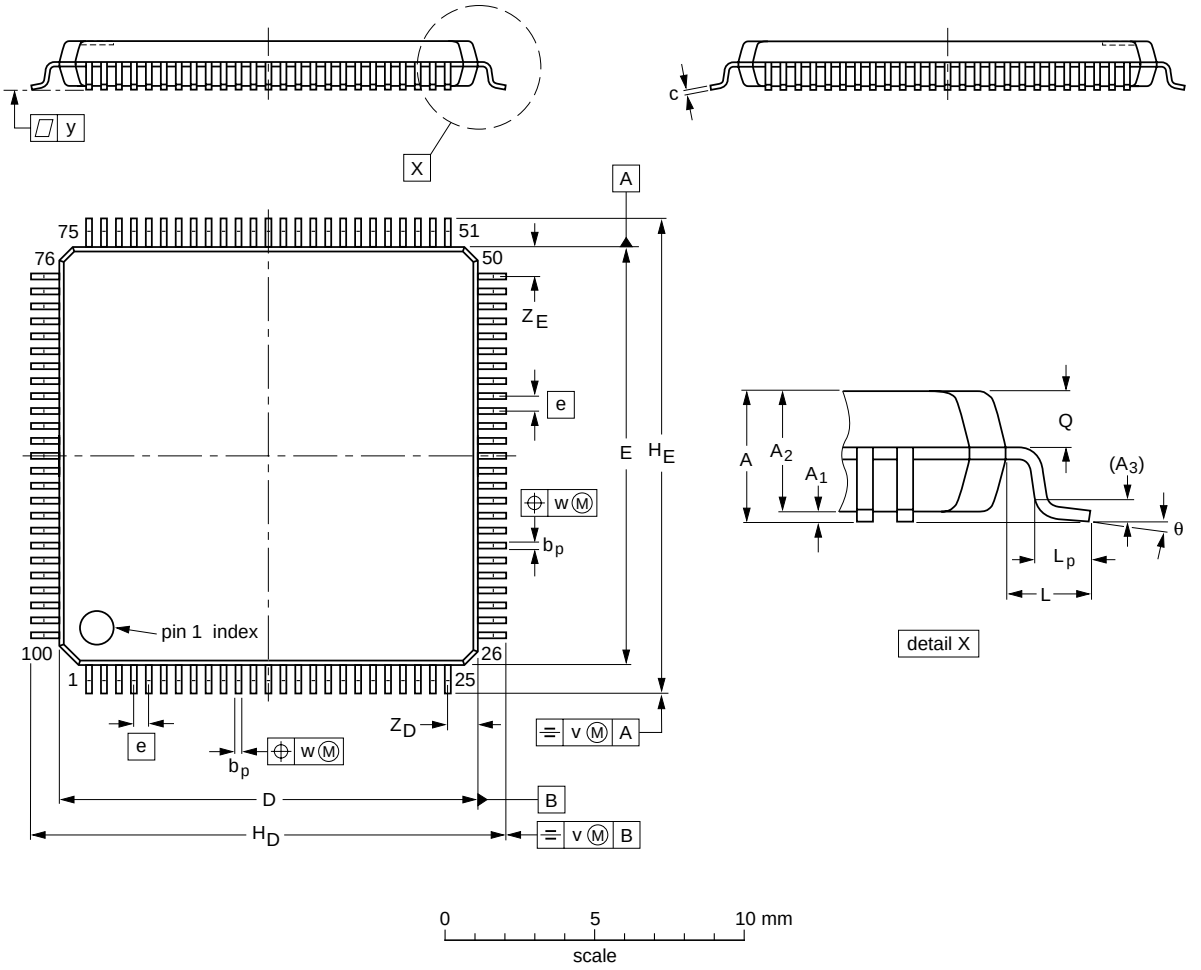


Fig.12 I²S Timing.

11 PACKAGE OUTLINE

LQFP100: plastic low profile quad flat package; 100 leads; body 14 x 14 x 1.4 mm **SOT407-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.5 1.3	0.25	0.28 0.16	0.18 0.12	14.1 13.9	14.1 13.9	0.5	16.25 15.75	16.25 15.75	1.0	0.75 0.45	0.70 0.57	0.2	0.12	0.1	1.15 0.85	1.15 0.85	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT407-1						95-12-19

12 SOLDERING

12.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

12.2 Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

12.3 Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering the following packages: QFP52 (SOT379-1), QFP100 (SOT317-1), QFP100 (SOT317-2), QFP100 (SOT382-1) or QFP160 (SOT322-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

12.4 Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

13 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

14 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

NOTES

NOTES

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Printed in The Netherlands 657027/1200/01/pp60 Date of release: 1997 Jul 11 Document order number: 9397 750 02136

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