DATA SHEET

MPEG Multichannel

SAA2503
MPEG2 audio decoder

Objective specification
File under Integrated Circuits, IC01

1997 Jul 02

Philips
Semiconductors

PHILIPS

MPEG2 audio decoder SAA2503

FEATURES

- Single-chip MPEG2 multichannel audio decoder
- Decodes MPEG high quality audio:
  - MPEG1 layer 2 (44.1 kHz)
  - MPEG2 multichannel layer 2 (48 kHz)
  - Supports pause frames
- Outputs 2 channels
  - Quasi surround down-mixing for Left and Right Dolby surround channel (Lt and Rt)
  - Stereo down-mixing for stereo reproduction
  - Stereo signal selection
  - Single channel down-mixing
- Karaoke modes
- Linear PCM modes:
  - Down-sampling from 96 to 48 kHz
  - Pass 48 kHz signals
- Bitstream input interface I^2S-bus (IEC 1937 formatted)
- IEC 958 output interface (IEC 1937 formatted)
- IEC 958 output simultaneously available while decoding MPEG2
- I^2C-bus control
- Output flags for direct control
- Stand-alone operation possible (self-booting)
- No external DRAM or SRAM required
- On-chip PLL for internal clock generation
- 13.5 or 27 MHz master clock
- 100 pins plastic LQFP package
- 5 V power supply.

APPLICATIONS

This IC is mainly intended for use in Digital Versatile Disc (DVD) players. However it may also be used in any application that is able to accept an MPEG2 audio bitstreams such as:

- Set top boxes
- Multimedia PCs
- Digital television
- Next generation audio equipment.

GENERAL DESCRIPTION

The SAA2503 incorporates all necessary functions, such as MPEG2 multichannel audio decoding plus down-mixing, MPEG1 layer 2 decoding, Linear PCM (LPCM) processing all producing high quality audio. Together with the serial audio interfaces and the IEC 958 transmitter this allows for the complete audio function of a DVD player in a single chip.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA2503HT	LQFP100	plastic low profile quad flat package; 100 leads; body 14 x 14 x 1.4 mm	SOT407-1

FUNCTIONAL I/O DIAGRAM

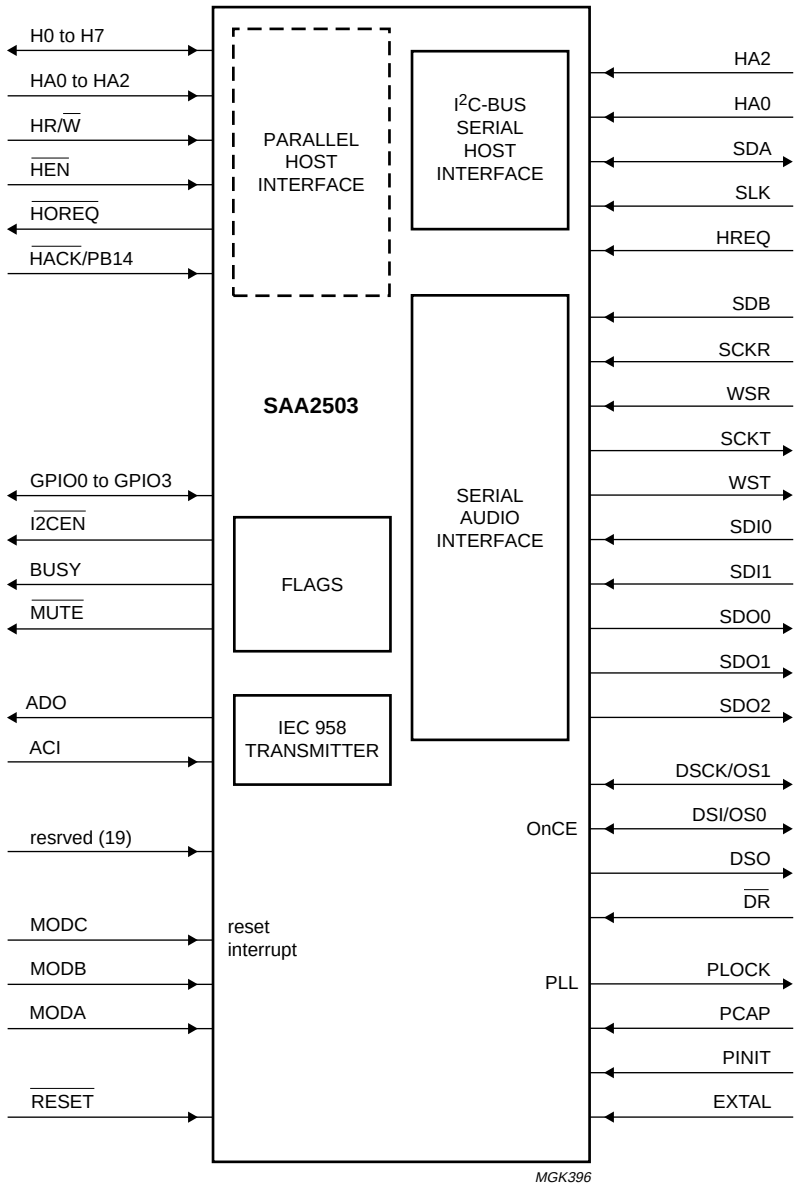


Fig.1 Functional I/O diagram.

PINNING

SYMBOL	PIN	I/O	DESCRIPTION
n.c.	1	–	not connected
n.c.	2	–	not connected
GNDA1	3	GND	ground 1 for some sections of internal logic
n.c.	4	–	not connected
n.c.	5	–	not connected
H7/PB7	6	I/O	not used
H6/PB6	7	I/O	not used
GNDH1	8	GND	isolated ground 1 for the HI I/O drivers
HOA2/PB10	9	I/O	not used
V_{CCH1}	10	supply	isolated power supply 1 for some sections of the internal chip logic
HOA1/PB9	11	I/O	not used
HR/$\overline{W}$/PB11	12	I/O	not used
$\overline{HEN}$/PB12	13	I/O	not used
V_{CCQ1}	14	supply	isolated power supply 1 for the HI I/O drivers
GNDQ1	15	GND	isolated ground 1 for the internal logic
$\overline{HACK}$/PB14	16	I/O	not used
GNDH2	17	GND	isolated ground 2 for the HI I/O drivers
HOA0/PB8	18	I/O	not used
H5/PB5	19	I/O	not used
V_{CCH2}	20	supply	isolated power supply 2 for the HI I/O drivers
H4/PB4	21	I/O	not used
H3/PB3	22	I/O	not used
GNDH3	23	GND	isolated ground 3 for the HI I/O drivers
H2/PB2	24	I/O	not used
H1/PB1	25	I/O	not used
H0/PB0	26	I/O	not used
$\overline{HOREQ}$/PB13	27	I/O	not used
GNDH4	28	GND	isolated ground 4 for the HI I/O drivers
V_{CCH3}	29	supply	isolated power supply 3 for the HI I/O drivers
ADO	30	O	digital audio data output
ACI	31	I	audio clock input
n.c.	32	–	not connected
n.c.	33	–	not connected
n.c.	34	–	not connected
PLOCK	35	O	HIGH when PLL is phase locked
V_{CCQ2}	36	supply	isolated power supply 2 for some sections of the internal chip logic
GNDQ2	37	GND	isolated ground 2 for the internal logic
PINIT	38	I	PLL enable/disable control
GNDP	39	GND	ground dedicated for the PLL
PCAP	40	I	PLL capacitor input

SYMBOL	PIN	I/O	DESCRIPTION
V_{CCP}	41	supply	supply voltage for the Phase Locked Loop (PLL)
EXTAL	42	I	external clock/crystal Input
SCL	43	I	I^2C-bus serial clock
GNDS1	44	GND	isolated ground 1 for the SHI I/O drivers
SDA	45	I/O	I^2C-bus data and acknowledge
$\overline{RESET}$	46	I	hardware reset for the microcontroller
MODA	47	I	mode select A
MODB	48	I	mode select B
MODC	49	I	mode select C
V_{CCS1}	50	supply	isolated power supply 1 for the SHI I/O drivers
HA0	51	I/O	I^2C-bus slave address 0
HA2	52	I	I^2C-bus slave address 2
$\overline{HREQ}$	53	I	host request
GNDS2	54	GND	isolated ground 2 for the SHI I/O drivers
SDO2	55	O	not used
SDO1	56	O	not used
SDO0	57	O	serial data output 0
V_{CCS2}	58	supply	isolated power supply 2 for the SHI I/O drivers
SCKT	59	O	transmit serial clock
WST	60	O	transmit word select
SCKR	61	I	receive serial clock
GNDQ3	62	GND	ground 3 dedicated for the PLL
V_{CCQ3}	63	supply	isolated power supply 3 for some sections of the internal chip logic
GNDS3	64	GND	isolated ground 3 for the SHI I/O drivers
WSR	65	I	receive word select
SDI1	66	I	serial data input 1
SDI0	67	I	not used
DSO	68	O	not used
DSI/OS0	69	O	not used
DSCK/OS1	70	O	not used
n.c.	71	–	not connected
n.c.	72	–	not connected
n.c.	73	–	not connected
n.c.	74	–	not connected
$\overline{DR}$	75	I	not used
SDB	76	I/O	general purpose I/O
$\overline{MUTE}$	77	I/O	general purpose I/O
GNDD1	78	GND	ground 1 for some sections of internal logic
BUSY	79	I/O	general purpose I/O
$\overline{I2CEN}$	80	I/O	general purpose I/O
V_{CCD1}	81	supply	isolated power supply 1 for some sections of the internal chip logic

SYMBOL	PIN	I/O	DESCRIPTION
GPIO3	82	I/O	not used
GPIO2	83	I/O	not used
GNDD2	84	GND	ground 2 for some sections of internal logic
GPIO1	85	I/O	not used
GPIO0	86	I/O	not used
GNDQ4	87	GND	ground 4 for some sections of internal logic
V_{CCQ4}	88	supply	isolated power supply 4 for some sections of the internal chip logic
n.c.	89	–	not connected
n.c.	90	–	not connected
GNDA2	91	GND	ground 2 for some sections of internal logic
n.c.	92	–	not connected
V_{CCA1}	93	supply	isolated power supply 1 for some sections of the internal chip logic
n.c.	94	–	not connected
n.c.	95	–	not connected
GNDA3	96	GND	ground 3 for some sections of internal logic
n.c.	97	–	not connected
n.c.	98	–	not connected
n.c.	99	–	not connected
V_{CCA2}	100	supply	isolated power supply 2 for some sections of the internal chip logic

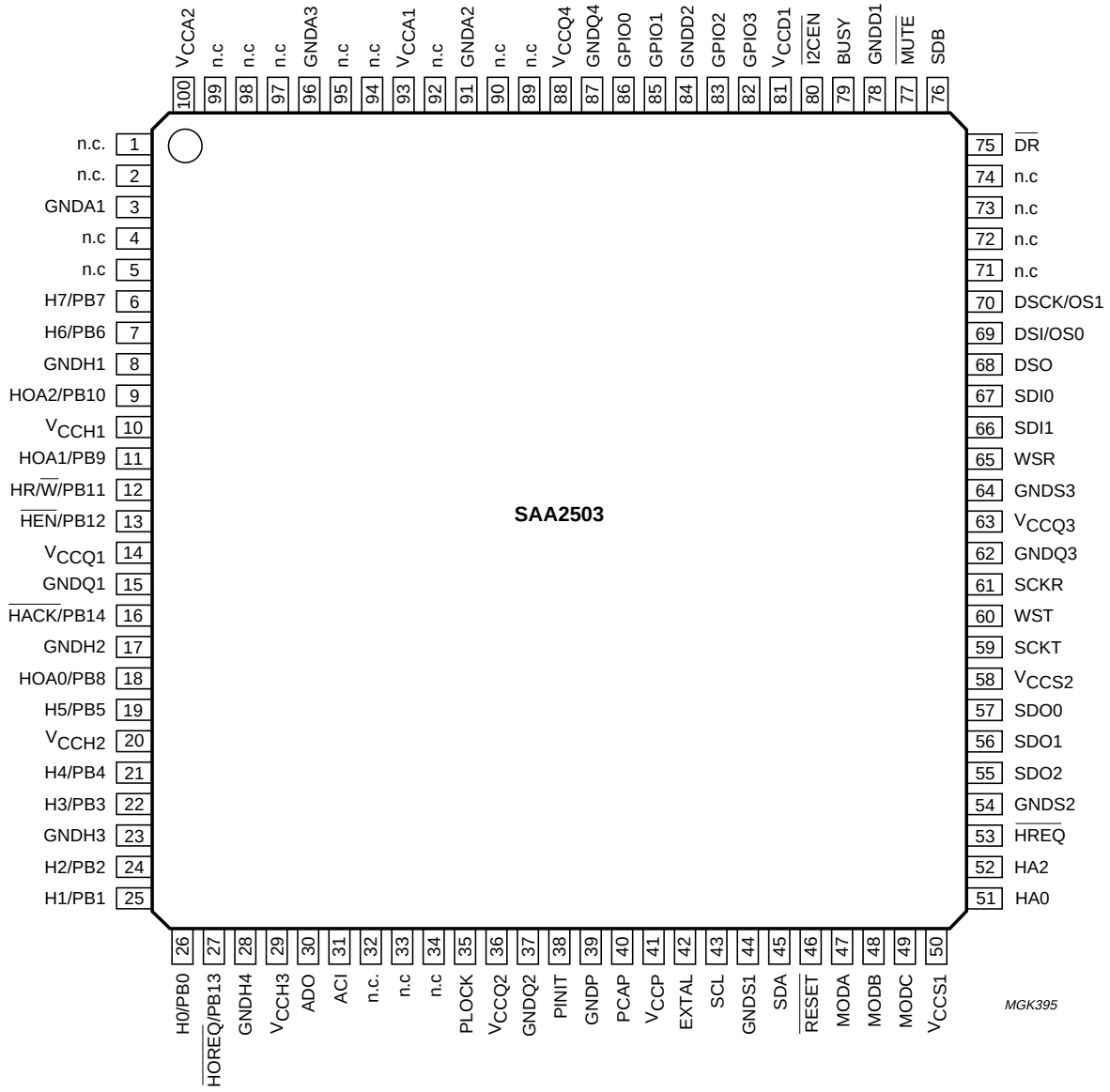


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Operating modes

The SAA2503 can operate in 2 modes.

Stand-alone (mode 4)

In this mode (modC = 1, modB = 0 and modA = 0) the SAA2503 boots itself from the internal program ROM after power-up and can start decoding when a decoding mode has been selected via the I²C-bus.

Booting via the I²C-bus (mode 7)

In this mode (modC = 1, modB = 1 and modA = 1) the SAA2503 starts executing an internal boot program that will receive 1536 bytes via the I²C-bus and then write those to an on-chip program RAM.

This mode allows the standard behaviour (I/O interfaces, additional processing) to be modified as specified in the stand-alone mode.

Decoding modes

The SAA2503 has the following decoding modes:

- MPEG decoding (48 kHz DVD; 44.1 kHz VCD) IEC 958 LPCM
- MPEG decoding (48 kHz DVD; 44.1 kHz VCD) IEC 958 BITSTR
- LPCM CD-DA (44.1 kHz)
- LPCM down-sampling DVD (96 kHz: 4 channel input; 48 kHz 2 channel output)
- LPCM DVD (48 kHz: 8 channel input; 2 channel output).

System clock

The preferred system clock to be applied to the EXTAL pin of the SAA2503 is 27 MHz if booted in mode 4 (stand-alone operation).

The internal PLL multiplies this clock by a factor of 3 to obtain an 81 MHz internal clock.

If using another external clock frequency it is advisable to ensure that:

- The internal PLL is disabled during booting when $f_{clk(ext)} > 27$ MHz
- That 10 MHz < ($f_{clk(ext)} \times 3$) < 81 MHz.

INTERFACING TO THE A/V SPLITTER

Serial audio interface

The serial audio interface can be configured as an I²S-bus interface and when required, as Quad I²S interface. The signal received via the I²S-bus is an encoded audio bitstream in accordance with IEC 1937, or LPCM.

Table 1 Pinning of the I²S-bus interface

PINS	DESCRIPTION	PIN NUMBER	DIRECTION
SDI0	high impedance	67	not used
SDI1	serial data	66	input/output
SDO0	serial data	57	output
SDO1	serial data	56	not used
SDO2	serial data	55	not used
SCKR	I²S-bus clock; notes 1 and 2	61	input
WSR	word select receive	65	input
SDB	serial data begin	76	input
SCKT	I²S-bus clock; notes 1 and 2	59	input
WST	word select transmit	60	input

Notes

1. SCKT is equal to SCKR when the I²S-bus format is the format of the input signal. When Quad I²S-bus is used SCKT = ¼SCKR.
2. The maximum allowed clock frequency for SCK is $\frac{1}{3}f_{clk}$ (f_{clk} is the internal clock generated by the PLL of the SAA2503).

MPEG2 bitstreams

The MPEG2 audio bitstream is received via the I²S-bus in the same format as specified in IEC 1937. The MPEG2 audio bitstream consists of data bursts of 1 frame. The data is formatted in 16-bit chunks. The time period until the next frame is filled with logic 0. The serial data is received by the SAA2503 via the SDI1 pin (pin 66).

For more information on transporting MPEG2 bitstreams via IEC 958 see IEC 1937.

Linear PCM (LPCM)

I²S-BUS

Linear PCM samples are received in an I²S-bus format. Serial audio data is received via SDI1 (pin 66). The I²S-bus clock is received via SCKR (pin 61) and the I²S-bus word select is received via WSR (pin 65); the I²S-bus clock operates at $64f_s$.

QUAD I²S-BUS

Quad I²S-bus is the interface providing audio samples in LPCM with 4 times the sampling frequency. The interface is an extension of the I²S-bus where the Serial Data Begin (SDB) indicates the first 2 channels out of 8 channels.

The audio samples are transferred with MSB first, where each sample occupies 32 bits, filled with logic 0.

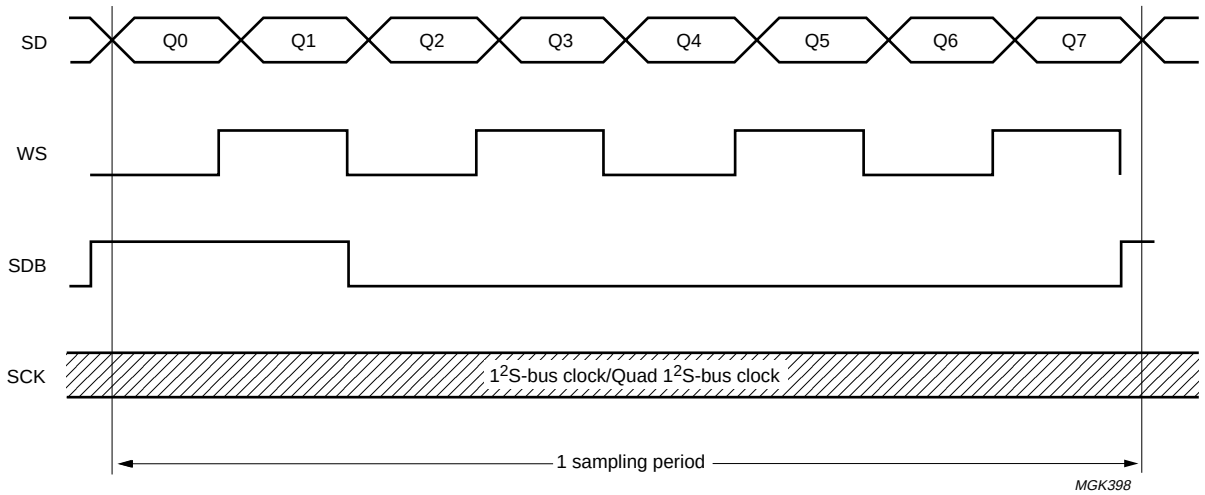


Fig.3 Quad I²S-bus frame format.

The SDB remains HIGH when only 2 channels LPCM or encode bitstreams (in accordance with IEC 1937) are transferred (Quad I²S-bus is equal to I²S-bus).

Table 2 Allocation of LPCM channels on Quad I²S-bus, f_s = 48 or 96 kHz

NUMBER OF LPCM CHANNELS	f_s (kHz)	INPUT							
		CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7
1	48	Q0	mute	mute	mute	mute	mute	mute	mute
2	48	Q0	Q1	mute	mute	mute	mute	mute	mute
3	48	Q0	Q1	Q2	mute	mute	mute	mute	mute
4	48	Q0	Q1	Q2	Q3	mute	mute	mute	mute
5	48	Q0	Q1	Q2	Q3	Q4	mute	mute	mute
6	48	Q0	Q1	Q2	Q3	Q4	Q5	mute	mute
7	48	Q0	Q1	Q2	Q3	Q4	Q5	Q6	mute
8	48	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
1	96	Q0	mute	mute	mute	Q0	mute	mute	mute
2	96	Q0	Q1	mute	mute	Q0	Q1	mute	mute
3	96	Q0	Q1	Q2	mute	Q0	Q1	Q2	mute
4	96	Q0	Q1	Q2	Q3	Q0	Q1	Q2	Q3

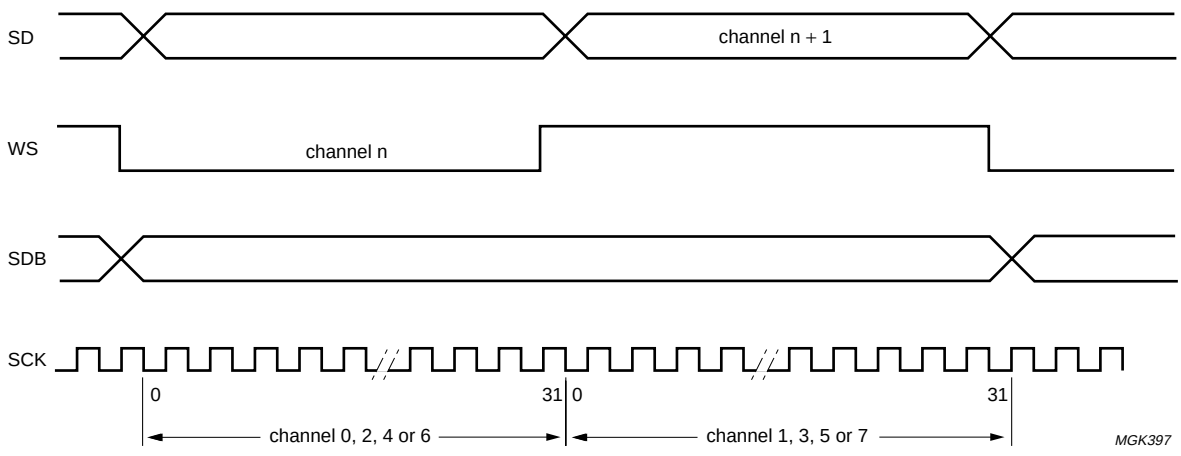


Fig.4 Quad I²S-bus channel format.

AUDIO OUTPUTS INTERFACING

Also see Chapter “Interfacing to the A/V splitter”.

Stereo output for DAC

The output stereo down-mixing signal is in I²S-bus format and can be directly connected to a DAC. The SDO0 (pin 57) provides the output for the serial audio data. Furthermore, SCKT (pin 59) provides the I²S-bus clock and WST (pin 60), the I²S-bus word select.

IEC 958 transmitter

The format of the IEC 958 interface consists of a sequence of IEC 958 sub frames. Each IEC 958 sub frame is normally used to carry one LPCM sample. The IEC 958 sub frame may also be used to convey data words. The non-PCM encoded audio bitstreams to be transferred are formed into data bursts. These bitstreams consist of a sequence of data words.

Each data burst contains a 64-bit burst_preamble, followed by the burst_payload.

The burst_preamble provides a sync_word, information on the burst_payload and the bitstream number.

The interface may convey one or more bitstreams. Each type of bitstream may impose a particular requirement for the repetition time for the data bursts that make up the bitstream.

The 16-bit data words of a data burst are placed in time slots 12 to 27 of an IEC 958 sub frame. In the consumer application, both odd and even IEC 958-sub frames (CH1 and CH2) are simultaneously used to carry 32-bit data words (32-bit mode). This allows the consumer IEC 958 to convey either 2-channel LPCM audio, or a set of alternating data words, but not both simultaneously. For more information see IEC 1937.

The IEC 958 interface is of the digital audio interface. This conveys LPCM or encoded audio bitstreams according to IEC 1937 (IEC 1937), using the ‘network layer’ of IEC 958 (IEC 958). The audio data will be accompanied by a validity bit, channel status and user data (sub code).

Table 3 Pinning of IEC 958 interface

PINS	DESCRIPTION	PIN NUMBER	DIRECTION
ADO	Audio Data Output	30	output
ACI	Audio Clock Input; note 1	31	input

Note

1. The ACI clock is $256f_s$ (or 512 or $384f_s$).

INTERFACING WITH THE MICROCONTROLLER

Flags

The SAA2503 has 3 flags which, after a hardware reset, are all initialized to logic 1.

1. I²C-bus communication disabled (pin 80); $\overline{\text{I2CEN}}$**:** this flag is set to logic 0 when the SAA2503 is ready to accept messages via the I²C-bus.
2. Life test (pin 79); BUSY: when the SAA2503 operates in the MPEG decoding mode, this flag toggles whenever the SAA2503 has detected a synchronization pattern. The flag will then produce a 20.833 Hz (f_{as} = 48 kHz) and a 19.140 Hz (f_{as} = 44.1 kHz) signal. It can be used to monitor the MPEG decoding process. When this flag no longer toggles there is an error. When the SAA2503 operates in one of the LPCM modes however, the flag produces either a 23.437 Hz (f_{as} = 48 kHz) or a 21.533 Hz (f_{as} = 44.1 kHz) signal.
3. MPEG decoding active and synchronised (pin 77); $\overline{\text{MUTE}}$: when the SAA2503 operates in the MPEG decoding mode, this flag indicates the state of the SAA2503 (synchronized or not). When this pin is at logic 1 the SAA2503 is out of sync, when set to logic 0 the SAA2503 is synchronized. It will not change state when the SAA2503 remains synchronized. When the SAA2503 is operating in one of the LPCM modes, the $\overline{\text{MUTE}}$ pin is set at logic 1 during initialization and logic 0 during processing.

I²C-bus interface

The I²C-bus interface supports data rates of up to 400 kbits/s. For a description of the I²C-bus see *“The I²C-bus and how to use it”*, ordering number 9398 393 40011.

For a description of the I²C-bus commands controlling the SAA2503 see Table 1.

APPLICATION SCHEMATIC

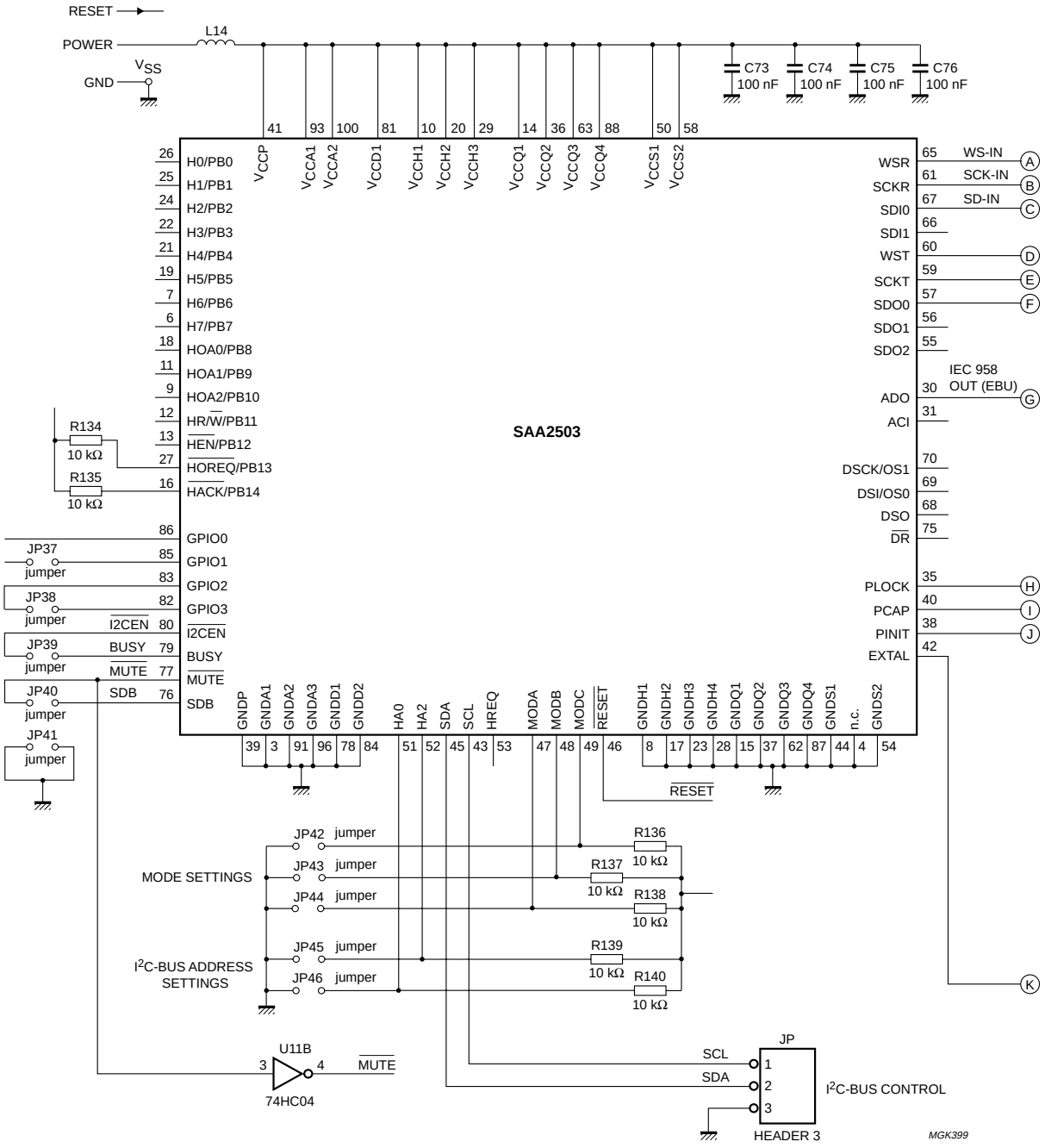


Fig.5 Application diagram (continued in Fig.6).

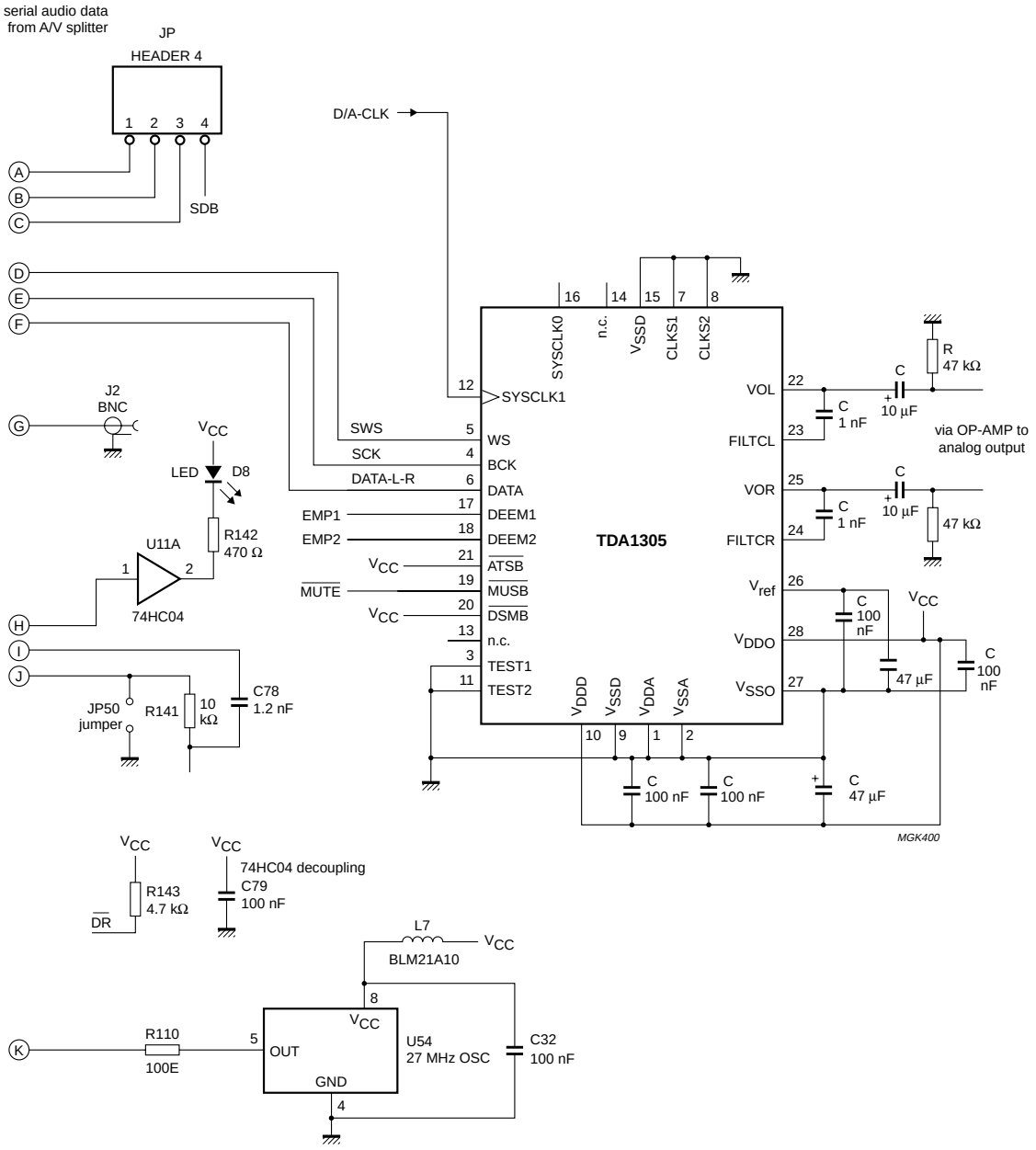
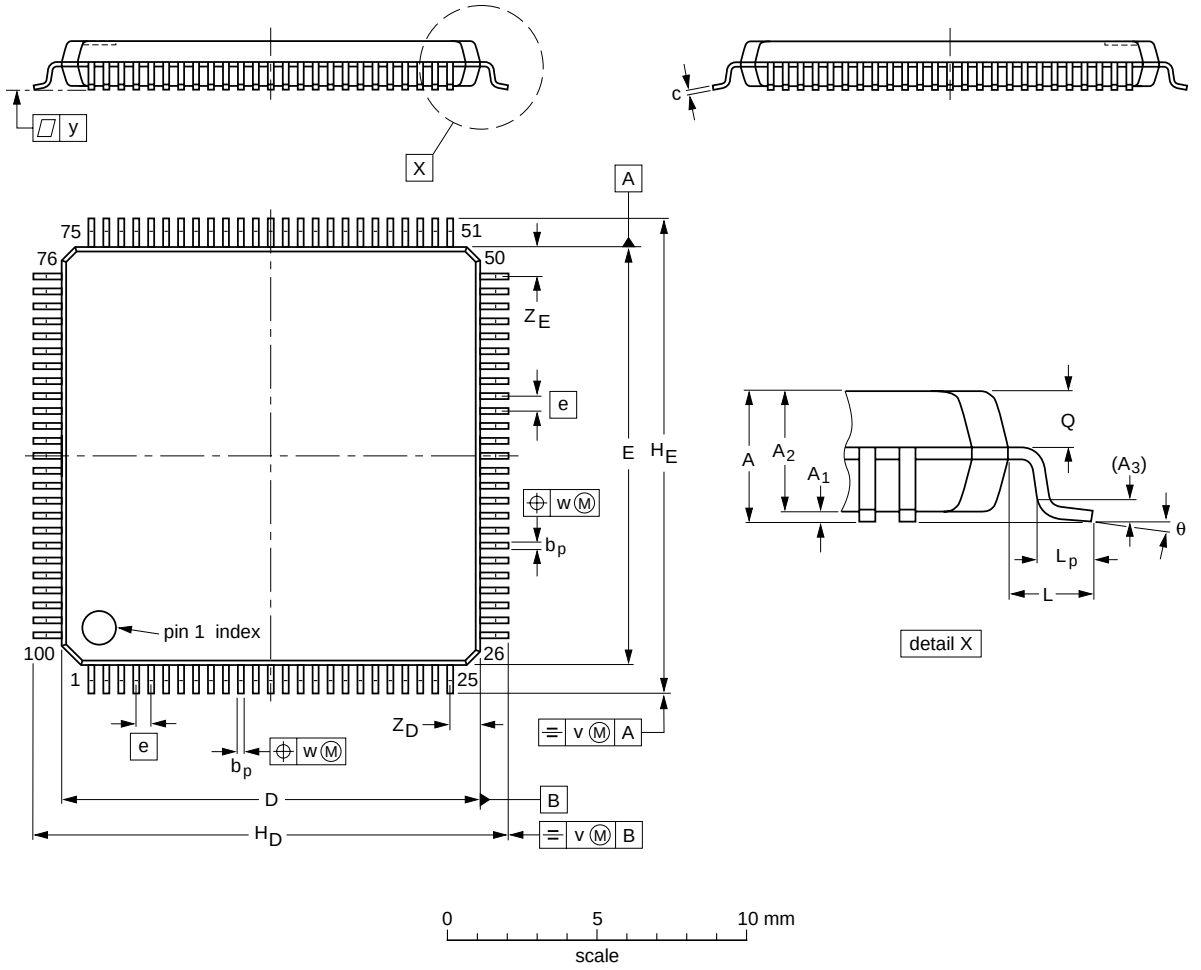


Fig.6 Application diagram (continued from Fig.5).

PACKAGE OUTLINE

LQFP100: plastic low profile quad flat package; 100 leads; body 14 x 14 x 1.4 mm **SOT407-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.5 1.3	0.25	0.28 0.16	0.18 0.12	14.1 13.9	14.1 13.9	0.5	16.25 15.75	16.25 15.75	1.0	0.75 0.45	0.70 0.57	0.2	0.12	0.1	1.15 0.85	1.15 0.85	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT407-1						95-12-19

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all LQFP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for LQFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering LQFP packages LQFP48 (SOT313-2), LQFP64 (SOT314-2) or LQFP80 (SOT315-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

NOTES

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