DATA SHEET

DIGITAL dcc COMPACT CASSETTE

SAA2022
Tape formatting and error correction for the DCC system

Product specification
Supersedes data of February 1993
File under Integrated Circuits, Miscellaneous

September 1995

Philips Semiconductors

PHILIPS

Tape formatting and error correction for the DCC system

SAA2022

FEATURES

- Integrated error correction encoder/decoder function with Digital Compact Cassette (DCC) optimized algorithms
- Control of capstan servo during recording and after recording by microcontroller
- Frequency and phase regulation of capstan servo during playback
- Choice of two Dynamic Random Access Memory (DRAM) types operating in page mode
- Scratch pad RAM area available to microcontroller in system DRAM
- Low power standby mode
- I^2S interface
- Microcontroller interface for high-speed transfer burst rates up to 170 kbytes per second
- SYSINFO and AUXILIARY data flags on microcontroller interface
- Protection against invalid AUXILIARY data
- +4 V operating voltage capability.

DIGITAL dcc COMPACT CASSETTE

GENERAL DESCRIPTION

Performing the tape formatting and error correction functions for DCC applications, the SAA2022 can be used in conjunction with the PASC (SAA2002/SAA2012), tape equalization (SAA2032), read amplifier (TDA1317 or TDA1318) and write amplifier (TDA1316 or TDA1319) circuits to implement a full signal processing system.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA2022GP	64	QFP(1)	plastic	SOT208A

Note

1. When using reflow soldering it is recommended that the Dry Packing instructions in the *"Quality Reference Pocketbook"* are followed. The pocketbook can be ordered using the code 9398 510 34011.

BLOCK DIAGRAM

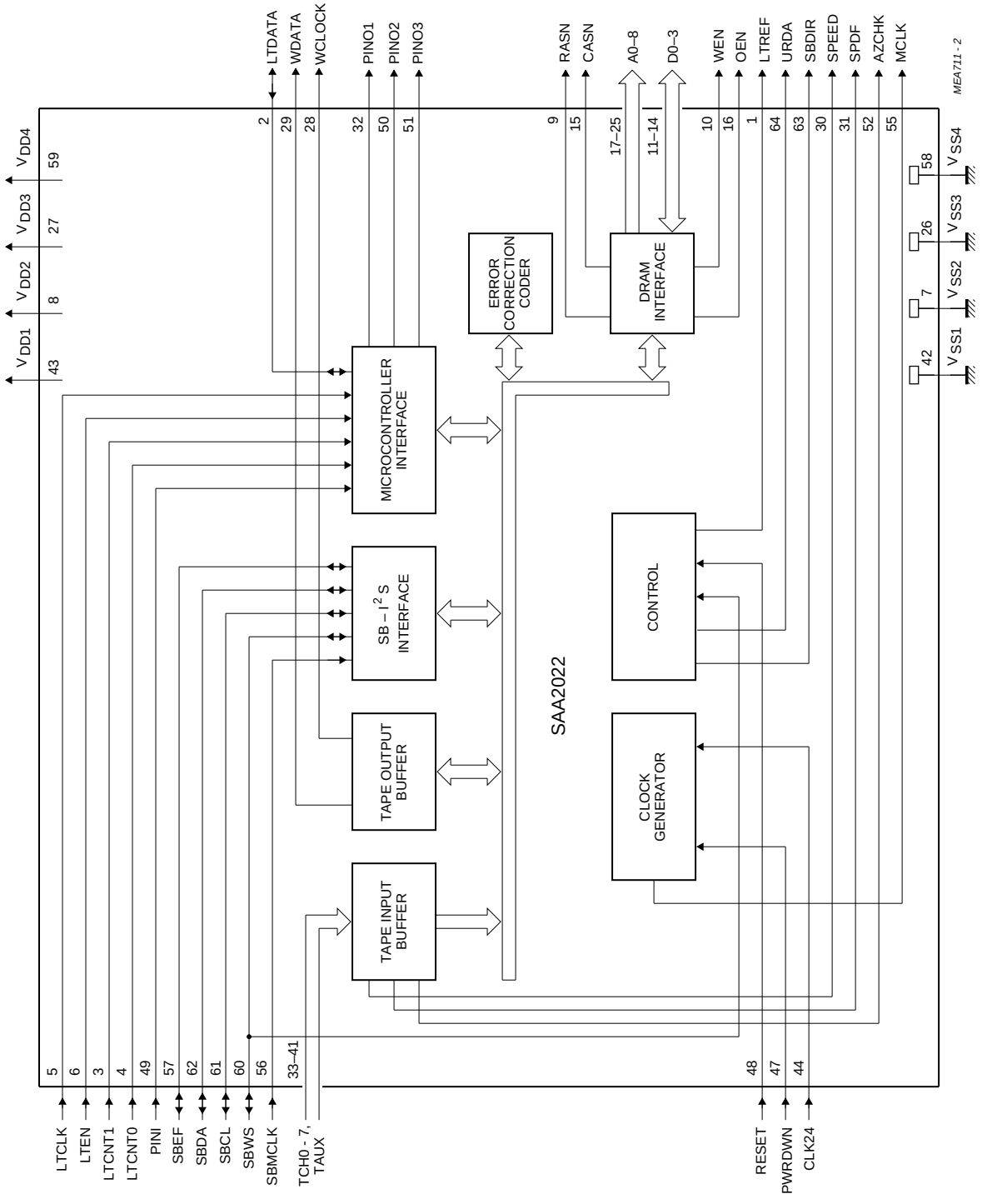


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
LTREF	1	timing reference for microcontroller interface
LTDATA	2	data for microcontroller interface (3-state; CMOS levels)
LTCNT1	3	control for microcontroller interface
LTCNT0	4	control for microcontroller interface
LTCLK	5	bit clock for microcontroller interface
LTEN	6	enable for microcontroller interface
V_{SS2}	7	supply ground (0 V)
V_{DD2}	8	supply voltage (+5 V)
RASN	9	DRAM row address strobe
WEN	10	DRAM write enable
D3	11	DRAM data (MSB); 3-state output; TTL compatible input
D2	12	DRAM data; 3-state output; TTL compatible input
D1	13	DRAM data; 3-state output; TTL compatible input
D0	14	DRAM data (LSB); 3-state output; TTL compatible input
CASN	15	DRAM column address strobe
OEN	16	DRAM output enable
A8	17	DRAM address (MSB)
A7	18	DRAM address
A6	19	DRAM address
A5	20	DRAM address
A4	21	DRAM address
A3	22	DRAM address
A2	23	DRAM address
A1	24	DRAM address
A0	25	DRAM address (LSB)
V_{SS3}	26	supply ground (0 V)
V_{DD3}	27	supply voltage (+5 V)
WCLOCK	28	clock for write amplifier transfers
WDATA	29	write amplifier serial data
SPEED	30	capstan phase information
SPDF	31	capstan frequency information
PINO1	32	Port expander output 1
TAUX	33	AUX channel input from SAA2032
TCH7	34	main data channel 7, input from SAA2032
TCH6	35	main data channel 6, input from SAA2032
TCH5	36	main data channel 5, input from SAA2032
TCH4	37	main data channel 4, input from SAA2032
TCH3	38	main data channel 3, input from SAA2032
TCH2	39	main data channel 2, input from SAA2032

SYMBOL	PIN	DESCRIPTION
TCH1	40	main data channel 1, input from SAA2032
TCH0	41	main data channel 0, input from SAA2032
V_{SS1}	42	supply ground (0 V)
V_{DD1}	43	supply voltage (+5 V)
CLK24	44	24.576 MHz clock from SAA2002
TEST0	45	test select LSB; **do not connect**
TEST1	46	test select MSB; **do not connect**
PWRDWN	47	sleep mode selection
RESET	48	reset input with hysteresis and pull-down resistor
PINI	49	Port expander input
PINO2	50	Port expander output 2
PINO3	51	Port expander output 3
AZCHK	52	azimuth check (channels 0 and 7)
TEST2	53	symbol error rate measurement output
TEST3	54	**do not connect**
MCLK	55	master clock output (6.144 MHz)
SBMCLK	56	master clock for SB-I^2S-interface
SBEF	57	byte error SB-I^2S-interface
V_{SS4}	58	supply ground (0 V)
V_{DD4}	59	supply voltage (+5 V)
SBWS	60	word select SB-I^2S-interface; 3-state output; CMOS levels
SBCL	61	bit clock SB-I^2S-interface; 3-state output; CMOS levels
SBDA	62	data line SB-I^2S-interface; 3-state output; CMOS levels
SBDIR	63	direction SB-I^2S-interface
URDA	64	unusable data SB-I^2S-interface

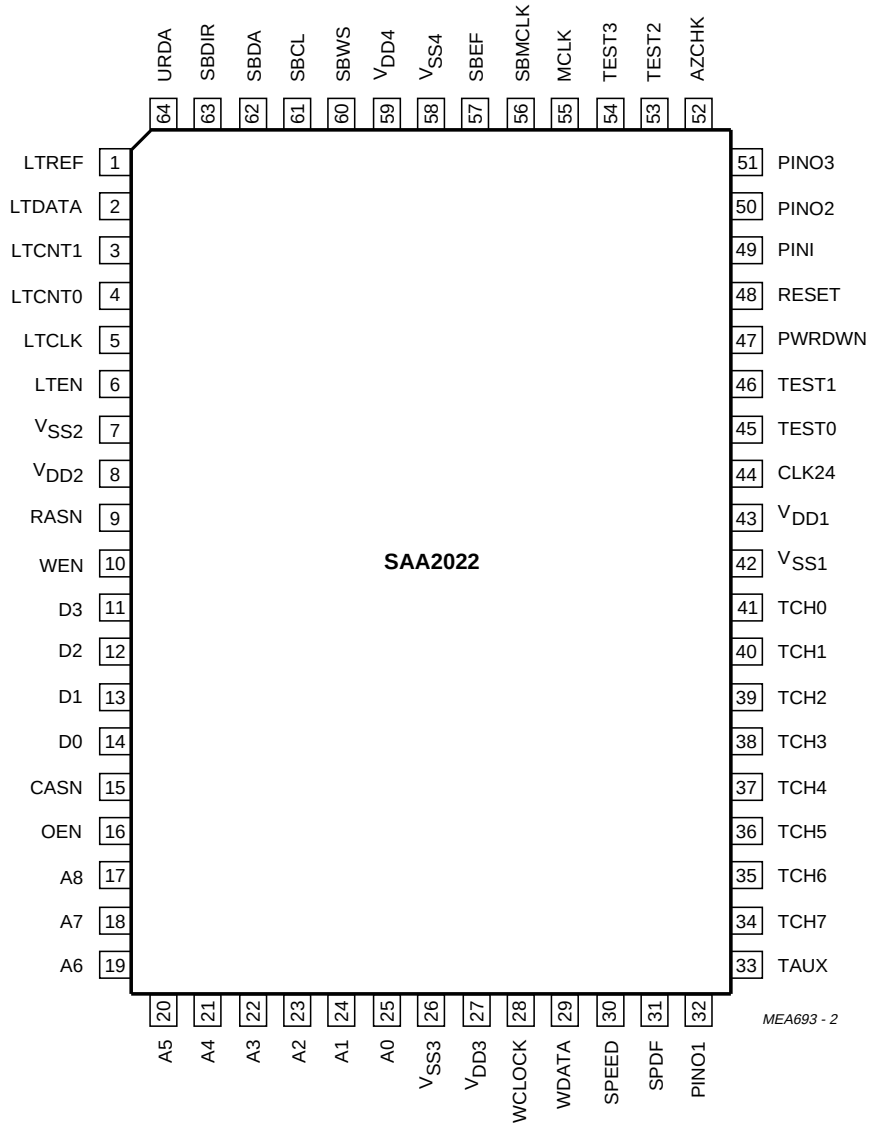


Fig.2 Pin configuration (SOT208A).

FUNCTIONAL DESCRIPTION

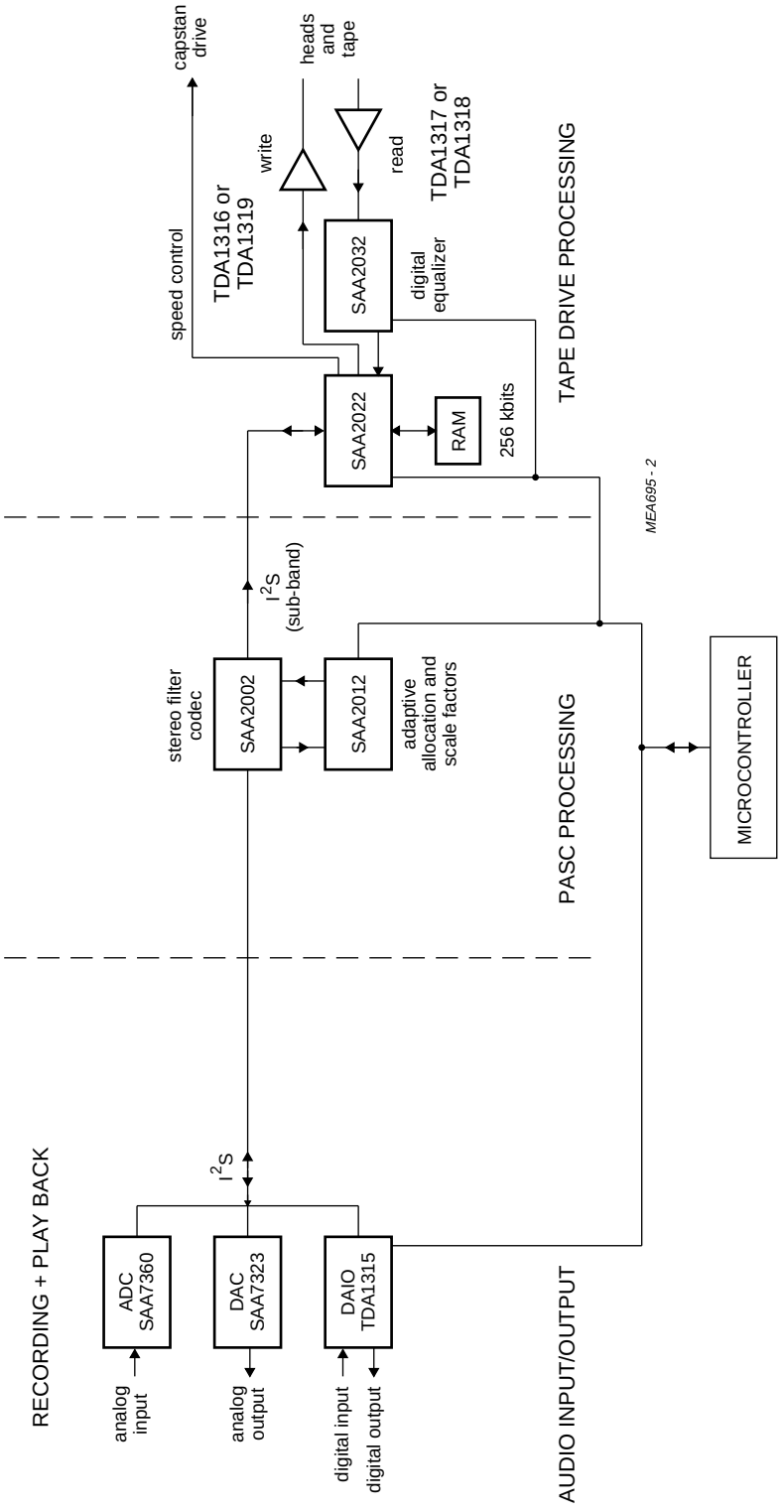


Fig.3 DCC data flow diagram.

The SAA2022 provides the following functions:

In Playback Modes

- Tape channel data and clock recovery
- 10 to 8 demodulation
- Data placement in DRAM
- C1 and C2 error correction decoding
- I^2S-interfacing to SB-I^2S-bus
- Interfacing to microcontroller for SYSINFO and AUX data
- Capstan control for tape deck.

In Record Modes

- I^2S-interfacing to SB-I^2S-bus
- C1 and C2 error correction encoding
- Formatting for tape transfer
- 8 to 10 modulation
- Interfacing to microcontroller for SYSINFO and AUX data
- Capstan control for tape deck, programmable by microcontroller.

Operational Modes

The 3 basic modes of operation are:

- DPAP - Main data (audio) and SYSINFO play, AUX play
- DRAR - Main data (audio) and SYSINFO record, AUX record
- DPAR - Main data (audio) and SYSINFO play, AUX record.

Hardware Interfacing

RESET

This is an active HIGH input signal which resets the SAA2022 and brings it into its default mode, DPAP. This should be connected to the system reset, which can be driven by the microcontroller. The duration of the reset pulse should be at least 15 μs. This pin has an internal pull-down resistor of between 20 kΩ and 125 kΩ.

PWRDWN

This pin is an active HIGH signal which places the SAA2022 in a “SLEEP” mode. When the SAA2022 is in “SLEEP” mode and the CLK24 is either held HIGH or held LOW, there is no activity in the device, thus resulting in no EMI and a low power dissipation (typically <10% of operational dissipation). This pin should be connected to the DCC power-down signal, which can be driven by the system microcontroller.

To enter the “SLEEP” mode the SAA2022 should reset and hold reset. After a delay of at least 15 μs the PWRDWN pin should be brought HIGH after which the state of the reset pin is “don’t care”. The power dissipation is reduced further when the CLK24 input signal stops.

When recovering from “SLEEP” mode the PWRDWN pin should be driven LOW and the chip reset with a pulse of at least 15 μs duration.

CLK24

This is the 24.576 MHz clock input and should be connected directly to the SAA2002 CLK24 pin.

Connections to SAA2032

TCH0 TO TCH7 AND TAUX

These lines are the equalized and clipped (to V_{DD}) tape channel inputs and should be connected to the SAA2032 pins TCH0 to TCH7 and TAUX.

Sub-band I^2S-bus Connections

The timing for the SB-I^2S-interface is given in Figs 4 to 9.

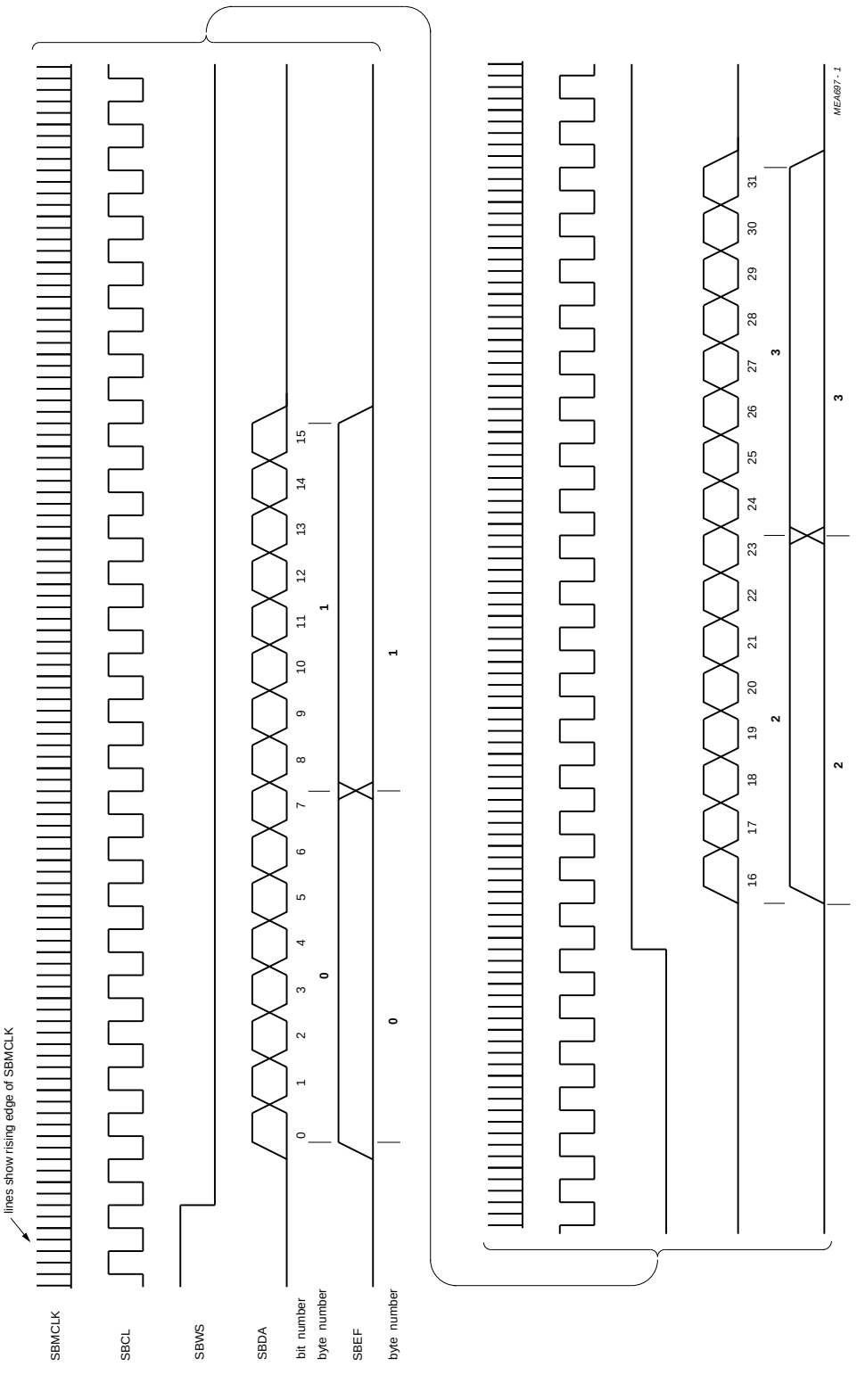


Fig.4 SB-I²S-interface in playback master mode (1).

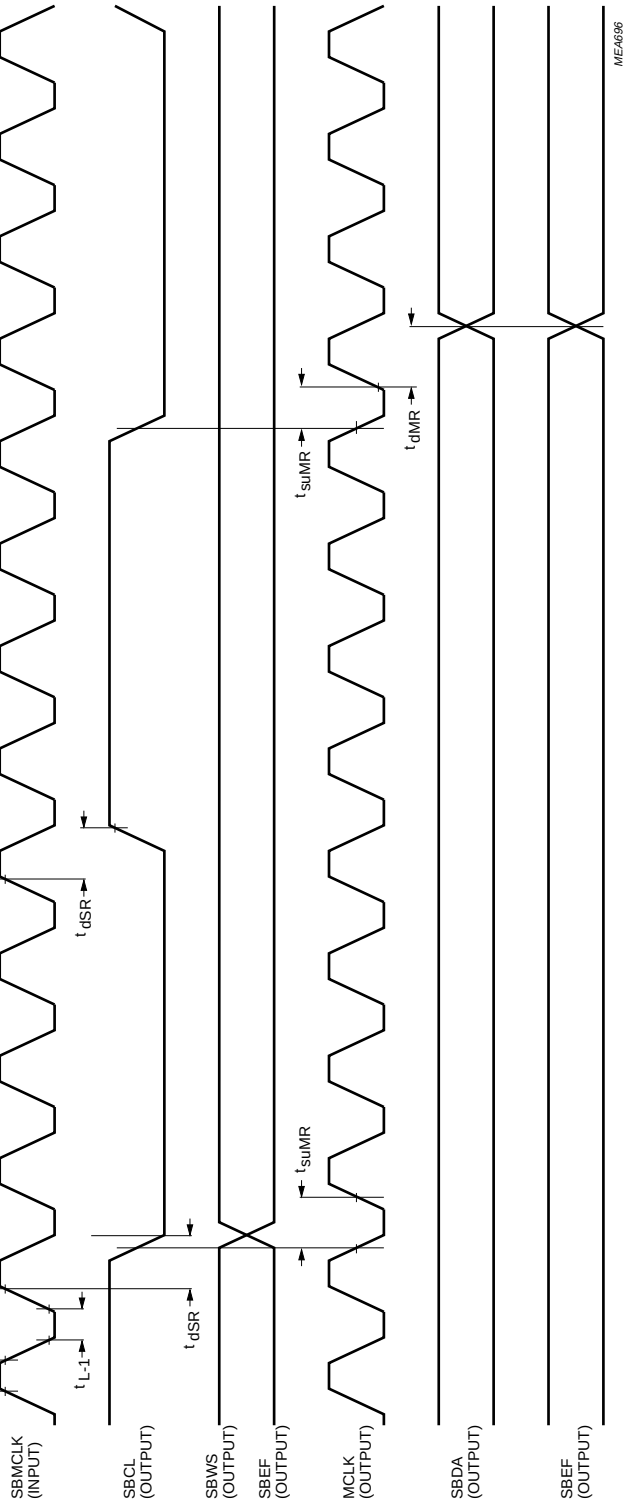


Fig.5 SB-I²S-interface in playback master mode (2).

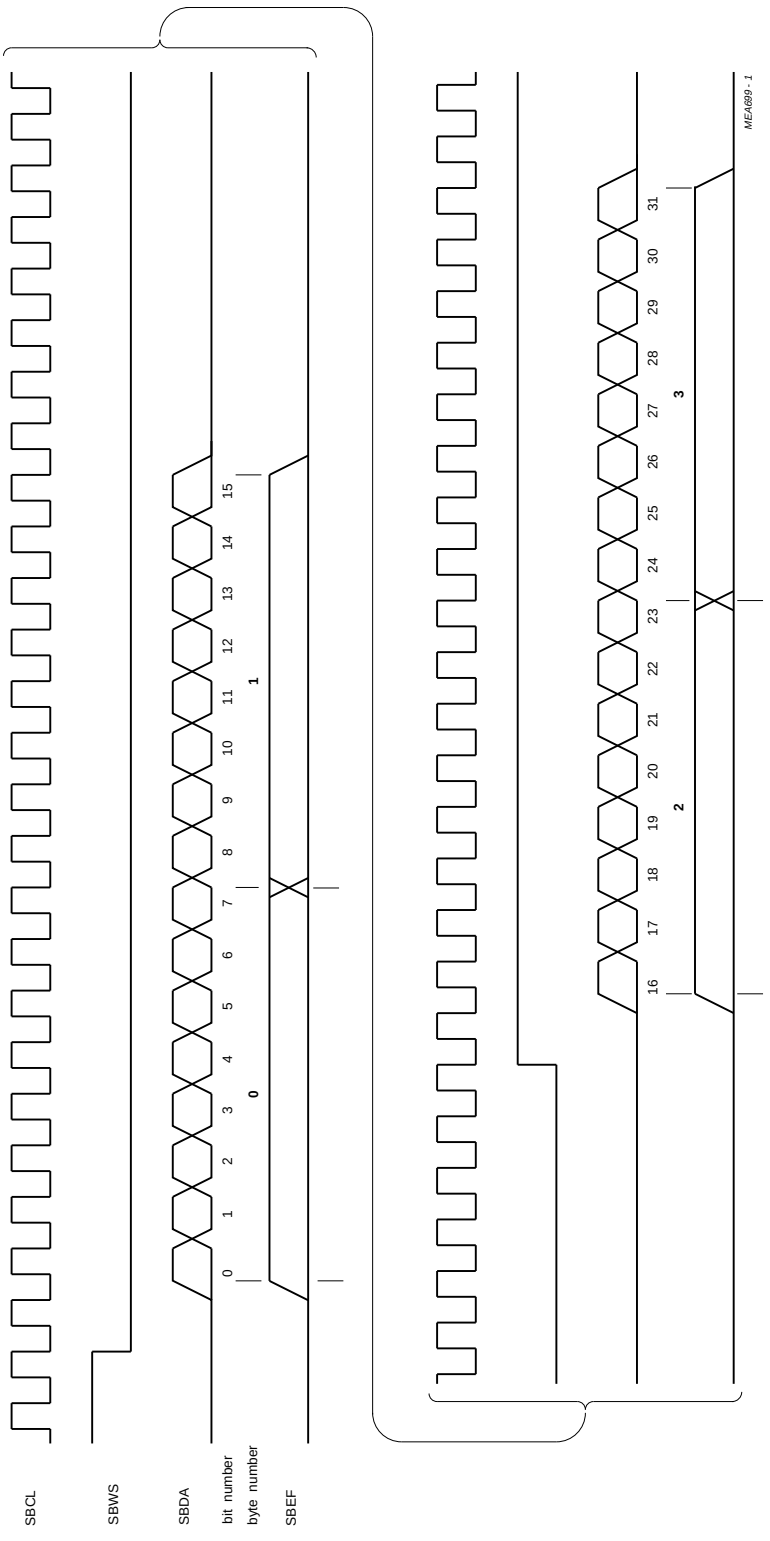


Fig.6 SB-I²S-interface in playback slave mode (1).

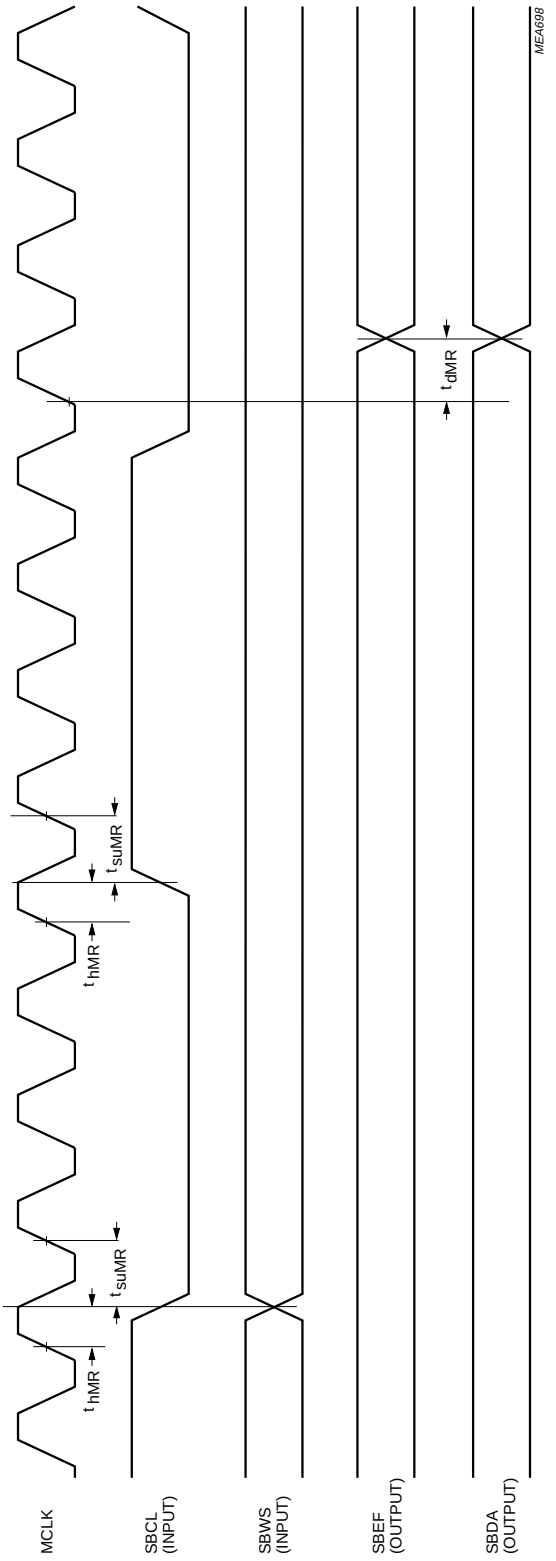


Fig.7 SB-I²S-interface in playback slave mode (2).

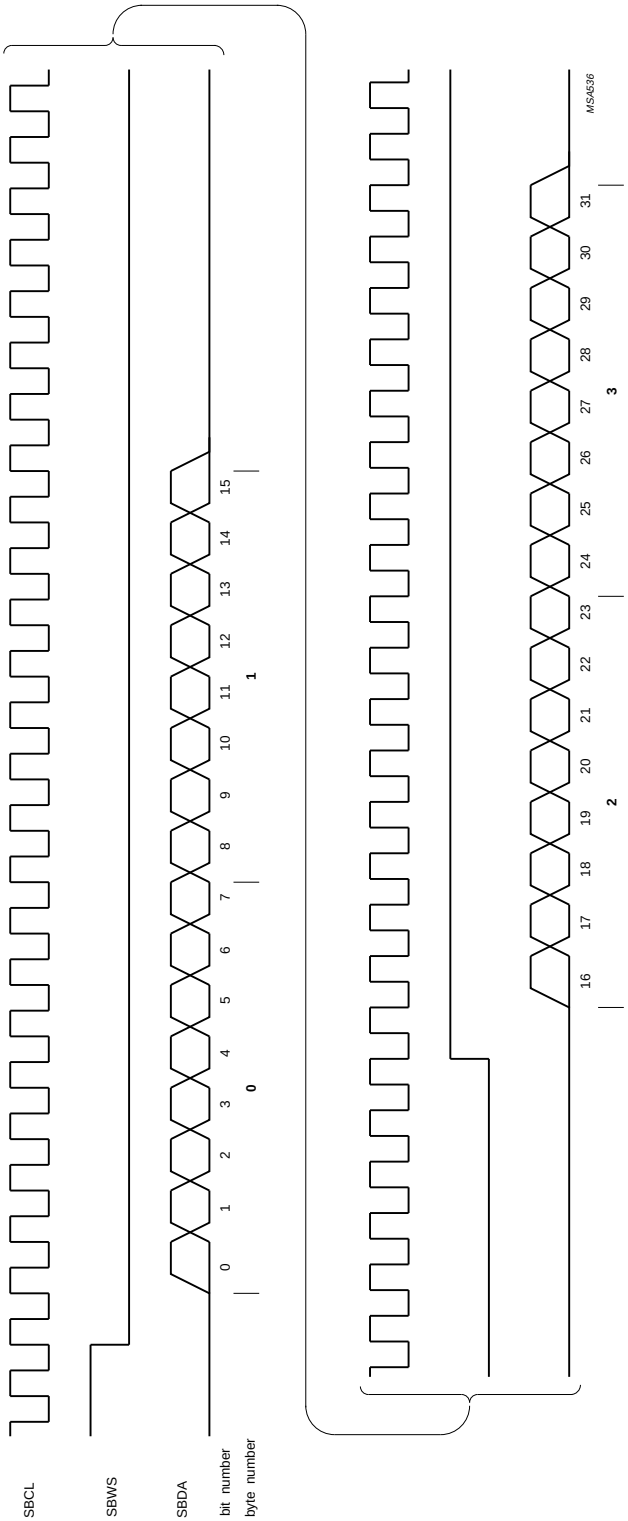


Fig.8 SB-I²S-interface in record mode (1).

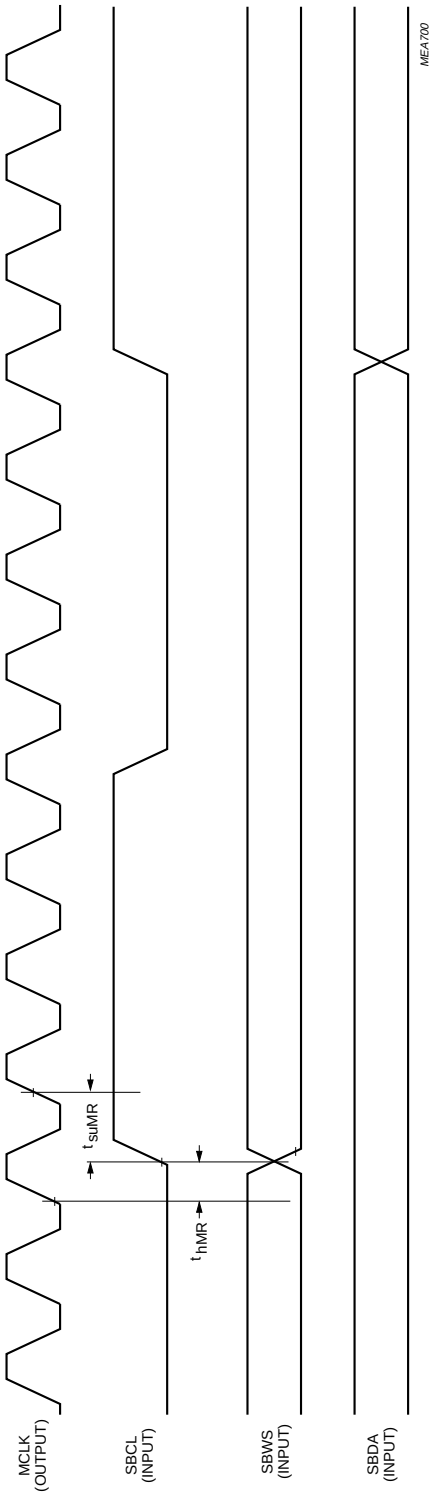


Fig.9 SB-I²S-interface in record mode (2).

SBMCLK

This is the sub-band master clock input for the SB-I^{2}S-interface. The frequency of this signal is nominally 6.144 MHz. This pin should be connected to the SBMCLK pin of the SAA2002.

SBDIR

This output pin is the sub-band I^{2}S-bus direction signal, it indicates the direction of transfer on the SB-I^{2}S-bus. A logic 1 indicates a SAA2022 to SAA2002 transfer (audio play) whilst a logic 0 is output for a SAA2002 to SAA2022 transfer (audio record). This pin connects directly to the SBDIR pin on the SAA2002.

SBCL

This input/output pin is the bit clock line for the SB-I^{2}S-interface to the SAA2002. Is has a nominal frequency of 768 kHz.

SBWS

This input/output pin is the word select line for the SB-I^{2}S-interface to the SAA2002. It has a nominal frequency of 12 kHz.

SBDA

This input/output pin is the serial data line for the SB-I^{2}S-interface to the SAA2002.

SBEF

This active HIGH output pin is the error per byte line for the SB-I^{2}S-interface to the SAA2002.

URDA

This active HIGH output pin indicates that the main data (audio), the SYSINFO and the AUXILIARY data are **not** usable, regardless of the state of the corresponding reliability flags. The state of this pin is reflected in the URDA bit of STATUS byte 0, which can be read by the microcontroller. This pin should be connected directly to the URDA pin of the SAA2002. URDA is activated as a result of a reset, a mode change from DRAR to DPAP, or if the SAA2022 has had to resynchronize with the incoming data from tape.

The position of the first SB-I^{2}S-bytes in a tape frame is shown in Fig.10.

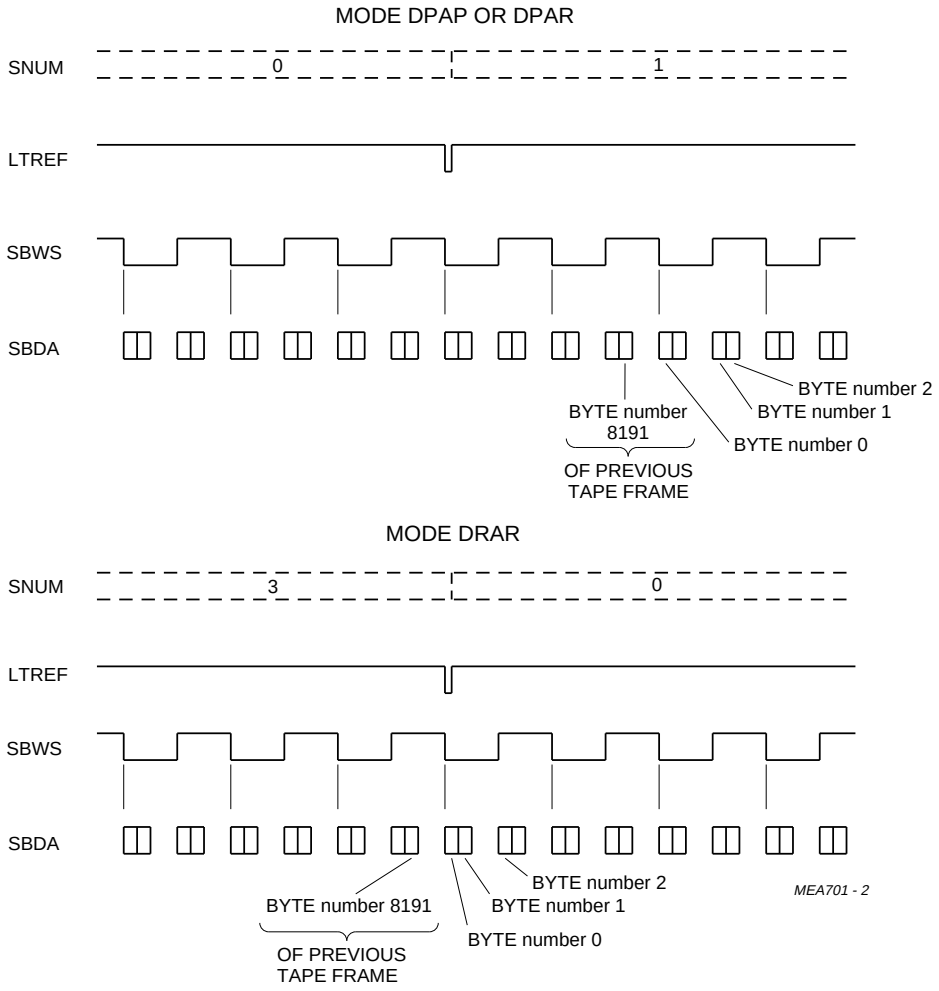


Fig.10 Position of first SB-I²S-bytes in tape frame.

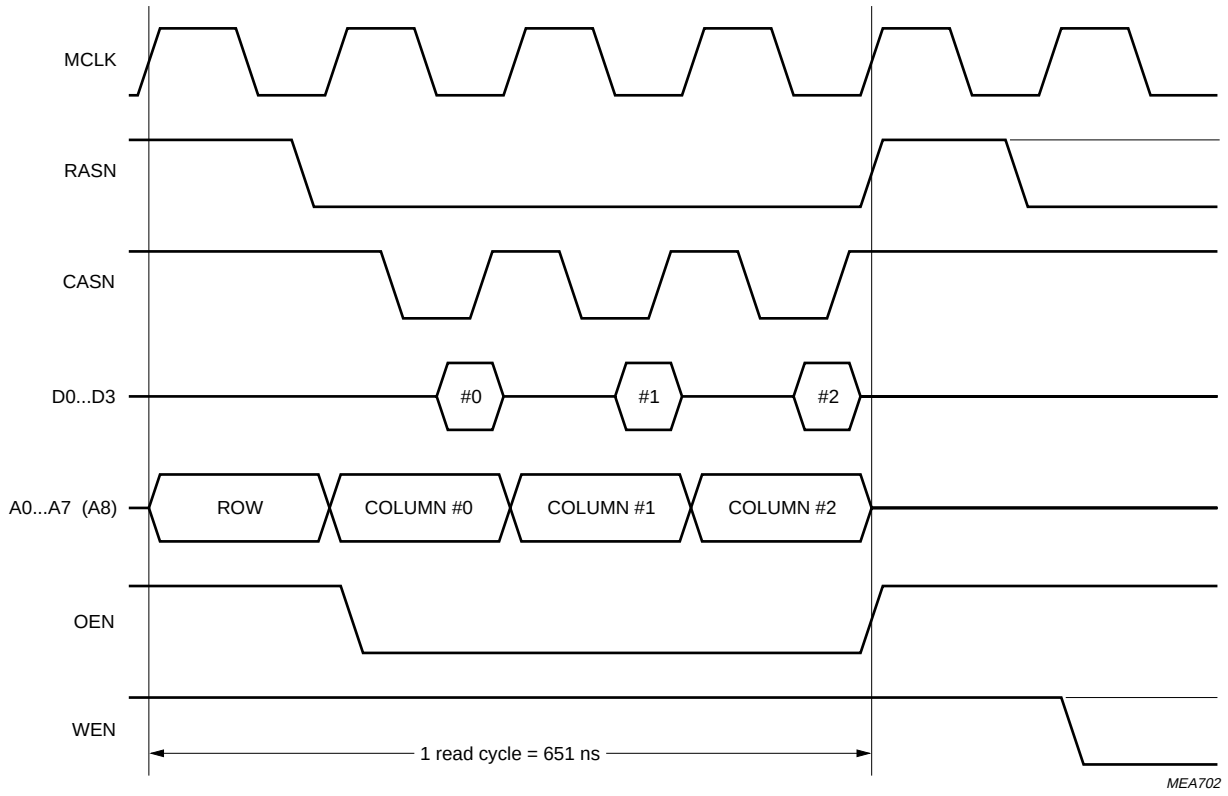


Fig.11 DRAM timing read cycle.

DRAM Interface

The SAA2022 has been designed to operate with 64 k × 4-bit or 256 k × 4-bit DRAMs operating in page mode, with an access time of 80 to 100 ns. The timing for read, write and refresh cycles is shown in Figs 11 to 13.

CASN

This output pin is the column address strobe (active LOW) for the DRAM, it connects directly to the column address strobe pin of the DRAM.

RASN

This output pin is the row address strobe (active LOW) for the DRAM, it connects directly to the row address strobe pin of the DRAM.

OEN

This pin provides the output enable (active LOW) for the DRAM, it connects directly to the output enable pin of the DRAM.

WEN

This output pin provides the write enable (active LOW) for the DRAM, it connects directly to the write enable pin of the DRAM.

A0 TO A8

These output pins are the multiplexed column and row address lines for the DRAM. When the 64 k × 4-bit DRAM is used, pins A0 to A7 should be connected to the DRAM address input pins, and pin A8 should be left unconnected. When using the 256 k × 4-bit DRAM then address pins A0 to A8 should be connected to the address input pins of the DRAM.

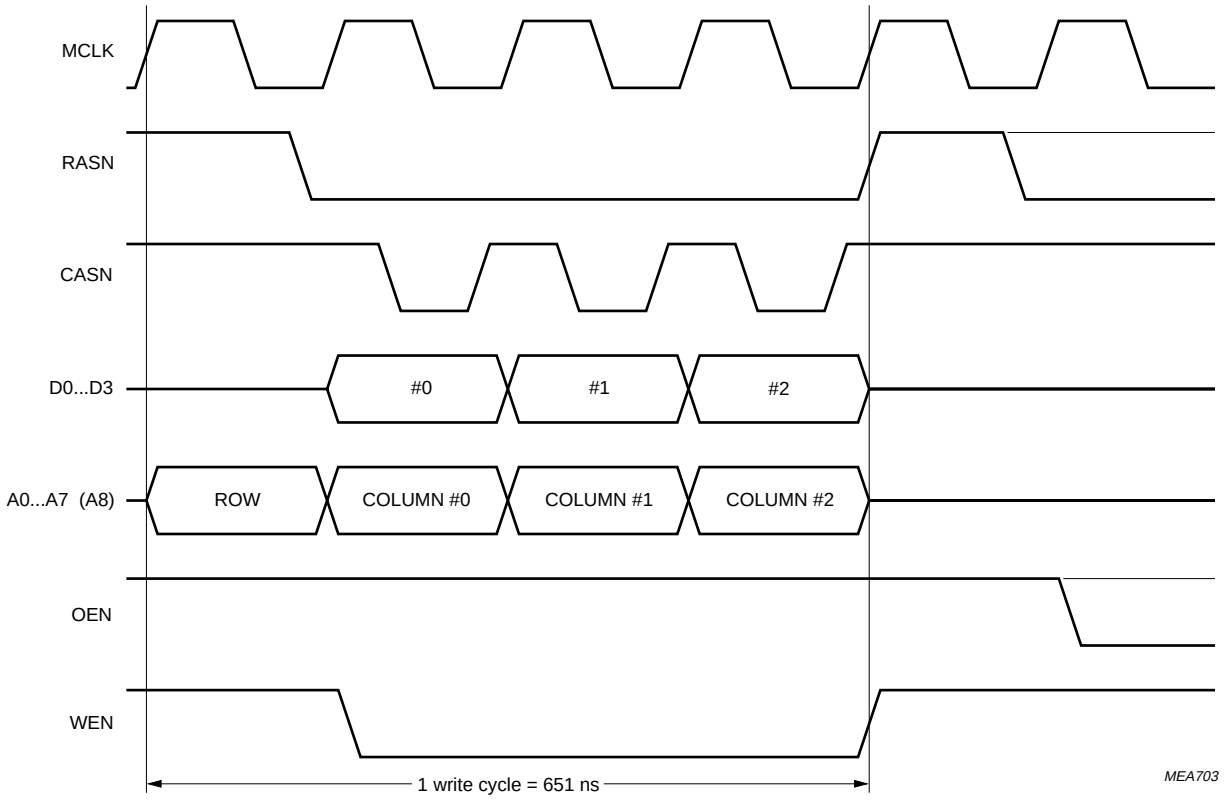


Fig.12 DRAM write cycle.

D0 TO D3

These input/output pins are the data lines for the DRAM, they should be connected directly to the DRAM data I/O pins.

Write amplifier interface

The SAA2022 may be used with either the TDA1316 or TDA1319 write amplifiers.

WCLOCK

This output pin provides the 3.072 MHz clock output for the WRITE AMPLIFIER, it should be connected directly to the WCLOCK pin of the WRITE AMPLIFIER.

WDATA

This output pin is the multiplexed data and control line for the WRITE AMPLIFIER (timing information is shown in Fig.14). The WDATA pin should be connected directly to the WDATA pin of the WRITE AMPLIFIER.

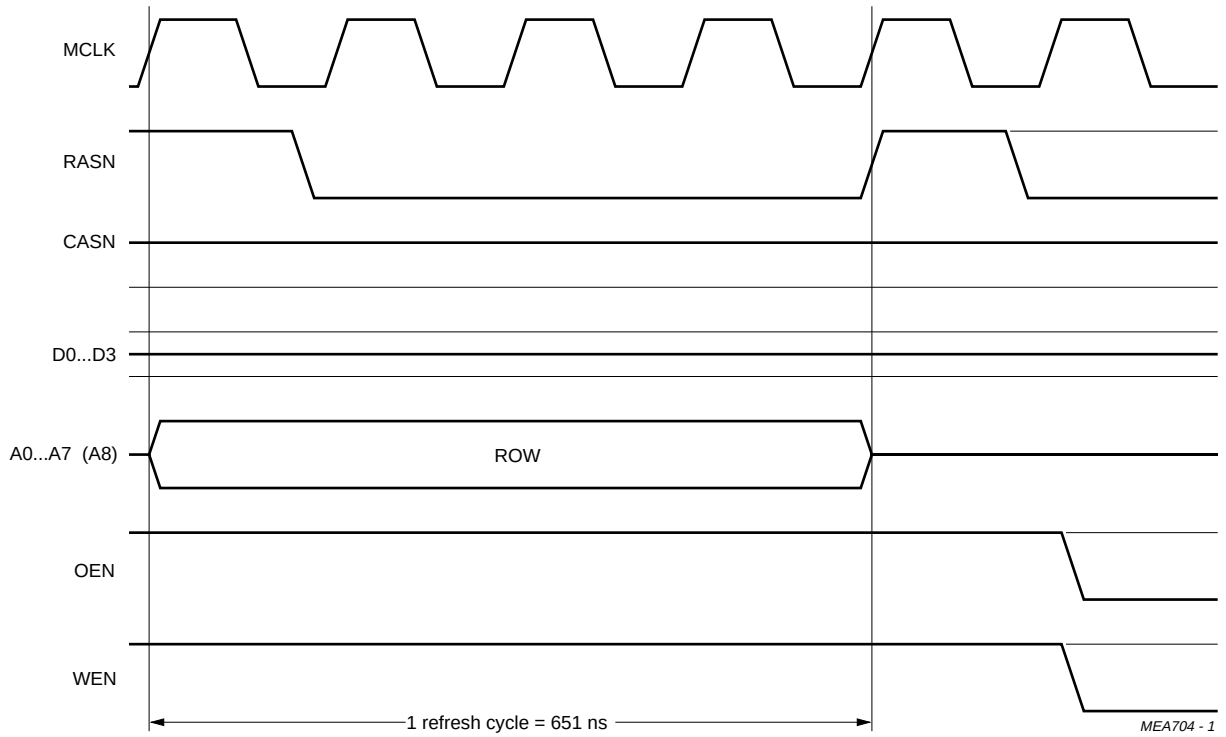


Fig.13 DRAM refresh cycle.

Tape deck capstan control interface

SPEED

This signal is a pulse width modulated output that may be used to control the tape deck capstan. The period of the SPEED signal is 41.66 µs and the nominal duty cycle is 50%.

There are 4 modes of operation for the SPEED signal which can be selected by the programmed settings of µCSPD (microcontroller capstan speed), ENFREG (enable frequency regulation) and ENEFREG (enable extended frequency regulation) flags.

SPDF

If µCSPD = logic 0 this pin outputs a pulse width modulated measurement of the main data channel bit rates and may be used in combination with the SPEED signal to control the tape deck capstan. The period of the SPDF signal is 5.2 µs. The duty cycle of SPDF can vary from 0% at +6.5% deviation to 100% at –6.5% deviation. If the deviation = 0% then the duty cycle of SPDF is 50%.

Microcontroller Interface

LTREF

The SAA2022 divides time into segments of 42.67 ms nominal duration which are counted in modulo 4. The LTREF active LOW output pin can be connected directly to the interrupt input of the microcontroller and indicates the start of a time segment. It goes LOW for 5.2 µs once every 42.66 ms and can be used for generating interrupts. Note if a resync occurs then the time between the occurrences of LTREF can vary. The function and programming of the other interface lines LTCNT0, LTCNT1, LTEN, LTCLK and LTDATA are described in the pinning and programming sections.

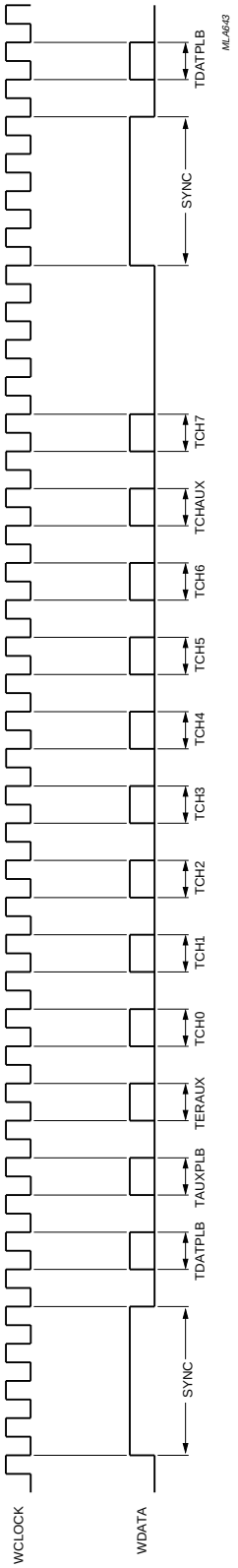


Fig.14 WDATA and WCLOCK timing.

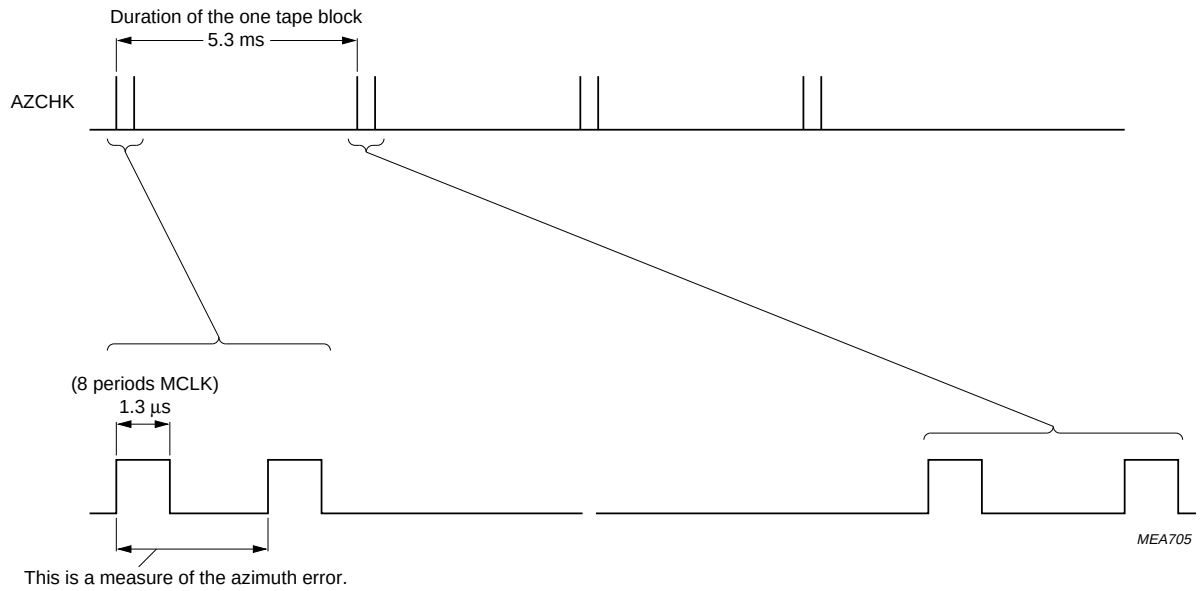


Fig.15 AZCHK timing.

Test Pins

TEST0, TEST1, TEST2 AND TEST 3

These input pins are for test use only and for normal operation should **not** be connected.

AZCHK

This output pin indicates the occurrence of a tape channel sync symbol on tape channels TCH0 and TCH7. The separation between the pulses for the TCH0 and TCH7 channels gives a measure of the azimuth error between the tape and head alignment (see Fig.15).

Port Expansion Pins

PINI

This input pin is connected directly to the PINI bit in the STATUS byte 1, it can be read by the microcontroller, and may be used for any CMOS level compatible input signals.

PINO1

This output pin is connected directly to the PINO1 bit of the SETTINGS byte 1 register and can be set or reset by the microcontroller.

PINO2

This output pin is connected directly to the PINO2 bit of the SETTINGS byte 1 register and can be set or reset by the microcontroller.

PINO3

This output pin is connected directly to the PINO3 bit of the SETTINGS byte 1 register and can be set or reset by the microcontroller.

Power Supply Pins

V_{DD1} TO V_{DD4}

These are the +5 V power supply pins which must all be connected. Decoupling of V_{SS1} to V_{SS4} is recommended.

V_{SS1} TO V_{SS4}

These are the +5 V power supply ground pins, all of which must be connected.

Programming the SAA2022 via the Microcontroller Interface

Table 1 SAA2022 interface connections to the microcontroller.

PIN	INPUT/OUTPUT	DESCRIPTION
LTEN	I	enable active HIGH
LTCLK	I	clock signal
LTCNT0	I	control LSB
LTCNT1	I	control MSB
LTDATA	I/O	bi-directional data
LTREF	O	timing reference 5 μs at start of every segment active LOW

All transfers are in units of 8-bits, registers with less than 8-bits are LSB justified, unless otherwise specified. The four basic types of transfer are shown in Table 2.

Table 2 Types of transfer.

LTCNT1	LTCNT0	TRANSFER	EXPLANATION
0	0	WDAT	write DATA to SAA2022
0	1	RDAT	read DATA from SAA2022
1	0	WCMD	write Command to SAA2022
1	1	RSTAT	read Status from SAA2022

Microcontroller Interface Registers

The SAA2022 microcontroller interface has 7 write and 4 read registers, as shown in Table 3.

Table 3 SAA2022 Microcontroller Interface Registers.

REGISTER	READ/WRITE	NO. OF BITS	COMMENTS
SET0	WRITE	7	primary settings
SET1	WRITE	8	secondary settings
CMD	WRITE	6	microcontroller command
BYTCNT	WRITE	8	byte counter
RACCNT	WRITE	7	random access counter
SPDDTY	WRITE	8	duty cycle for SPEED
AFLEV	WRITE	4	AUXILIARY flag level
STATUS0	READ	8	primary status
STATUS1	READ	7	secondary status
STATUS2	READ	8	SYSINFO/AUX flags
STATUS3	READ	8	channel status flags

Direct Access

Only one write (CMD) and four read (STATUS0 to STATUS3) registers can be directly accessed using the LTCNT lines, all other registers must be accessed by first programming the command register.

The four Status registers can be read by performing 4 RSTAT transfers within the same LTEN = HIGH period.

Indirect Access

To write to or read from the indirect access registers, a command must first be sent to the command register. The transfer of bytes can then occur using WDAT and RDAT type transfers. It is the responsibility of the microcontroller to ensure that the transfer type and the last command are compatible. The same type of transfer can continue until a new command is sent.

Typical transfers on the microcontroller interface are shown in Figs 16 to 19.

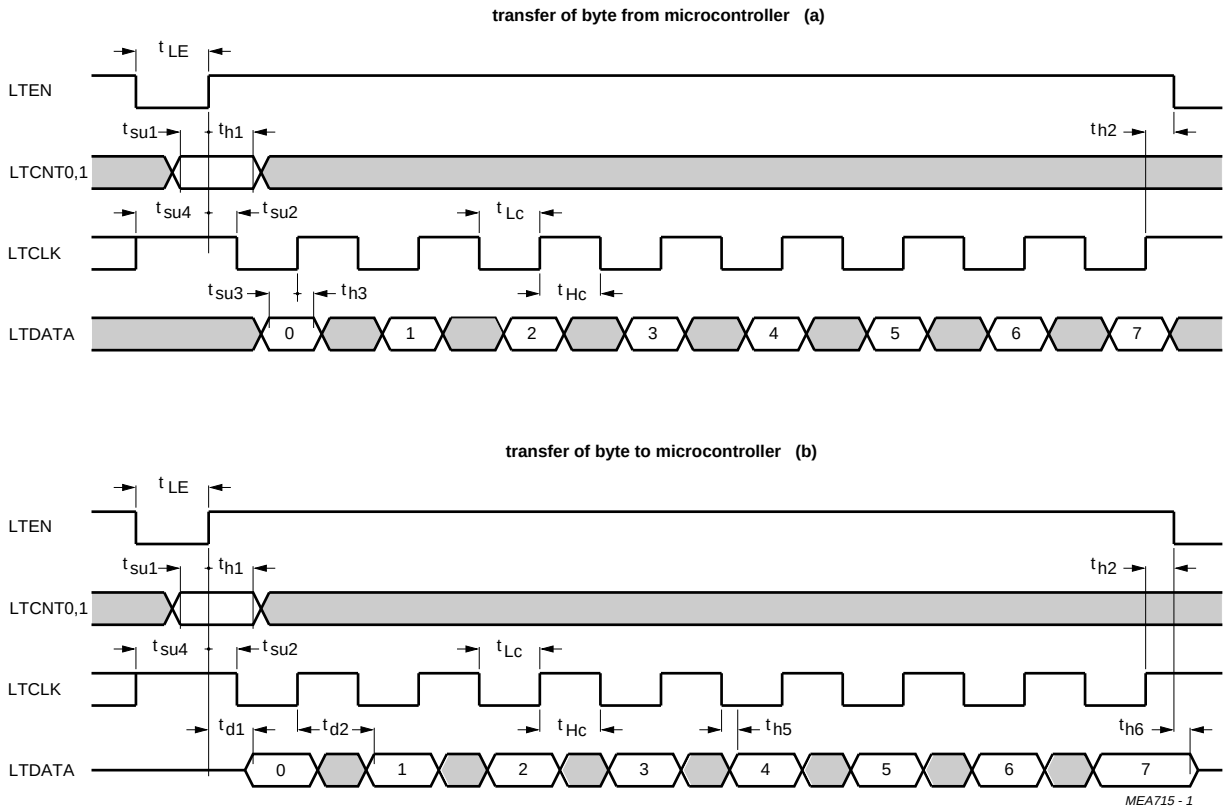


Fig.16 LT interface timing (1).

Notes to Fig.16a.

DESCRIPTION	TIMING
For the timing figures it is assumed that cycle time T_{cy} of MCLK is within the limits	160 ns < T_{cy} < 165 ns
The set-up time t_{su} of LTEN, LTCNT, LTCLK and LTDATA to MCLK HIGH	t_{su} < 40 ns
The hold time t_h of LTEN, LTCNT, LTCLK and LTDATA to MCLK HIGH	t_h = 0 ns
LTEN LOW time before start data transfer	t_{LE} > 535 ns; note 1
LTCLK LOW time	t_{Lc} > 205 ns
LTCLK HIGH time	t_{Hc} > 205 ns
LTCNT0/1 set-up time to LTEN HIGH	t_{su1} > 205 ns
LTCNT0/1 hold time to LTEN HIGH	t_{h1} > 205 ns
LTEN set-up time to LTCLK LOW	t_{su2} > 0 ns
LTEN hold time to LTCLK HIGH	t_{h2} > 205 ns
LTDATA set-up time to LTCLK HIGH	t_{su3} > 205 ns
LTDATA hold time to LTCLK HIGH	t_{h3} > 40 ns
LTCLK set-up time to LTEN HIGH	t_{su4} > 535 ns

Note

1. See interface timing (Fig.16b) for the transfer of a byte to the microcontroller.

Notes to Fig.16b.

DESCRIPTION	TIMING
For the timing figures it is assumed that cycle time T_{cy} of MCLK is within the limits	160 ns < T_{cy} < 165 ns
The set-up time t_{su} of LTEN, LTCNT, LTCLK and LTDATA to MCLK HIGH	t_{su} < 40 ns
The hold time t_h of LTEN, LTCNT, LTCLK and LTDATA to MCLK HIGH	t_h = 0 ns
The delay time t_d of LTDATA from MCLK HIGH is within the limits	0 ns < t_d < 30 ns
The delay time t_d of LTEN to the 3-state control of LTDATA	0 ns < t_d < 50 ns
LTEN LOW time before start data transfer	t_{LE} > 535 ns; note 1
LTCLK LOW time	t_{Lc} > 205 ns
LTCLK HIGH time	t_{Hc} > 205 ns
LTCNT0/1 set-up time to LTEN HIGH	t_{su1} > 205 ns
LTCNT0/1 hold time from LTEN HIGH	t_{h1} > 205 ns
LTEN set-up time to LTCLK LOW	t_{su2} > 0 ns
LTEN hold time from LTCLK HIGH	t_{h2} > 205 ns
LTCLK set-up time to LTEN HIGH	t_{su4} > 535 ns
LTCLK hold time from LTEN LOW	t_{h5} > 160 ns
LTDATA hold time from LTEN LOW	t_{h6} > 0 ns
LTDATA delay time from LTEN HIGH	t_{d1} < 235 ns
LTDATA delay time from LTCLK HIGH	t_{d2} < 400 ns
LTDATA delay time from LTEN (3-state control)	t_{d4} < 50 ns

Note

1. t_{LE} is determined by the longest path from LTEN LOW to LTDATA. This path is via the reset of the internal bit counter. This reset is only necessary when after the last LTEN = LOW, an exact multiple of 8-bits has not been transferred. Otherwise t_{LE} can be T_{cy} = 165 ns less.

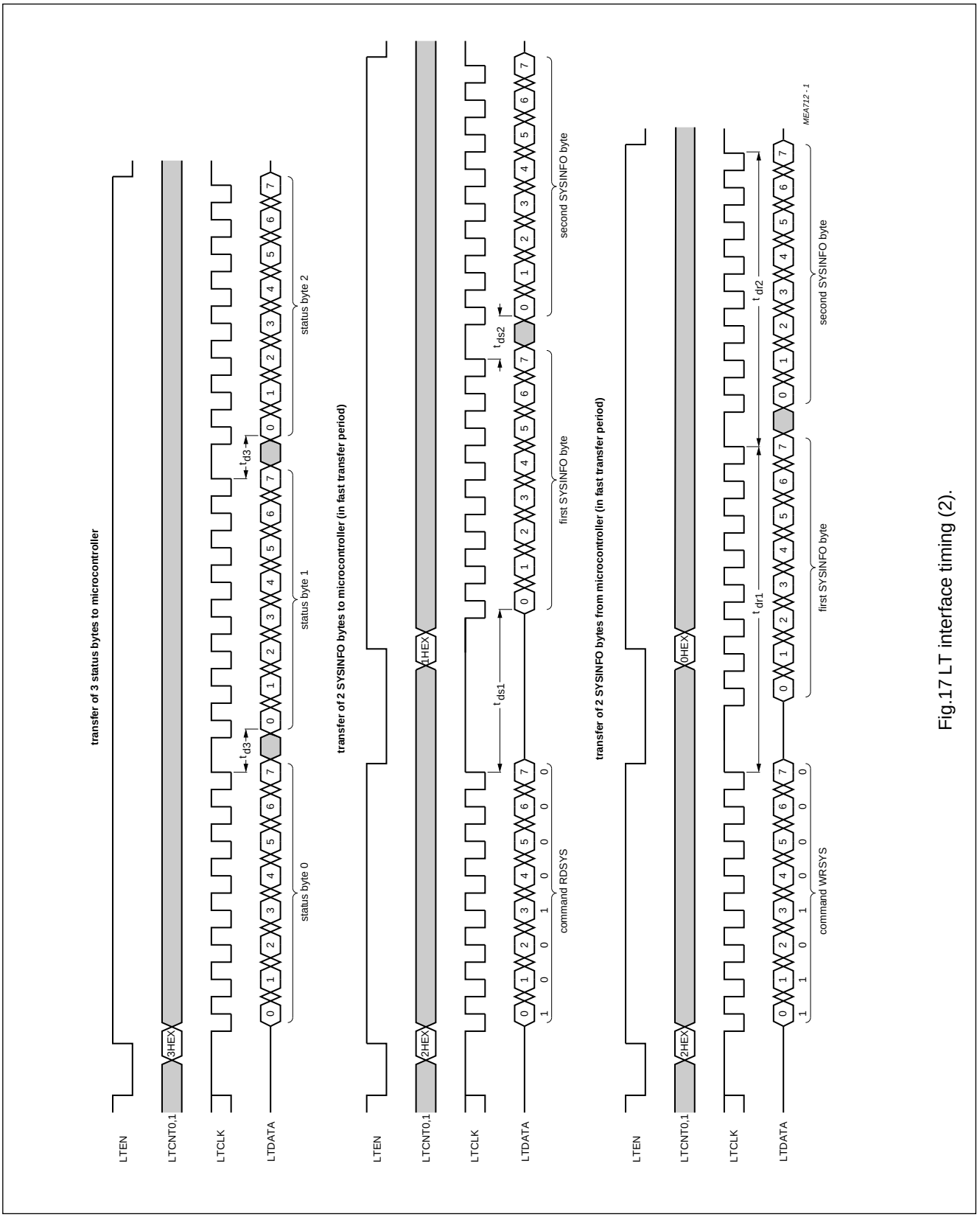


Fig.17 LT interface timing (2).

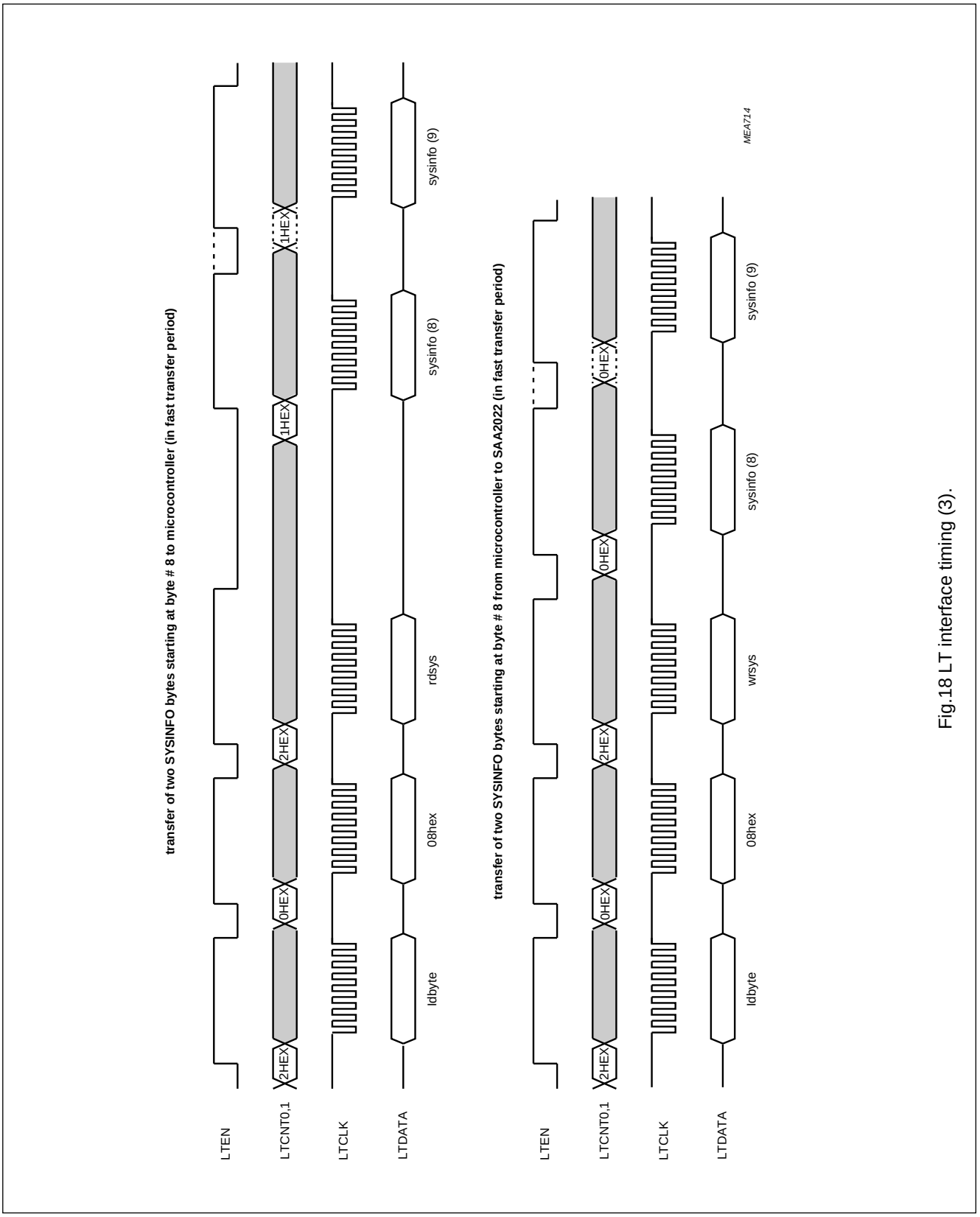


Fig.18 LT interface timing (3).

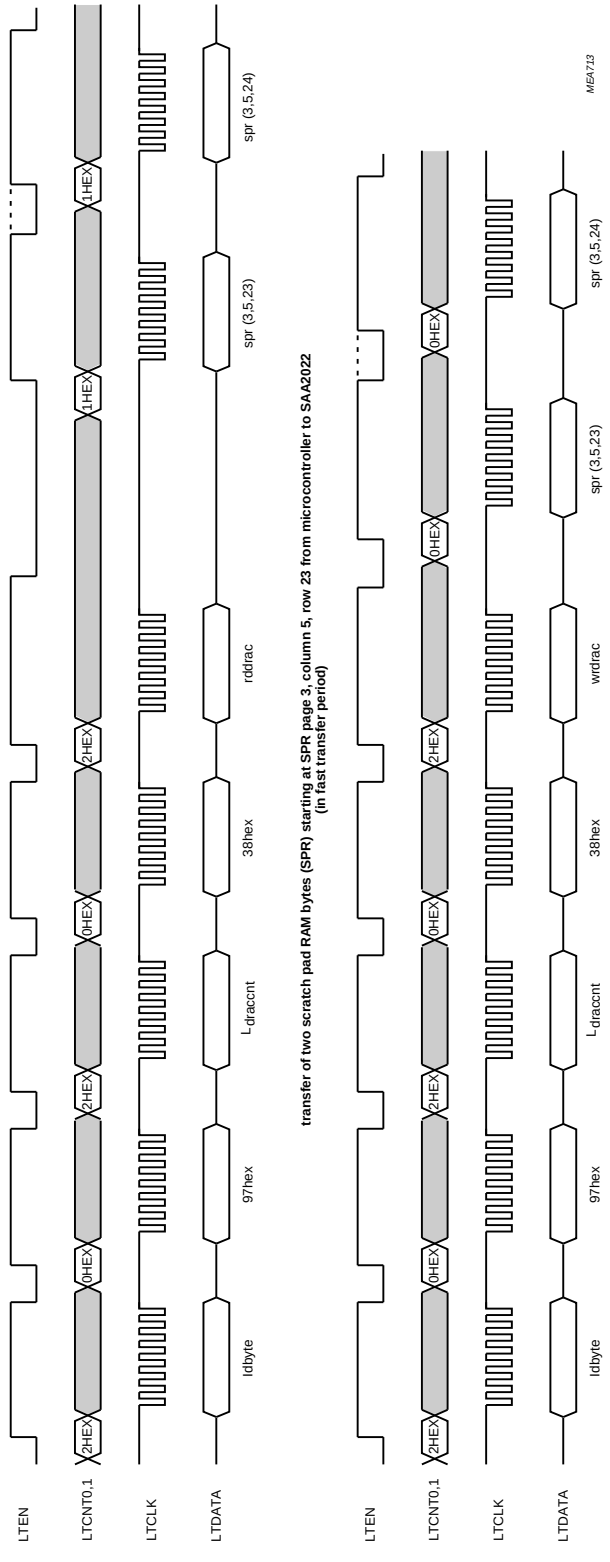


Fig.19 LT interface timing (4).

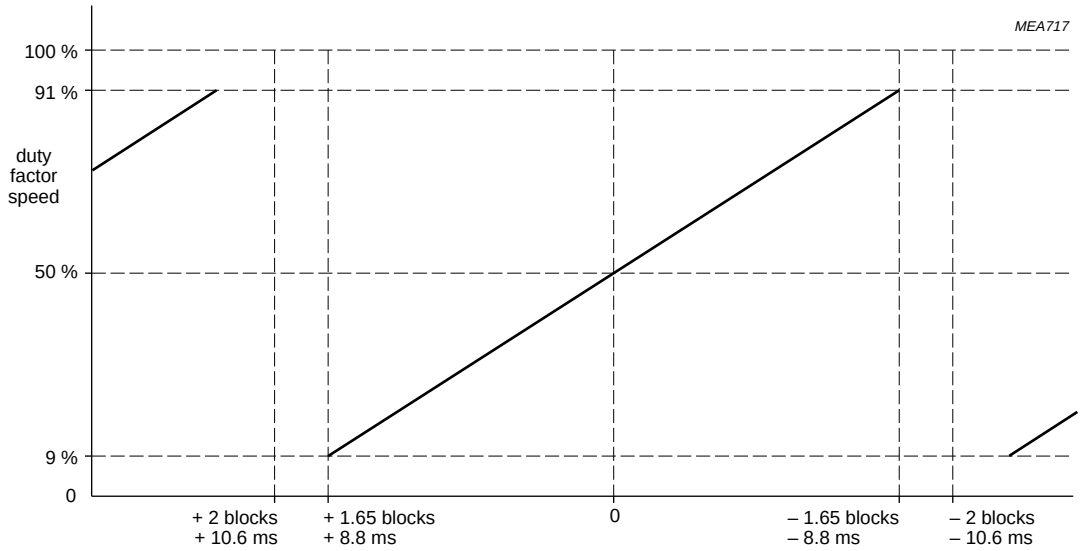


Fig.20 SPEED pulse width as a function of phase error.

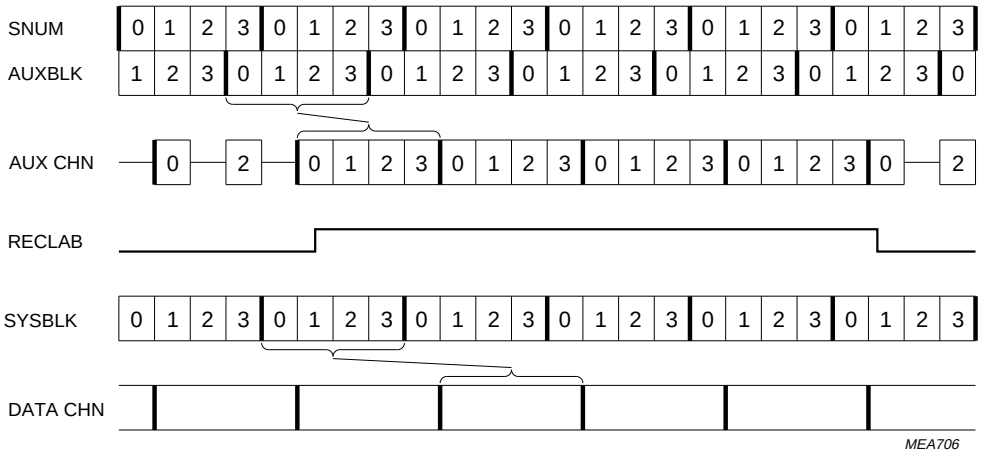


Fig.21 Recording a label.

Table 4 Microcontroller Interface Commands.

CMD REGISTER 76543210	COMMAND	EXPLANATION
XXXX1000	RDAUX	read AUXILIARY INFO
XXXX1001	RDSYS	read SYSINFO
XXXX1010	WRAUX	write AUXILIARY INFO
XXXX1011	WRSYS	write SYSINFO
XXXX0000	LDSET0	load new settings register 0
XXXX0001	LDSET1	load new settings register 1
XXXX0010	LDAFLEV	load AUX flag threshold level
XXXX0011	LDSPDDTY	load record speed duty cycle
XXXX0101	LDBYTCNT	load byte counter
XXXX0110	LDRACCNT	load random access counter
XXYZ1100	RDDRAC	read data in random access mode from RAM quarter YZ
XXYZ1101	RDFDRAC	read flag and data in random access mode from RAM quarter YZ
XXYZ1110	WRDRAC	write data in random access mode to RAM quarter YZ
XXYZ1111	WRFDRAC	write flag and data in random access mode to RAM quarter YZ

Explanation of settings

SET0 REGISTER (TABLE 6)

µCSPD

An active HIGH, selects microprocessor control for the SPEED pulse width modulated servo control signal.

DISRSY

Disable Resyncs active HIGH, is used in after recording.

RECLAB

Record labels active HIGH when in DRAR or DPAR modes; a label being defined as the bodies of all four AUX tape blocks in a tape frame which is being written. This setting has immediate effect and should only be modified in time segment 1.

ENFREG

In modes DPAP and DPAR Enable Frequency Regulation active HIGH, allows frequency information from the data channels to be used with the phase information to generate the capstan SPEED signal.

ENEFREG

Enable Extended Frequency Regulation active HIGH, allows extended frequency information from the data channels to be used with the “normal” frequency information and the phase information to generate the capstan SPEED signal, if ENFREG is active.

SET1 REGISTER (TABLE 7)

TEST1

This setting is for test only. For use in applications this bit should be always programmed to logic 0.

PINO1

Pin Output 1, Port expander output for the microcontroller.

TFEMAS

This allows the SAA2022 to become master of the SB-I^{2}S-bus in modes DPAP and DPAR. In mode DRAR the device always operates as a slave irrespective of the settings bit.

PORTAB

Portable application active HIGH, allows for the data channels clock extraction to track fast variations in tape bit rate. For home use set to inactive.

NOCOS

No Corrected Output Symbol active HIGH, disables the writing of the error corrected output to the DRAM. It is only used for debugging.

TEST2

This setting is for test only. For use in applications this bit should always be programmed to logic 0.

PINO2

Pin output 2, Port expander output for the microcontroller.

PINO3

Pin output 3, Port expander output for the microcontroller.

TAPE PHASE MODE

ENFREG = logic 0, ENEFREG = logic 0 and µCSPD = logic 0

In this mode the SAA2022 performs a new calculation to determine the pulse width for the SPEED signal approximately once every 21.33 ms, giving a sampling rate of approximately 46.9 Hz. This calculation is basically a phase comparison between the incoming main data tape frame and an internally generated reference. The pulse duty cycle increases linearly from approximately 9% when the incoming main data tape frame is 1.65 tape blocks (8.8 ms) too early up to 91% when the incoming main data tape frame is 1.65 tape blocks (8.8 ms) too late, in 256 steps (see Fig.20). Outside ±2 tape blocks range the pulse width characteristic overflows and repeats itself forming a saw-tooth pattern. The SAA2022 has an internal buffer of ±8.8 ms inside which the phase information is valid.

TAPE FREQUENCY MODE

ENFREG = logic 1, ENEFREG = logic 0 and µCSPD = logic 0

The above description is overridden with frequency information. That is if the incoming main data bit rate deviates by more than approximately ±6% from the nominal bit rate of 96000 bits per second, frequency information is mixed with the phase information. In between the limits ±6% the pulse width is determined as above.

EXTENDED TAPE FREQUENCY MODE

ENFREG = logic 1, ENEFREG = logic 1 and µCSPD = logic 0

In this mode there are 3 regions. This provides a more gentle transition from frequency plus phase control to phase only control. Firstly from 0% to ±4.5% deviation, where the operation is as for the tape phase mode. Secondly from ±4.5% to ±6% deviation where the contribution of the frequency information to the servo information is half of that in the region beyond ±6% deviation. Thirdly when the deviation is greater than ±6%, which is the same as for the tape frequency mode.

MICROCONTROLLER MODE

µCSPD = logic 1

In this mode the pulse width is determined by the microcontroller programming of the SPDDTY interface register.

NMODE0, NMODE1

These two bits control the mode change operation in the SAA2022.

Table 5 NMODE1, NMODE0.

NMODE1	NMODE0	OPERATING MODE
0	0	DPAP
1	0	DPAR
1	1	DRAR
0	1	invalid state

SETTINGS REGISTERS

Table 6 SET0.

SETTING	BIT	DEFAULT
ENEFREG	6	0
ENFREG	5	0
RECLAB	4	0
DISRSY	3	0
µCSPD	2	0
NMODE1	1	0
NMODE0	0	0

Table 7 SET1.

SETTING	BIT	DEFAULT
PINO3	7	0
PINO2	6	0
TEST2	5	0
NOCOS	4	0
PORTAB	3	1
TFEMAS	2	1
PINO1	1	0
TEST1	0	0

Table 8 SPEED Source.

MODE	µCSPD	SPEED
DPAP	0	tape(1)
DPAP	1	µC(2)
DPAR	0	tape(1)
DPAR	1	µC(2)
DRAR	0	50%(3)
DRAR	1	µC(2)

Notes

1. “Tape” means that the duty cycle has been calculated from the playback tape signal.
2. “µC” means that the microcontroller programs the duty cycle via the SPDDTY register in the microcontroller interface.
3. “50%” defines that the duty cycle is fixed at 50%.

Table 9 Typical Settings.

SETTING BYTE																WHEN
0								1								
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	
X	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	play home machine
X	1	1	0	0	0	0	0	0	0	0	0	1	1	0	0	play portable machine
X	X	X	0	X	0	1	1	0	0	0	0	0	1	0	0	record NO LABEL
X	X	X	1	X	0	1	1	0	0	0	0	0	1	0	0	record LABEL
X	X	X	0	1	1	1	0	0	0	0	0	0	1	0	0	after record NO LABEL
X	X	X	1	1	1	1	0	0	0	0	0	0	1	0	0	after record LABEL

STATUS REGISTERS

The SAA2022 has 4 status registers all of which are read only. A circular pointer is used to select which of the status registers is addressed. This pointer is reset to point to STATUS0 as result of the rising edge of LTEN while the LTCNT0/1 = RSTAT. Any number of the registers may be read, always starting at STATUS0.

Table 10 STATUS0.

STATUS BIT	BIT
RFBT	7
SYSFLC	6
AUXFLC	5
AUXFLO	4
FLAGI	3
URDA	2
SNUM1	1
SNUM0	0

Table 11 STATUS1.

STATUS BIT	BIT
SLOWTFR	7
TEST4	6
–	5
PINI	4
PAG2	3
PAG1	2
MODE1	1
MODE0	0

Table 12 STATUS2.

STATUS BIT	BIT
NFLG3	7
NFLG2	6
NFLG1	5
NFLG0	4
FLG3	3
FLG2	2
FLG1	1
FLG0	0

Table 13 STATUS3.

STATUS BIT	BIT
CHANS7	7
CHANS6	6
CHANS5	5
CHANS4	4
CHANS3	3
CHANS2	2
CHANS1	1
CHANS0	0

SNUM0, SNUM1

Time segment number.

URDA

Unreliable Data active HIGH, means that regardless of the other flag information **you cannot use the Data, SYSINFO or AUX, because they are unreliable**, this can occur as result of a RESYNC, a mode change from mode DRAR to mode DPAP, or a reset of the SAA2022. When a resync occurs it resynchronizes with the incoming main data tape channel information, with a result that for a period of time, the time that URDA is HIGH all output data is unusable.

FLAGI

Instantaneous flag active HIGH, indicates that the AUXILIARY byte that is about to be transferred to the microcontroller has a flag that is ≥ AFLEV, or that the SYSINFO byte that is about to be transferred is in error.

AUXFLO

Old Aux Flag active HIGH, indicates that AUXILIARY data due to be transferred to the microcontroller in the current segment should not be used.

AUXFLC

AUX Flag active HIGH, indicates that at least one of the AUXILIARY data bytes due to be transferred to the microcontroller in the current segment is in error. This information is provided before the transfer occurs.

SYSFLC

SYSINFO flag active HIGH, indicates that at least one of the SYSINFO bytes in the current segment is in error. This information is provided before the transfer occurs.

RFBT

Ready for byte transfer of SYSINFO, AUX or Scratch pad RAM to or from the microcontroller active HIGH.

MODE0, MODE1

Current mode of operation of the SAA2022.

PAG1, PAG2

Two most significant bits of the modulo 6 internal page counter, the least significant bit is equal to SNUM0.

PINI

Pin input, Port expander input for the microcontroller.

TEST4

This is for test purposes only.

SLOWTFR

Indicates that LT data transfers of SYSINFO, AUX or Scratch Pad RAM can only occur at low speed rate. This occurs only during the second half of time segment 0, therefore the status bit RFBT must be polled to see if a transfer is possible. This bit will be HIGH only during the second half of time segment 0.

FLG 0 to 3

Error flag from the next AUXILIARY/SYSINFO byte which is to be transferred to the microcontroller.

The flags for SYSINFO bytes have only 2 values, logic 0 which implies that the error corrector finds the bytes are good and logic 1 which implies that the bytes are in error.

The flags for AUXINFO bytes can have any one of 16 values, 0 to 15, depending on the type of correction. All of the AUX bytes in the same AUX code word will have the same flag value. The less reliable the data, the higher the flag value. It is recommended that any byte with a flag value of 10 or higher is deemed unreliable.

NFLG 0 to 3

Error flag from the byte after the next AUXILIARY/ SYSINFO byte which will be transferred to the microcontroller.

CHANS 0 to 7

Error Correction Channel status, which indicates if the even C1 code words in the 5th block of the segment for each data tape channel were non correctable. Therefore 1 in every 16 C1 code words from each channel is monitored to see if the C1 error correcting decoding was successful.

Loadable registers

Table 14 AFLev.

3	2	1	0	BIT
1	0	1	0	default value

AUX Flag threshold level. FLAGI goes HIGH for the AUX bytes whose flags are ≥ AFLev. AUXFLC will go HIGH if the flags from either code word in the current segment are ≥ AFLev. The default value is 10.

Table 15 SPDDTY.

7	6	5	4	3	2	1	0	BIT
1	0	0	0	0	0	0	0	default value

SPEED duty cycle register. If μCSPD is active, this register determines the duty cycle of the speed signal.

The duty cycle is given by:

$$Duty\ cycle = \frac{SPDDTY \times 100}{256}\ \%$$

- 0 for 0% duty cycle
- 128 for 50% duty cycle
- 255 for 99.6% duty cycle.

The default value is 128.

Table 16 BYTCNT.

7	6	5	4	3	2	1	0	BIT
0	0	0	0	0	0	0	0	default value

Byte counter for SYSINFO, AUX and Scratch Pad RAM transfers. For SYSINFO:

values 0 to 31 access SYSINFO from the current segment.

values 32 to 63 access SYSINFO from the current +1 segment.

values 64 to 95 access SYSINFO from the current +2 segments.

values 96 to 127 access SYSINFO from the current +3 segments.

In Random access mode the SYSTEM ADDRESS is mapped on to BYTCNT as follows:

Table 17 SYSTEM ADDRES in Random access mode.

7	6	5	4	3	2	1	0	BYTCNT
7	6	5	4	3	2	1	0	ROW

Table 18 RAACNT.

6	5	4	3	2	1	0	BIT
0	0	0	0	0	0	0	default value

Random Access counter is used for generating addresses in the Random access mode, the SYSTEM ADDRESS is mapped on to RACCNT as shown in Table 19.

Table 19 SYSTEM address.

6	5	4	3	2	1	0	RACCNT
–	–	–	–	–	–	8	ROW
–	–	–	2	1	0	–	COL
2	1	0	–	–	–	–	PAG

SYSINFO AND AUX DATA OFFSETS

AUX data consists of 4 blocks of 36 bytes, one block being transferred in each time segment.

Each tape frame contains 128 bytes of SYSINFO, the SYSINFO bytes can for convenience, be considered as being grouped into 4 SYSINFO blocks, with:

SYSBlk0 ==> SI0 to SI31,

SYSBlk1 ==> SI32 to SI63, etc.

In modes DPAP and DPAR SYSINFO transfers may occur in two ways:

1. 4 blocks of 32 bytes, one block being transferred from the SAA2022 in each time segment.
2. 1 block of 128 bytes being transferred in time segment 1.

In mode DRAR SYSINFO must be transferred to the SAA2022 as 4 blocks of 32 bytes, one block in each segment.

Figures 26 to 29 show the offsets between the SYSINFO and AUX and the time segment counter, for the various modes of operation of the SAA2022.

BLOCK OFFSETS WITH RESPECT TO TIME SEGMENT

Mode DPAP

SYSBlk = (SNUM + 3) MOD 4;
or read all 4 SYSINFO blocks when SNUM = 1.

If AUX and MAIN were recorded simultaneously then AUXBlk = (SNUM + 1) MOD 4; else read and interpret 1 AUX block in each time segment.

Mode DRAR

SYSBlk = SNUM;
AUXBlk = (SNUM + 1) MOD 4.

Mode DPAR

SYSBlk = (SNUM + 3) MOD 4;
or read all 4 SYSINFO blocks when SNUM = 1;
AUXBlk = (SNUM + 1) MOD 4.

THE SCRATCH PAD RAM

The SAA2022 provides the microcontroller with a scratch pad RAM, which it can use for any purpose. The size of the scratch pad depends upon the size of the DRAM used and the locations may be written and read in 8-bit or 12-bit units.

For a 64 k $\times$ 4-bit DRAM, the scratch pad is arranged as 6 pages, where each page consists of 7 columns $\times$ 64 rows. The pages are numbered 0 to 5, columns 1 to 7 and rows 0 to 63. This gives a total of $(6 \times 7 \times 64) = 2688$ locations.

For a 256 k $\times$ 4-bit DRAM, the scratch pad is the same as for the 64 k $\times$ 4 bit DRAM, plus an additional 3 RAM quarters, each of 6 pages where each page consists of 8 columns $\times$ 448 rows. The pages are numbered 0 to 5, columns 0 to 7 and rows 0 to 431. This gives then a total of $(2688 + (3 \times 6 \times 8 \times 448)) = 67200$ locations. The RAM quarter is chosen by the YZ bits of the microcontroller interface commands.

Use of the scratch pad RAM outside the above ranges will upset the operation of the device.

As with SYSINFO, AUX transfers can occur at high-speed at all times except the second half of time segment 0, that is when the status bit SLOWTFR is HIGH. During this period the microcontroller must poll the status bit RFBT to determine when a transfer can occur.

There are two possible methods for addressing the scratch pad RAM. For random access of the scratch pad the address of each location is sent by the microcontroller to the SAA2022 before each location transfer. Alternatively, the address of the first location can be sent by the microcontroller before the first location transfer. This will automatically increment the row for all subsequent transfers until the end of the column. The RACCNT and BYTCNT registers are used for addressing the scratch pad. For the 64 k $\times$ 4-bit DRAM, and first quarter of 256 k $\times$ 4 DRAM the mapping of the scratch pad RAM address onto the RACCNT and BYTCNT registers is shown in Tables 20 and 21. For the other three-quarters of the 256 k $\times$ 4 DRAM the mapping of the scratch pad RAM address onto the RACCNT and BYTCNT registers is shown in Tables 22 and 23.

Table 20 RACCNT bit.

RACCNT BIT						
6	**5**	**4**	**3**	**2**	**1**	**0**
P2	P1	P0	C2	C1	C0	1

Table 21 BYTCNT bit.

BYTCNT BIT							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
1	0	R5	R4	R3	R2	R1	R0

Table 22 RACCNT bit.

RACCNT BIT						
6	**5**	**4**	**3**	**2**	**1**	**0**
P2	P1	P0	C2	C1	C0	R8

Table 23 BYTCNT bit.

BYTCNT BIT							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R7	R6	R5	R4	R3	R2	R1	R0

Mode changes

Table 24 Possible mode changes for the SAA2022.

CURRENT MODE	NEW MODE		
	DPAP	**DRAR**	**DPAR**
DPAP	–	YES	YES
DRAR	YES	–	–
DPAR	YES	–	–

TIMING FOR MODE CHANGES

Mode change DPAP to DRAR

This mode change occurs at the end of the time segment in which the SAA2022 receives the new settings. Writing of the first MAIN and AUX data commences at the start of the time segment 1 which follows two subsequent end of time segment 3 intervals. The delay to writing to tape is approximately 222 ms, as shown in Fig.22. If “seamless appending” is required the new settings should be sent to the SAA2022 during time segment 2.

Mode change DPAP to DPAR

This mode change occurs at the first end of time segment 2 after the SAA2022 receives the new settings. Output of AUX to tape begins at the start of the following time segment 1, (i.e. ≈85.3 ms after the mode change), as shown in Fig.23.

Mode change DRAR to DPAP

This mode change occurs at the first end of time segment 0 after the SAA2022 receives the new setting. Writing of MAIN and AUX data stops immediately after the mode change. The time segment jumps back to 0, URDA goes HIGH and stays HIGH for 5 time segments (≈213.3 ms) after which it goes LOW, as shown in Fig.24.

Mode change DPAR to DPAP

This mode change occurs at the first end of time segment 0 after the SAA2022 receives the new setting. The writing of AUX data to tape stops immediately after the mode change. The first AUX read from tape can be expected during the following time segment 0 or 1 (i.e. 128 to 170.67 ms after the mode change), as shown in Fig.25.

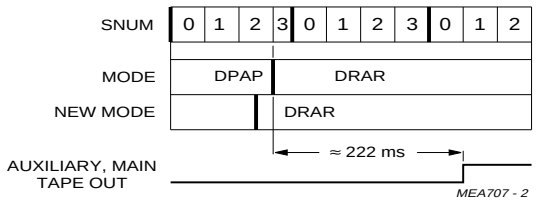


Fig.22 Mode change DPAP to DRAR (AUX and MAIN simultaneously recording).

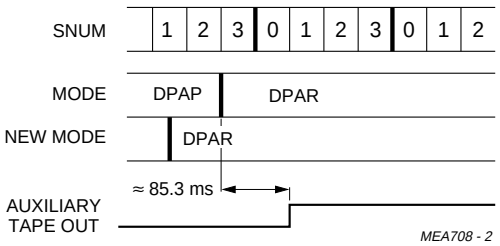


Fig.23 Mode change DPAP to DPAR (AUX after recording).

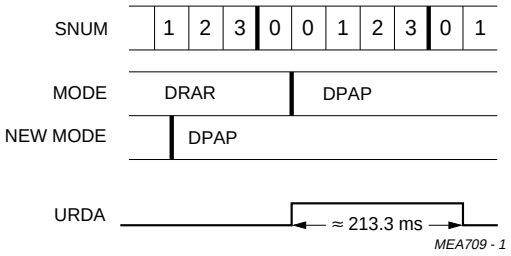


Fig.24 Mode change DRAR to DPAP.

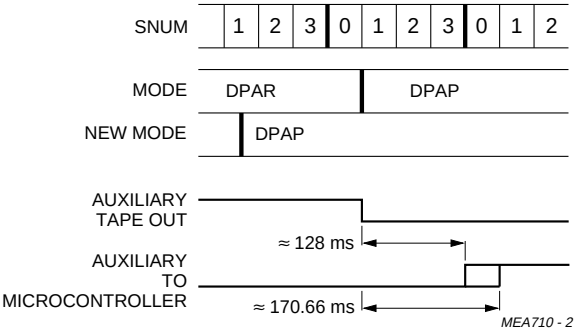


Fig.25 Mode change DPAR to DPAP.

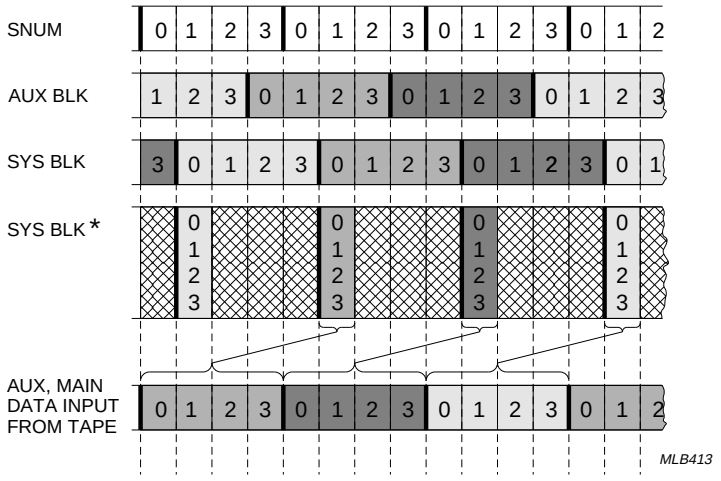


Fig.26 SYSINFO and AUX block delays in DPAP (Audio and AUX simultaneously recorded).

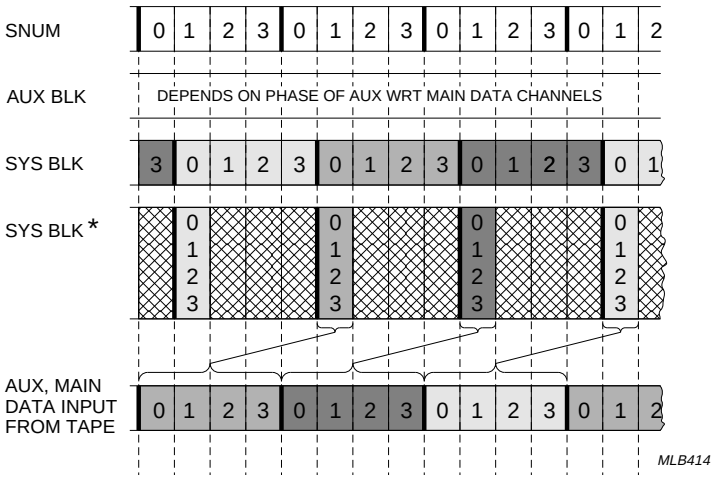


Fig.27 SYSINFO and AUX block delays in mode DPAP (Audio and AUX recorded separately).

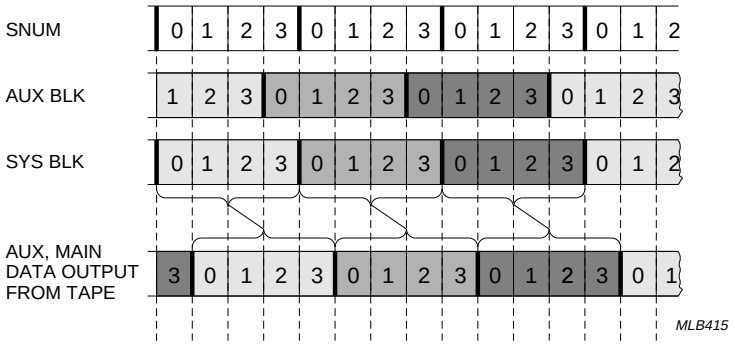


Fig.28 SYSINFO and AUX block delays in mode DRAR.

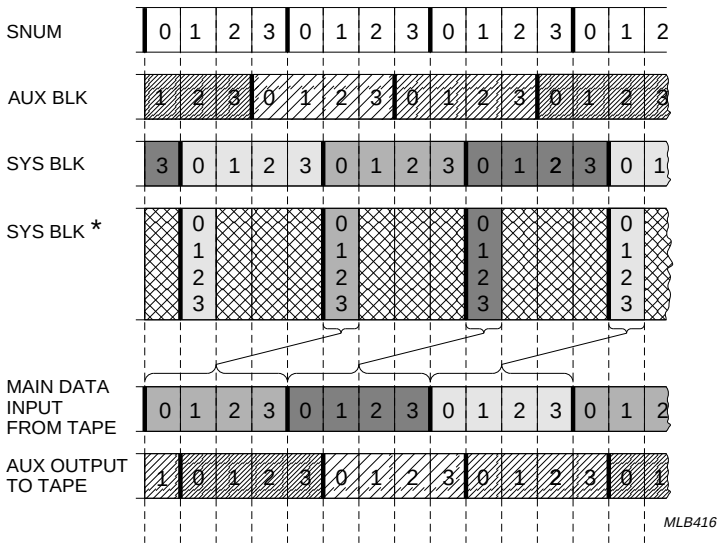


Fig.29 SYSINFO and AUX block delays in mode DPAR.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		–0.5	+6.5	V
V_I	input voltage	note 1	–0.5	V_{DD} + 0.5	V
I_{SS}	supply current in V_{SS}		–	–100	mA
I_{DD}	supply current in V_{DD}		–	100	mA
I_I	input current		–10	+10	mA
I_O	output current		–20	+20	mA
P_{tot}	total power dissipation		–	500	mW
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		–40	+85	°C
V_{es1}	electrostatic handling	note 2	–1500	+1500	V
V_{es2}	electrostatic handling	note 3	–70	+70	V

Notes

1. Input voltage should not exceed 6.5 V unless otherwise specified.
2. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.
3. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

DC CHARACTERISTICS

V_{DD} = 3.8 to 5.5 V; T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage	note 1	3.8	5.0	5.5	V
I_{DD}	supply current	V_{DD} = 5 V	–	21	30	mA
		V_{DD} = 3.8 V	–	16	25	mA
Inputs CLK24, TCH0 to TCH7, TAUX, PWRDWN, LTCLK, LTCNT0, LTCNT1, LTEN, PINI and SBMCLK						
V_{IL}	LOW level input voltage		–	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	–	V
I_I	input current	V_I = 0 V; T_{amb} = 25 °C	–	–	–10	µA
		V_I = 5.5 V; T_{amb} = 25 °C	–	–	10	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input RESET						
V_{tLH}	threshold voltage LOW-HIGH		$0.8V_{DD}$	–	–	V
V_{tHL}	threshold voltage HIGH-LOW		–	–	$0.2V_{DD}$	V
V_{hys}	hysteresis	$V_{tLH} - V_{tHL}$	–	1.5	–	V
I_I	input current	$V_I = V_{DD}$	25	–	400	µA
Outputs RASN, CASN, WCLOCK and WDATA						
V_{OL}	LOW level output voltage	I_O = –3 mA	–	–	0.4	V
V_{OH}	HIGH level output voltage	I_O = 3 mA	$V_{DD} - 0.5$	–	–	V
Outputs LTREF, WEN, OEN, A0 to A8, SPEED, SPDF, PINO1, PINO3, AZCHK, TEST2, TEST3, MCLK, SBEF, SBDIR and URDA						
V_{OL}	LOW level output voltage	I_O = –2 mA	–	–	0.4	V
V_{OH}	HIGH level output voltage	I_O = 2 mA	$V_{DD} - 0.5$	–	–	V
Inputs/outputs D0 to D3; with outputs in 3-state						
V_{IL}	LOW level input voltage	TTL-level	–	–	0.8	V
V_{IH}	HIGH level input voltage	TTL-level	2	–	–	V
I_I	input leakage current	V_I = 0 V; T_{amb} = 25 °C	–	–	–10	µA
		V_I = 5.5 V; T_{amb} = 25 °C	–	–	10	µA
Inputs/outputs D0 to D3						
V_{OL}	LOW level output voltage	I_O = –3 mA	–	–	0.4	V
V_{OH}	HIGH level output voltage	I_O = 3 mA	$V_{DD} - 0.5$	–	–	V
Inputs/outputs LTDATA, SBCL, SBDA and SBWS; with outputs in 3-state						
V_{IL}	LOW level input voltage	TTL-level	–	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage	TTL-level	$0.7V_{DD}$	–	–	V
I_I	input leakage current	V_I = 0 V; T_{amb} = 25 °C	–	–	–10	µA
		V_I = 5.5 V; T_{amb} = 25 °C	–	–	10	µA
Inputs/outputs LTDATA, SBCL, SBDA and SBWS						
V_{OL}	LOW level output voltage	I_O = – 3mA	–	–	0.4	V
V_{OH}	HIGH level output voltage	I_O = 3 mA	$V_{DD} - 0.5$	–	–	V

Note

1. For applications requiring minimum power dissipation the device may be operated from a nominal +4 V supply.

AC CHARACTERISTICS

V_{DD} = 3.8 to 5.5 V; T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Clock inputs						
C_i	input capacitance		–	–	10	pF
CLK24						
f	pulse frequency		23	24.576	26	MHz
t_{L-i}	pulse width LOW		10	–	–	ns
t_{H-i}	pulse width HIGH		10	–	–	ns
SBMCLK						
f	pulse frequency		–	6.144	12.5	MHz
t_{L-i}	pulse width LOW		30	–	–	ns
t_{H-i}	pulse width HIGH		30	–	–	ns
Clock outputs						
C_L	load capacitance		–	–	50	pF
MCLK						
f	pulse frequency		–	6.144	–	MHz
t_{L-i}	pulse width LOW		50	–	–	ns
t_{H-i}	pulse width HIGH		50	–	–	ns
t_{dMFR}	delay time from CLK24	note 1	–	–	45	ns
t_d	delay time from PWRDWN		–	15	–	ns
Clock inputs						
C_i	input capacitance		–	–	10	pF
Inputs LTCLK, LTCNT0, LTCNT1, LTEN, RESET, TCH0 to TCH7 and TAUX						
t_{suMR}	set-up time to MCLK	note 2	40	–	–	ns
t_{hMR}	hold time from MCLK	note 2	0	–	–	ns
Input PINI						
t_{suMR}	set-up time to MCLK	note 1	70	–	–	ns
t_{hMR}	hold time from MCLK	note 1	0	–	–	ns
Outputs						
C_L	load capacitance		–	–	50	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Outputs A0 to A8, AZCHK, TEST2, LTREF, SBDIR, SBEF, SPDF, SPEED, PINO1 to PINO3, URDA, WCLOCK, WDATA, OEN and WEN						
t_{dMR}	delay time from MCLK	note 2	–	–	30	ns
Outputs OEN and WEN						
t_d	delay time from PWRDWN		–	15	–	ns
Output RASN						
t_{dFR}	delay time from CLK24	note 1	–	–	30	ns
t_d	delay time from PWRDWN		–	15	–	ns
Output CASN						
t_{dFR}	delay time from CLK24	note 1	–	–	30	ns
t_d	delay time from PWRDWN		–	15	–	ns
Inputs/outputs						
C_i	input capacitance		–	–	10	pF
C_L	load capacitance		–	–	50	pF
Inputs/outputs D0 to D3						
t_{suCR}	set-up time to CASN	note 3	10	–	–	ns
t_{hCR}	hold time from CASN	note 3	0	–	–	ns
t_{dMR}	delay time from MCLK	note 2	–	–	25	ns
t_d	delay time from PWRDWN		–	15	–	ns
Input/output LTDATA						
t_{suMR}	set-up time to MCLK	note 2	40	–	–	ns
t_{hMR}	hold time from MCLK	note 2	0	–	–	ns
t_{dMR}	delay time from MCLK	note 2	–	–	30	ns
t_d	delay time from PWRDWN		–	15	–	ns
t_d	delay time from LTEN		–	15	–	ns
Inputs/outputs SBCL and SBWS						
t_{suMR}	set-up time to MCLK	note 2	40	–	–	ns
t_{hMR}	hold time from MCLK	note 2	0	–	–	ns
t_{dSR}	delay time from SBMCLK	note 3	–	–	40	ns
t_{dMR}	delay time from MCLK	notes 2 and 5	–	–	30	ns
t_d	delay time from PWRDWN		–	15	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input/output SBDA						
t_{suMR}	set-up time to MCLK	note 2	40	–	–	ns
t_{hMR}	hold time from MCLK	note 2	0	–	–	ns
t_{dMR}	delay time from MCLK	note 2	–	–	30	ns
t_d	delay time from PWRDWN		–	15	–	ns

Notes

1. LOW-to-HIGH transition of CLK24.
2. LOW-to-HIGH transition of MCLK.
3. LOW-to-HIGH transition of CASN.
4. LOW-to-HIGH transition of SBMCLK.
5. 3-state control.

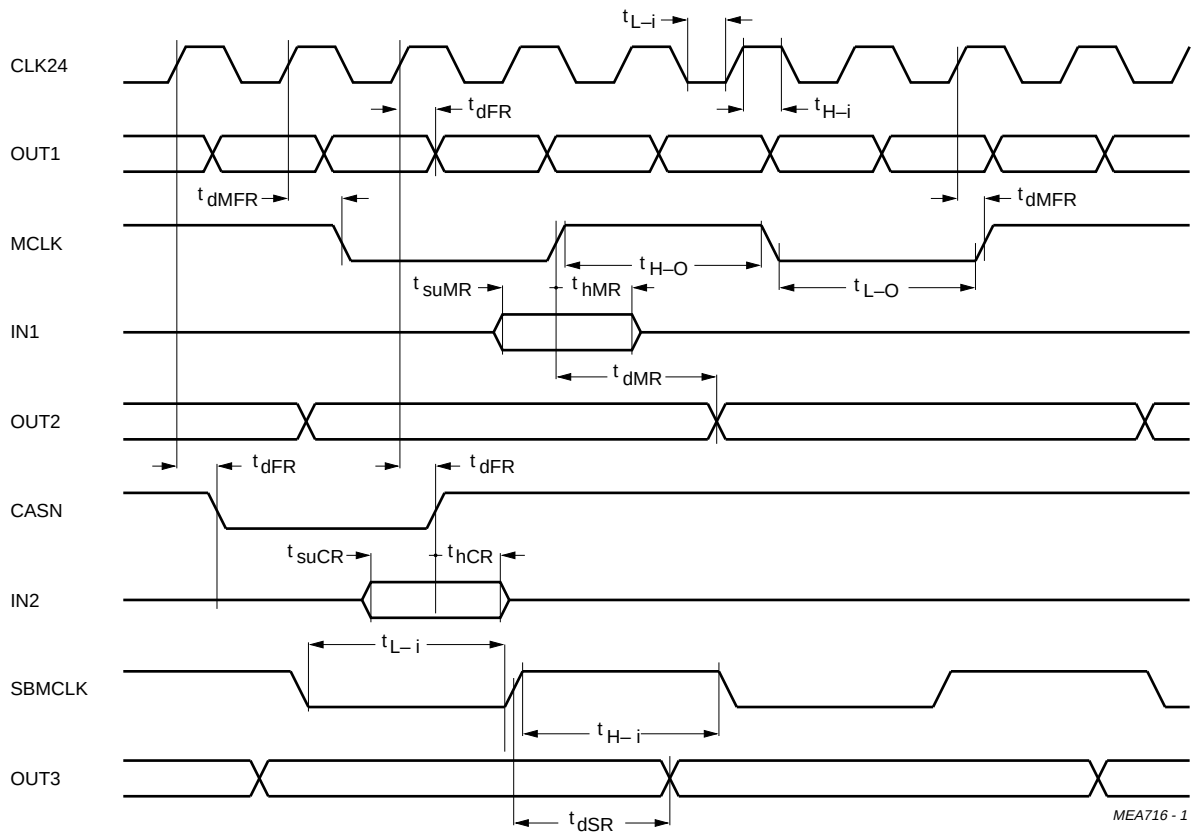
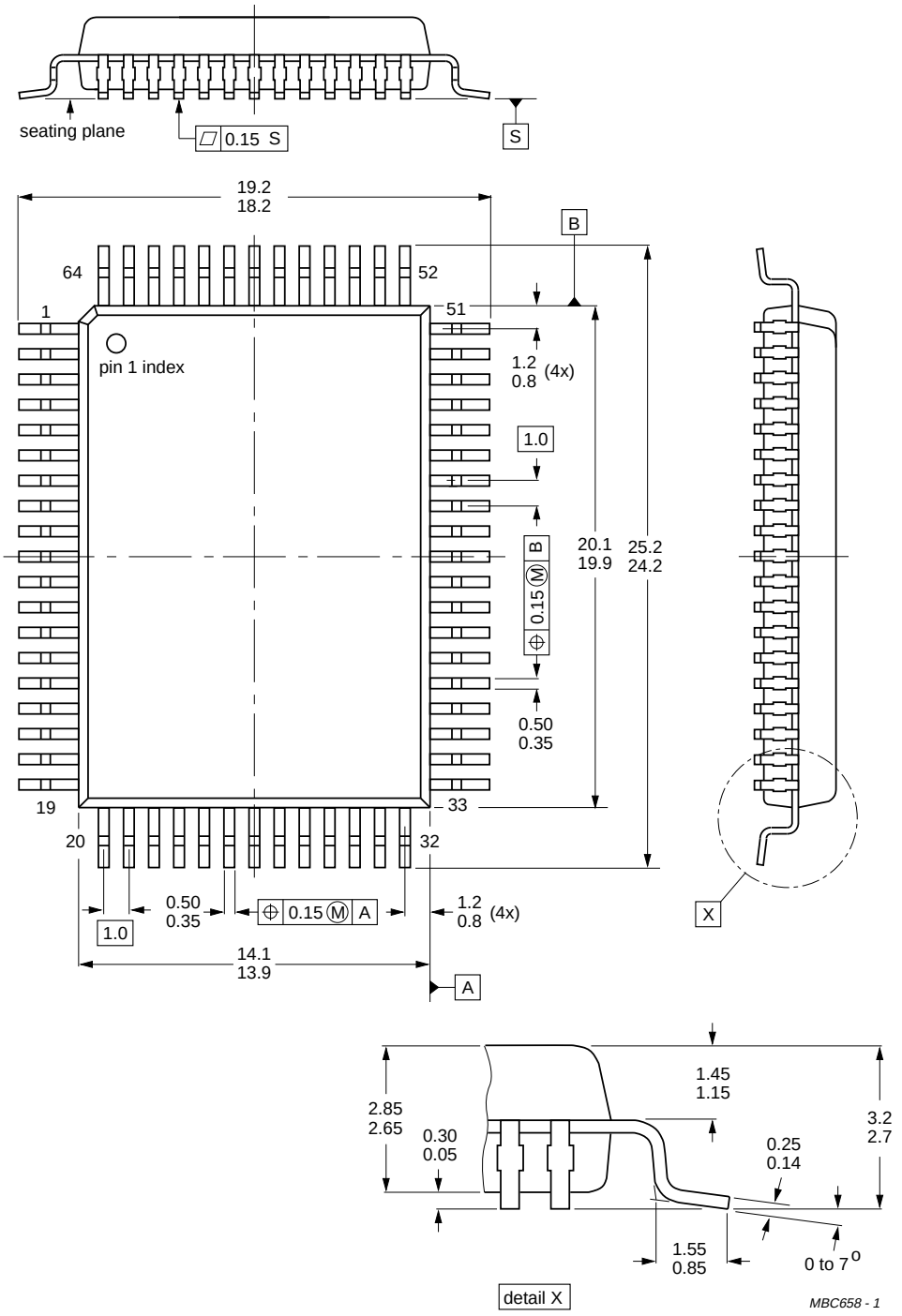


Fig.30 Timing for AC characteristics.

PACKAGE OUTLINE



Dimensions in mm.

Fig.31 64-lead quad flat-pack; plastic (SOT208).

SOLDERING

Quad flat-packs

BY WAVE

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 s, if allowed to cool to less than 150 °C within 6 s. Typical dwell time is 4 s at 250 °C.

A modified wave soldering technique is recommended using two waves (dual-wave), in which, in a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly-activated flux eliminates the need for removal of corrosive residues in most applications.

BY SOLDER PASTE REFLOW

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 s according to method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 min at 45 °C.

REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING IRON OR PULSE-HEATED SOLDER TOOL)

Fix the component by first soldering two, diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages.)

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress rating only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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NOTES

NOTES

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