PROGRAMMABLE ANALOG COMPANDOR — SA/NE572

DESCRIPTION

The NE572 is a dual channel, high performance gain control circuit in which either channel may be used for dynamic range compression or expansion. Each channel has a full wave rectifier to detect the average value of input signal; a linearized, temperature compensated variable gain cell (ΔG) and a dynamic time constant buffer. The buffer permits independent control of dynamic attack and recovery time with minimum external components and improved low frequency gain control ripple distortion over previous compandors.

The NE572 is intended for noise reduction in high performance audio systems. It can also be used in a wide range of communication systems and video recording applications.

FEATURES

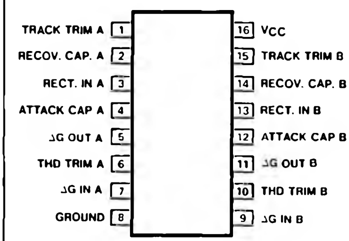
- **Independent control of attack and recovery time.**
- **Improved low frequency gain control ripple**
- **Complementary gain compression and expansion with external Op Amp**
- **Wide dynamic range—greater than 110dB**
- **Temperature compensated gain control**
- **Low distortion gain cell**
- **Low noise—6μV typical**
- **Wide supply voltage range—6V-22V**
- **System level adjustable with external components.**

APPLICATIONS

- **Dynamic noise reduction system**
- **Voltage control amplifier**
- **Stereo expandor**
- **Automatic level control**
- **High level limiter**
- **Low level noise gate**
- **State variable filter**

PIN CONFIGURATION

D, N PACKAGE



(Top view)

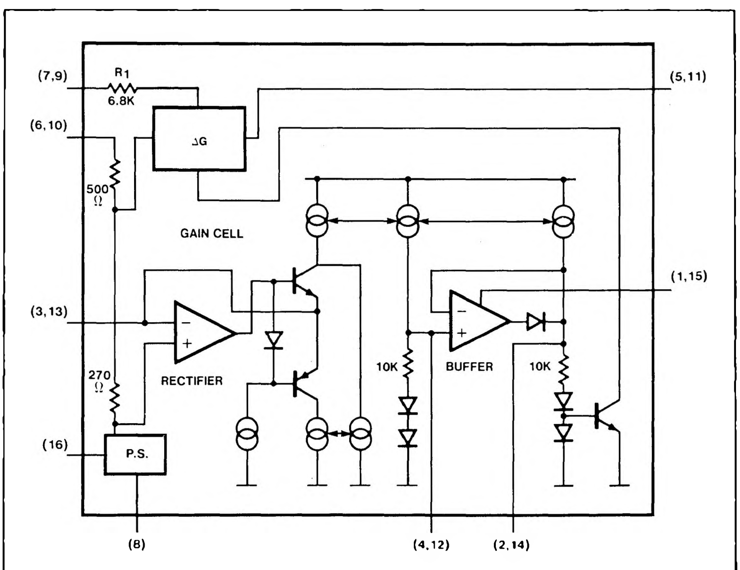
ORDER PART NO.

NE572N SA572N
SA572F NE572D SA572D

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	22	VDC
T_A	Operating temperature range	0 to 70	°C
P_D	Power dissipation	500	mW

BLOCK DIAGRAM



Note:
1. Supplied only in large SO (Small Outline) package.

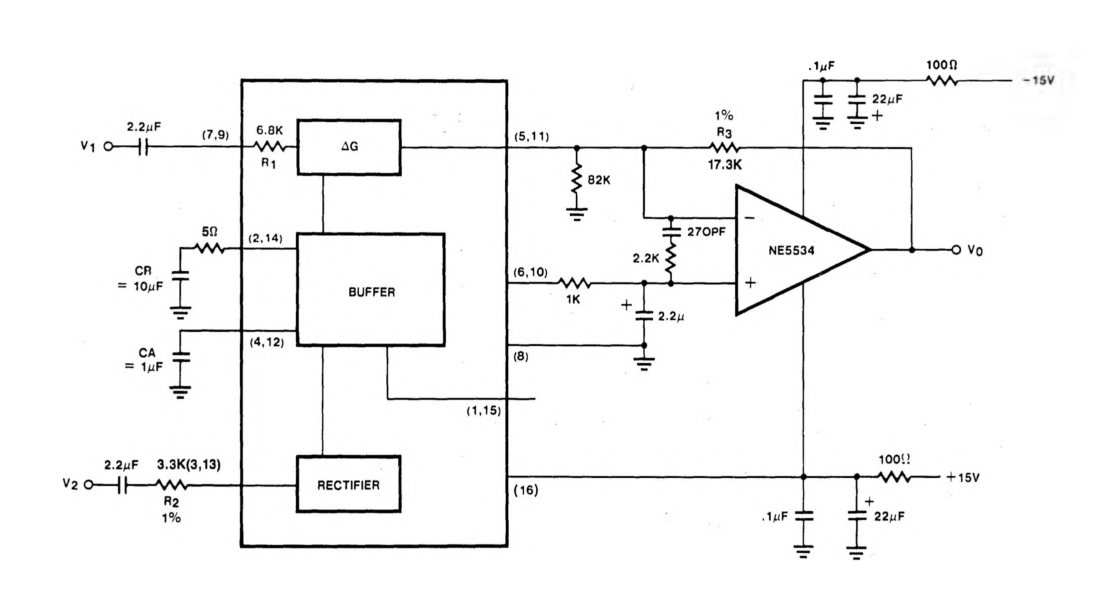
PROGRAMMABLE ANALOG COMPANDOR — SA/NE572

ELECTRICAL CHARACTERISTICS

Standard Test Conditions (unless otherwise noted) V_{CC} = 15V TA = 25°C Expandor mode (see test circuit) Input signals at unity gain level (OdB) = 100mV RMS at 1KHz, $V_1 = V_2$, R_2 = 3.3K, R_3 = 17.3K

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Supply voltage		6		22	V_{DC}
I_{CC}	Supply current	No Signal			6	mA
	Internal voltage reference		2.3	2.5	2.7	V_{DC}
THD	(untrimmed)	1kHz C_A = 1.0μF		.2	1.0	%
THD	(trimmed)	1kHz C_R = 10μF		.05		%
THD	(trimmed)	100Hz		.25		%
	No signal output noise	Input to V_1 and V_2 grounded (20-20kHz)		6	25	uV
	DC level shift (untrimmed)	Input change from no signal to 100mV RMS		±20	±50	MV
	Unity gain level		−1	0	+1	dB
	Large signal distortion	$V_1 = V_2$ = 400mV		0.7	3.0	%
	Tracking error (measured relative to value at unity gain output) = $[V_O - V_O(\text{unity gain})]$ dB − V_2 (dBm)	Rectifier input V_2 = +6dB, V_1 = OdB V_2 = −30dB, V_1 = OdB		±.2 ±.5	−1.5 +.8	dB
	Channel crosstalk	200mV RMS into channel A, measured output on channel B	60			dB
	Power supply rejection ratio	120Hz		70		dB

TEST CIRCUIT



AUDIO SIGNAL PROCESSING IC COMBINES VCA AND FAST ATTACK-SLOW RECOVERY LEVEL SENSOR

In high performance audio gain control applications it is desirable to independently control the attack and recovery time of the gain control signal. This is true, for example, in compandor applications for noise reduction. In high end systems the input signal is usually split into two or more frequency bands to optimize the dynamic behavior for each band. This reduces low frequency distortion due to control signal ripple, phase distortion, high frequency channel overload and noise modulation. Because of the expense in hardware, multiple band signal processing up to now was limited to professional audio applications.

With the introduction of the Signetics NE572 this high performance noise reduction concept becomes feasible for consumer hi fi applications. The NE572 is a dual channel gain control IC. Each channel has a linearized, temperature compensated gain cell and an improved level sensor. In conjunction with an external low noise op amp for current to voltage conversion, the VCA features low distortion, low noise and wide dynamic range. The novel level sensor which provides gain control current for the VCA gives lower gain control ripple and independent control of fast attack, slow recovery dynamic response. An attack capacitor CA with an internal 10K resistor RA defines the attack time TA. The recovery time TR of a tone burst is defined by a recovery capacitor CR and an internal 10K resistor R_R. Typical attack time of 4MS for the high frequency spectrum and 40MS for the low frequency band can be obtained with .1µF and 1.0µF attack capacitors respectively. Recovery time of 200MS can be obtained with a 4.7µF external capacitor. With the recovery capacitor added in the level sensor, the gain control ripple for low frequency signals is much lower than that of a simple RC ripple filter. As a result the residual third harmonic distortion of low frequency signal in a two quad transconductance amplifier is greatly improved. With the 1.0µF attack capacitor and 4.7µF recovery capacitor for a 100HZ signal the third harmonic distortion is improved by more than 10db over the simple RC ripple filter with a single 1.0µF attack and recovery capacitor, while the attack time remains the same.

The NE572 is assembled in a standard 16 pin dual in line plastic package and in oversized SO (Small Outline) package. It operates over wide supply range from 6V to 22V. Supply current is less than 6mA. The NE572 is designed for consumer application over a temperature range 0-70°C. The SA572 is intended for applications from −40°C to +85°C.

NE572 BASIC APPLICATIONS

Description

The NE572 consists of two linearized, temperature compensated gain cells (ΔG) each with a full-wave rectifier and a buffer amplifier as shown in the block diagram. The two channels share a 2.5V common bias reference derived from the power supply but otherwise operate independently. Because of inherent low distortion, low noise and the capability to linearize large signals, a wide dynamic range can be obtained. The buffer amplifiers are provided to permit control of attack time and recovery time independent of each other. Partitioned as shown in the block diagram, the IC allows flexibility in the design of system levels that optimize DC shift, ripple distortion, tracking accuracy and noise floor for a wide range of application requirements.

Gain Cell

Figure 1 shows the circuit configuration of the gain cell. Bases of the differential pairs $Q_1 - Q_2$ and $Q_3 - Q_4$ are both tied to the output and inputs of OPA A_1. The negative feedback through Q_1 holds the V_{BE} of $Q_1 - Q_2$ and the V_{BE} of $Q_3 - Q_4$ equal. The following relationship can be derived from the transistor model equation in the forward active region.

$$\Delta V_{BE_{Q_3-Q_4}} = \Delta_{BE_{Q_1-Q_2}}$$

$$(V_{BE} = V_T \ln I_C/I_S)$$

$$V_T \ln\left(\frac{\frac{1}{2}I_G + \frac{1}{2}I_O}{I_S}\right) - V_T \ln\left(\frac{\frac{1}{2}I_G - \frac{1}{2}I_O}{I_S}\right) = V_T \ln\left(\frac{I_1 + I_{in}}{I_S}\right) - V_T \ln\left(\frac{I_2 - I_1 - I_{in}}{I_S}\right) \quad \text{--(2)}$$

where $I_{in} = \frac{V_{in}}{R_1}$

$R_1 = 6.8K$
$I_1 = 140\mu A$
$I_2 = 280\mu A$

I_O is the differential output current of the gain cell and I_G is the gain control current of the gain cell.

If all transistors Q_1 through Q_4 are of the same size, equation (2) can be simplified to:

$$I_O = \frac{2}{I_2} \cdot I_{in} \cdot I_G - \frac{1}{I_2}(I_2 - 2I_1) \cdot I_G \qquad (3)$$

The first term of eqn. (3) shows the multiplier relationship of a linearized two quadrant transconductance amplifier. The second term is the gain control feed through due to the mismatch of devices. In the design this

BASIC GAIN CELL SCHEMATIC

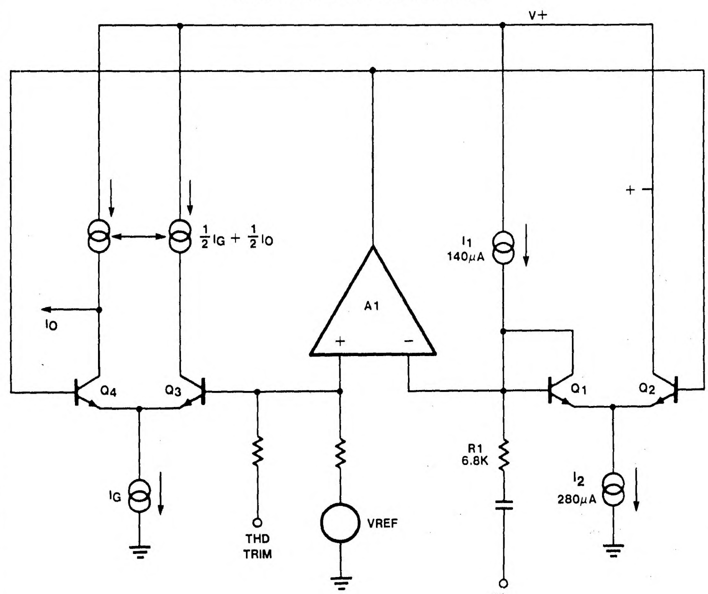


Figure 1

has been minimized by large matched devices and careful layout. Offset voltage is caused by the device mismatch and it leads to even harmonic distortion. The offset voltage can be trimmed out by feeding a current source within $\pm 25\mu A$ into the THD trim pin. The residual distortion is third harmonic distortion and is caused by gain control ripple. In a compandor system, available control of fast attack and slow recovery improves ripple distortion significantly. At the unity gain level of 100mV, the gain cell gives THD (total harmonic distortion) of .17% TYP. Output noise with no input signals is only $6\mu V$ in the audio spectrum (10HZ-20KHZ). The output current I_O must feed the virtual ground input of an operational amplifier with a resistor from output to inverting input. The non-inverting input of the operational amplifier has to be biased at VREF if the output current I_O is dc coupled.

Rectifier

The rectifier is a full-wave design as shown in Figure 2. The input voltage is converted to current through the input resistor R2 and turns on either Q5 or Q6 depending on the signal polarity. Deadband of the voltage to current converter is reduced by the loop gain of the gain block A2. If AC coupling is used, the rectifier error comes only from input bias current of gain block A2. The input bias current is typically about 70nA. Frequency response of the gain block A2 also causes second order error at high frequency. The collector current of Q6 is mirrored and summed at the collector of Q5 to form the full wave rectified output current I_R. The rectifier transfer function is

$$\frac{V_{IN} - V_{REF}}{R_2} \quad (4)$$

If Vin is A.C. coupled, then the equation will be reduced to:

$$I_{RAC} = \frac{V_{in}(AVG)}{R_2}$$

The internal bias scheme limits the maximum output current I_R to be around $300\mu A$. Within a $\pm$ 1dB error band the input range of the rectifier is about 52dB.

Buffer Amplifier

In audio systems, it is desirable to have fast attack time and slow recovery time for a tone burst input. The fast attack time reduces transient channel overload but also causes low frequency ripple distortion. The low frequency ripple distortion can be improved with the slow recovery time. If different attack times are implemented in corresponding frequency spectrums in a split band audio system, high quality performance can be achieved. The buffer amplifier is designed to make this feature available with minimum external components. Refer-

SIMPLIFIED RECTIFIER SCHEMATIC

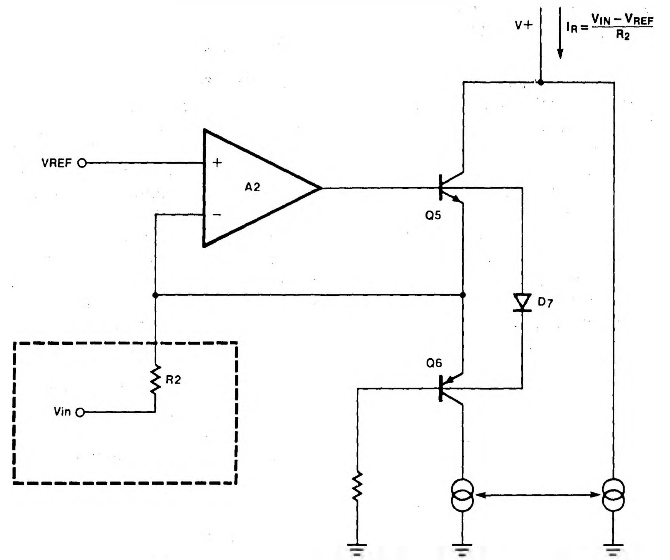


Figure 2

BUFFER AMPLIFIER SCHEMATIC

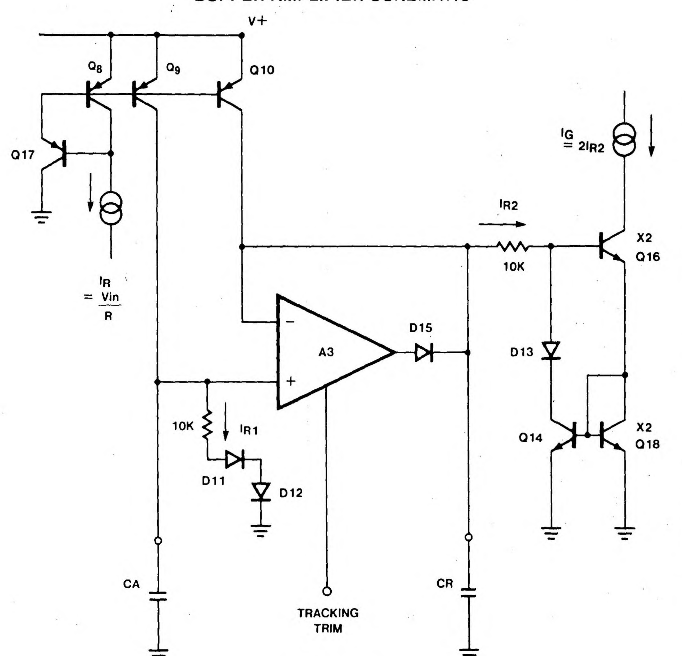


Figure 3

ring to Figure 3, the rectifier output current is mirrored into the input and output of the unipolar buffer amplifier A_3 through Q_8, Q_9 and Q_{10}. Diodes D_{11} and D_{12} improve tracking accuracy and provide common mode bias for A_3. For a positive going input signal, the buffer amplifier acts like a voltage follower. Therefore, the output impedance of A_3 makes the contribution of capacitor CR to attack time insignificant. Neglecting diode impedance the gain Ga(t) for ΔG can be expressed as follows.

$$Ga(t) = (Ga_{INT} - Ga_{FNL})\, e^{\frac{-t}{\tau A}} + Ga_{FNL}$$

Ga_{INT} = Initial Gain

$\tau A = R_A \cdot CA = 10K \cdot CA$ Ga_{FNL} = Final Gain

where τA is the attack time constant and RA is a 10K internal resistor. Diode D_{15} opens the feedback loop of A_3 for a negative going signal if the value of capacitor CR is larger than capacitor CA. The recovery time depends only on CR • R_R. If the diode impedance is assumed negligible, the dynamic gain G_R (t) for ΔG is expressed as follows.

$$G_R(t) = (G_{R\,INT} - G_{R\,FNL})\, e^{\frac{-t}{\tau R}} + G_{R\,FNL}$$

$\tau R = R_R \cdot CR = 10K \cdot CR$

where τR is the recovery time constant and R_R is a 10K internal resistor. The gain control current is mirrored to the gain cell through Q_{14}. The low level gain errors due to input bias current of A_2 and A_3 can be trimmed through the tracking trim PIN into A_3 with a current source of $\pm 3\mu A$.

Basic Expandor

Figure 4 shows an application of the circuit as a simple expandor. The gain expression of the system is given by

$$\frac{V_{OUT}}{V_{IN}} = \frac{2}{I_1} \bullet \frac{R_3 \bullet V_{IN}(AVG)}{R_2 \bullet R_1} \quad (I_1 = 140\mu A) \qquad (5)$$

Both the resistors R_1 and R_2 are tied to internal summing nodes. R_1 is a 6.8K internal resistor. The maximum input current into the gain cell can be as large as 140μA. This corresponds to a voltage level of 140μA • 6.8K = 952mV peak. The input peak current into the rectifier is limited to 300μA by the internal bias system. Note that the value of R_1 can be increased to accommodate higher input level. R_2 and R_3 are external resistors. It is easy to adjust the ratio of R3/R2 for desirable system voltage and current levels. A small R2 results in higher gain control current and smaller static and dynamic tracking error. However, an impedance buffer A_1 may be necessary if the input is voltage drive with large source impedance.

The gain cell output current feeds the summing node of the external OPA A_2. R_3 and A_2 convert the gain cell output current to the output voltage. In high performance applications, A_2 has to be low noise, high speed and wide band so that the high performance output of the gain cell will not be degraded. The non-inverting input of A_2 can be biased at the low noise internal reference PIN 6 or 10. Resistor R_4 is used to biased up the output DC level of A_2 for maximum swing. The output DC level of A_2 is given by

$$V_{ODC} = V_{REF}\left(1 + \frac{R_3}{R_4}\right) - V_B \frac{R_3}{R_4} \qquad (6)$$

V_B can be tied to a regulated power supply for a dual supply system and be grounded for a single supply system. CA sets the attack time constant and CR sets the recovery time constant.

BASIC EXPANDOR SCHEMATIC

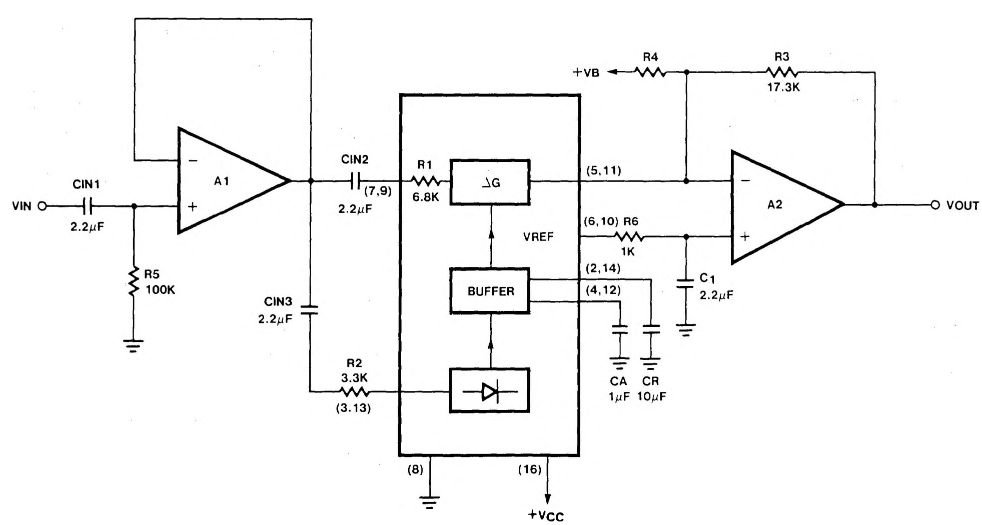


Figure 4

Basic Compressor

Figure 5 shows the hook-up of the circuit as a compressor. The IC is put in the feedback loop of the OPA A_1. The system gain expression is as follows:

$$\frac{V_{OUT}}{V_{IN}} = \left(\frac{I_1}{2} \cdot \frac{R_2 \cdot R_1}{R_3 \cdot V_{IN}(AVG)}\right)^{1/2} \quad (7)$$

RDC1, RDC2, and CDC form a dc feedback for A_1. The output DC level of A_1 is given by

$$V_{ODC} = V_{REF}\left(1 + \frac{R_{DC1} + R_{DC2}}{R_4}\right) - V_B \cdot \left(\frac{R_{DC1} + R_{DC2}}{R_4}\right) \quad (8)$$

The zener diodes D_1 and D_2 are used for channel overload protection.

Basic Compandor System

The above basic compressor and expandor can be applied to systems such as tape/disc noise reduction, digital audio, bucket brigade delay lines. Additional system design techniques such as bandlimiting, band splitting, pre-emphasis, de-emphasis and equalization are easy to incorporate. The IC is a versatile functional block to achieve a high performance audio system. Figure 6 shows the system level diagram for reference.

For additional information, refer to tho Applications Section.

BASIC COMPRESSOR SCHEMATIC

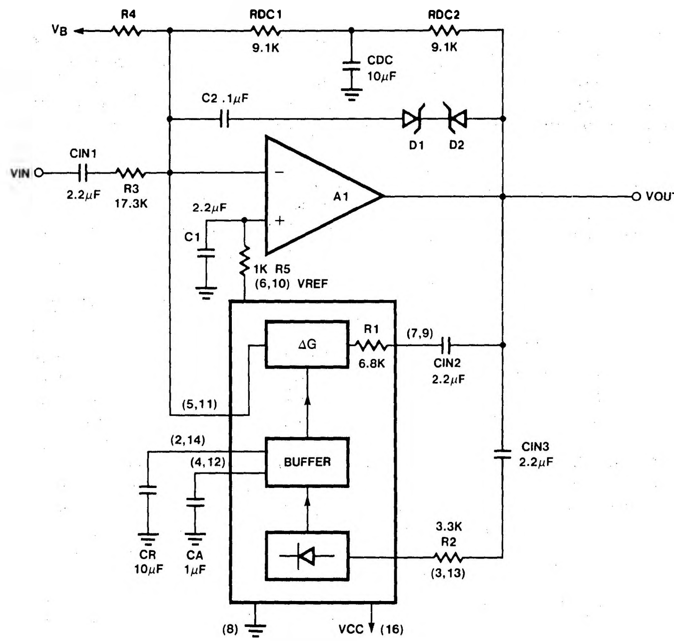


Figure 5

NE572 SYSTEM LEVEL

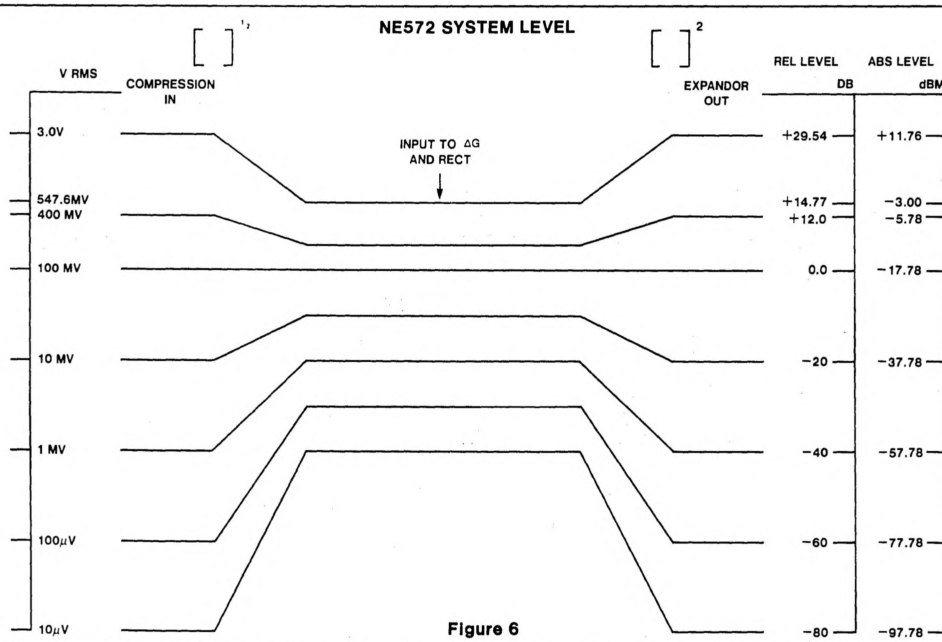


Figure 6

*For additional information, consult the Applications Section.