signetics

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

S54S194
N74S194

DIGITAL 54/74 TTL SERIES

DESCRIPTION

These high-performance bidirectional shift registers are functionally and mechanically identical to the N54194 and S74194, however, with a typical shift frequency of 110 megahertz the Schottky-clamped versions can be used in very high-speed systems, or can be substituted for the N54194/S74194 to upgrade the performance of most existing systems. The universal shift register has four distinct modes of operation, namely:

	MODE CONTROL	
	S1	S0
Parallel (Broadside) Load	H	H
Shift Right (In the direction Q_A toward Q_D)	L	H
Shift Left (In the direction Q_D toward Q_A)	H	L
Hold (recirculate) data	L	L

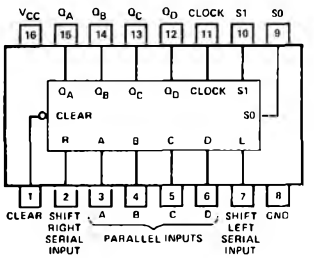
In the parallel-load mode, data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited. Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial input. Data is recirculated when both mode control inputs are low. For added flexibility the mode controls can be changed independently of the clock.

These four-bit shift registers are compatible with most other TTL and DTL logic families. All inputs are buffered to lower the drive requirements to one normalized Series 54S/74S load, and input clamping diodes minimize switching transients to simplify system design. With the equivalent of 46 gates on the monolithic chip, typical power dissipation is less than 10 milliwatts per equivalent gate.

The N54S194 is characterized for operation over the full military temperature range of −55°C to 125°C; the S74S194 is characterized for operation from 0°C to 70°C.

PIN CONFIGURATION

J OR N DUAL IN-LINE OR W FLAT PACKAGE
(TOP VIEW)



Positive Logic: See description

FEATURES

- SCHOTTKY-CLAMPED TO ACHIEVE TYPICAL MAXIMUM SHIFT FREQUENCY OF 110 MHz
- FUNCTIONALLY AND MECHANICALLY IDENTICAL TO N54194, S74194 AND CAN BE USED TO UPGRADE EXISTING SYSTEMS WITH SIGNIFICANT IMPROVEMENT IN SPEED
- FULLY COMPATIBLE WITH MOST OTHER TTL AND DTL CIRCUITS
- N54S194 OPERATES OVER FULL MILITARY TEMPERATURE RANGE OF −55°C TO 125°C
- FOR USE IN HIGH-PERFORMANCE:
  ACCUMULATORS/PROCESSORS,
  SERIAL-TO-PARALLEL AND
  PARALLEL-TO-SERIAL CONVERTERS

RECOMMENDED OPERATING CONDITIONS

		N54S194,			S74S194			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Input clock frequency, f_{clock}		0		75	0		75	MHz
Width of clock or clear pulse, t_w		12			12			ns
Setup time, t_{setup} **(NOTE 2)**	Mode control	12			12			ns
	Serial and parallel data	10			10			
	Clear inactive-state	15			15			
Hold time at any input, t_{hold}		2			2			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA					−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −1 mA	N54S194		2.5	3.4		V
			S74S194		2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA					0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V					1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V					50	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V					−2	mA
I_{OS}	Short-circuit output current‡	V_{CC} = MAX			−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 1	N54S194			90		mA
			S74S194			90		

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Not more than one output should be shorted at a time and duration of the short-circuit test should not exceed one second.

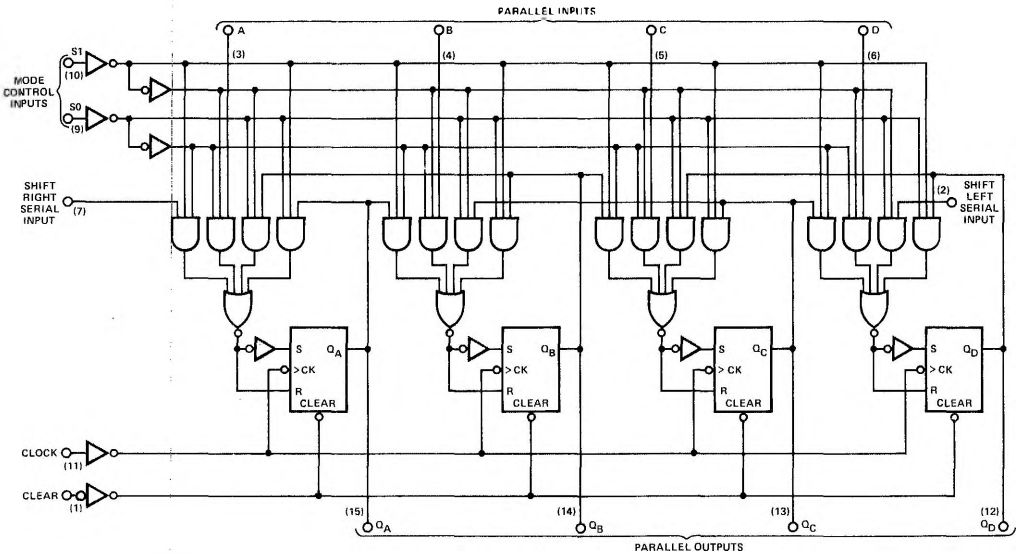
NOTE 1: With all outputs open, inputs A through D grounded, and 4.5 V applied to S0, S1, clear, and the serial inputs, I_{CC} is tested with a momentary ground, then 4.5 V, applied to clock.

SWITCHING CHARACTERISTICS, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum input clock frequency	C_L = 15 pF, R_L = 280 Ω, See Note 2	75	110		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear			11		ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock		4	9		ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock		4	10		ns

NOTE 2: Waveforms and load circuits on page 2-293 with the following additions: $t_{w\ (clock)} \geq 12$ns, $t_{w\ (clear)} \geq 12$ns.

FUNCTIONAL BLOCK DIAGRAM



. . . Dynamic input activated by a transition from a high level to a low level.

TYPICAL CLEAR, LOAD, RIGH-SHIFT, INHIBIT, AND CLEAR SEQUENCES