signetics

DUAL J-K EDGE-TRIGGERED FLIP-FLOP

S54H108 N74H108

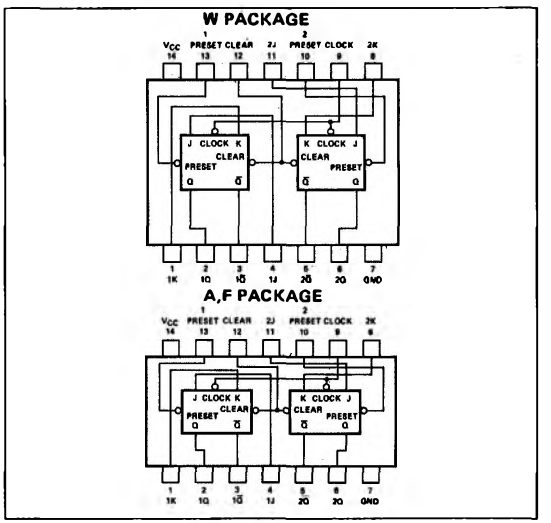
S54H108–A,F,W • N74H108–A,F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

These dual monolithic J-K flip-flops are negative-edge-triggered. They feature individual J, K, and asynchronous preset inputs to each flip-flop as well as common clock and asynchronous clear inputs. When the clock goes high, the inputs are enabled and data is accepted. Logical state of J and K inputs may be allowed to change when the clock pulse is in a high state and bistable performs according to the truth table as long as minimum set-up times are observed. Data input is transferred to the outputs on the negative edge of the clock pulse.

PIN CONFIGURATIONS



TRUTH TABLE

LOGIC

t_n J	t_n K	t_{n+1} Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES:
1. t_n = bit time before clock pulse
2. t_{n+1} = bit time after clock pulse

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S54H108 Circuits		4.5	5	5.5	V
N74H108 Circuits		4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A:	S54H108 Circuits	-55	25	125	°C
	N74H108 Circuits	0	25	70	°C
Normalized Fan-Out from each Output, N				10	
Width of Clock Pulse, $t_{p(clock)}$		10			ns
Width of Preset Pulse, $t_{p(preset)}$		15			ns
Width of Clear Pulse, $t_{p(clear)}$		16			ns
Input Setup Time, t_{setup}: Logical 1		10			ns
Logical 0		13			ns
Input Hold Time, t_{hold}		0			ns
Clock Pulse Transition Time, t_0				150	ns

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS •		MIN	TYP†	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN,	I_{load} = -500μA	2.4	3.2		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN,	I_{sink} = 20mA		0.25	0.4	V
$I_{in(0)}$	Logical 0 level input current at J,K, or preset	V_{CC} = MAX,	V_{in} = 0.4V		-1	-2	mA
$I_{in(0)}$	Logical 0 level input current at clock	V_{CC} = MAX,	V_{in} = 0.4V		-6	-9.6	mA
$I_{in(0)}$	Logical 0 level input current at clear	V_{CC} = MAX,	V_{in} = 0.4V		-2	-4	mA
$I_{in(1)}$	Logical 1 level input current at J or K	V_{CC} = MAX,	V_{in} = 2.4V			50	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
$I_{in(1)}$	Logical 1 level input current at clock	V_{CC} = MAX,	V_{in} = 2.4V	0		-1	mA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA

ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{in(1)}$	Logical 1 level input current at preset	V_{CC} = MAX,	V_{in} = 2.4V			100	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
$I_{in(1)}$	Logical 1 level input current at clear	V_{CC} = MAX,	V_{in} = 2.4V			200	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
I_{OS}	Short-circuit output current**	V_{CC} = MAX,	V_{in} = 0	-40		-100	mA
I_{CC}	Supply current	V_{CC} = MAX			40	76	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{clock}	Maximum input clock frequency	C_L = 25pF,	R_L = 280Ω	40	50		MHz
t_{pd1}	Propagation delay time to logical 1 level from preset or clear to output	C_L = 25pF,	R_L = 280Ω		8	12	ns
t_{pd0}	Propagation delay time to logical 0 level from preset or clear to output (clock low)	C_L = 25pF,	R_L = 280Ω		23	35	ns
t_{pd0}	Propagation delay time to logical 0 level from preset or clear to output (clock high)	C_L = 25pF,	R_L = 280Ω		15	20	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	C_L = 25pF,	R_L = 280Ω	5	10	15	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	C_L = 25pF,	R_L = 280Ω	8	16	20	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

† All typical values are at V_{CC} = 5V, T_A = 25°C.

DIGITAL 54/74 TTL SERIES

DESCRIPTION

Series 54S/74S Schottky TTL circuits are implemented with full Schottky-barrier-diode clamping to achieve ultra-high speeds previously obtainable only with emitter-coupled logic, yet they retain the desirable features of, and are completely compatible with, most of the popular saturated logic circuits. Schottky TTL circuits currently offer the best speed-power product of any high-speed logic family.

Schottky-barrier-diode clamping prevents transistors from achieving classic saturation and thereby effectively eliminates excess charge storage and subsequent recovery times. These recovery times contribute significantly to overall propagation delays experienced with saturated digital-logic circuits.

Series 54S/74S circuits are completely compatible with the Series 54/74, Series 54H/74H, and Series 54L/74L TTL logic families. Ease of use and compatibility with other TTL families result in flexibility of choice within the four speed-power ranges offered (Series 54/74, 54H/74H, 54L/74L, 54S/74S) to achieve highly efficient system grading to specific performance requirements.

Definitive specifications are provided for operating characteristics over the full military temperature range of −55°C to 125°C for Series 54S circuits and over the temperature range of 0°C to 70°C for Series 74S circuits.

FEATURES

VERY-HIGH-SPEED, LOW-POWER OPERATION

- 3-ns typical gate propagation delay time
- 19-mW-per-gate power dissipation at 50% duty cycle—speed-power product = 57pJ
- 125-MHz typical J-K flip-flop maximum input clock frequency (d-c coupled)

EASE OF SYSTEM DESIGN

- fully compatible with Series 54/74, 54H/74H, and 54L/74L TTL (including MSI/LSI), and most DTL
- Schottky-diode-clamped inputs simplify system design
- terminated, controlled-impedance lines not normally required
- low output impedance: provides low AC noise susceptability drives highly capacitive loads

IMPROVED CIRCUIT PERFORMANCE

- switching times virtually insensitive to power supply and/or temperature variations
- power dissipation remains relatively low at operating frequencies up to 100 MHz
- high-fan-out: 20 54S/74S loads at the high logic level 10 54S/74S loads at the low logic level
- high DC noise margin—typically 1 volt

ABSOLUTE MAXIMUM RATINGS (over operating free-air temperature range unless otherwise noted)

Supply Voltage V_{CC}	7V
Input Voltage	5.5V
Intermitter Voltage	5.5V
Output Voltage	7V
Operating Free-Air Temperature Range:	
Series 54S Circuits	−55°C to 125°C
Series 74S Circuits	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

NOTES:

1. Voltage values, except intermitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor.
3. This is the maximum voltage which should be applied to any open-collector output when it is in the off state.

UNUSED INPUTS OF POSITIVE-AND/NAND GATES

For optimum switching times and minimum noise susceptibility, unused inputs of AND or NAND gates should be maintained at a voltage greater than 2.7V, but not to exceed the absolute maximum rating of 5.5V. This eliminates the distributed capacitance associated with the floating input emitter, bond wire, and package lead, and ensures that no degradation will occur in the propagation delay times. Some possible ways of handling input emitters are:

a. Connect unused inputs to an independent supply voltage. Preferably, this voltage should be between 2.7V and 3.5V.
b. Connect unused inputs to a used input if maximum fan-out of the driving output will not be exceeded. Each additional input presents a full load to the driving output at a high-level voltage but adds no loading at a low-level voltage.
c. Connect unused inputs to V_{CC} through a 1-kΩ resistor so that if a transient which exceeds the 5.5-V maximum rating should occur, the impedance will be high enough to protect the input. One to 25 unused inputs may be connected to each 1-kΩ resistor.

INPUT-CURRENT REQUIREMENTS

Input-current requirements reflect worst-case V_{CC} and temperature conditions. Each input of the multiple-emitter input transistors requires a maximum of 2mA out of the input at a low logic level which is defined as 1 normalized load. Each input requires current into the input at a high logic level. This current is 50μA maximum for each emitter. Currents into the input terminals are specified as positive values.

FAN-OUT CAPABILITY

Fan-out (N) reflects the ability of an output to supply current to a number of normalized loads at a high logic level and to sink current at the low logic level. At the high logic level, each standard output is capable of supplying current to drive 20 Series 54H, 74H, 54S, or 74S loads (N_H = 20). Currents out of the output are specified as negative values. At the low logic level, each standard output is capable of sinking current from 10 Series 54H, 74H, 54S, or 74S loads (N_L = 10).

RECOMMENDED OPERATING CONDITIONS

	SERIES 54S CIRCUITS			SERIES 74S CIRCUITS			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Operating Free-Air Temperature, T_A	−55		125	0		70	°C