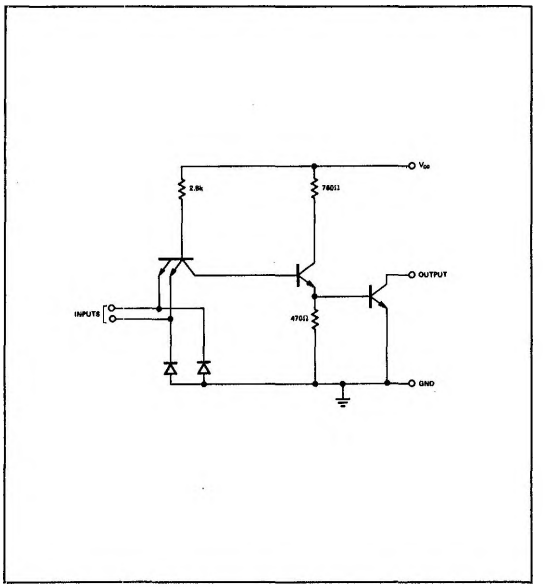
signetics QUADRUPLE 2-INPUT POSITIVE NAND GATE WITH OPEN COLLECTOR OUTPUT

S54H01 N74H01

S54H01–A,F,W • N74H01–A,F

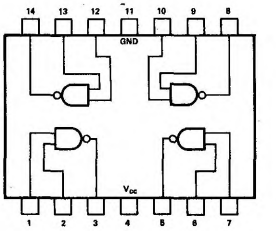
DIGITAL 54/74 TTL SERIES

SCHEMATIC (each gate)

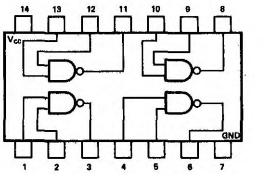


PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S54H01 Circuits		4.5	5	5.5	V
N74H01 Circuits		4.75	5	5.25	V
Normalized Fan-Out from each Output, N				10	
Operating Free-Air Temperature Range, T_A:	S54H01 Circuits	-55	25	125	°C
	N74H01 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical $0_{(on)}$ level at output	V_{CC} = MIN,		2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical $1_{(off)}$ level at output	V_{CC} = MIN,				0.8	V
$I_{out(1)}$	Output reverse current	V_{CC} = MIN, $V_{out(1)}$ = 5.5V	V_{in} = 0.8V,			250	μA
$V_{out(0)}$	Logical 0 output voltage (on level)	V_{CC} = MIN, I_{sink} = 20mA	V_{in} = 2V,			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.4V			-2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX,	V_{in} = 2.4V			50	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 4.5V		26	40	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX	V_{in} = 0		6.8	10.0	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS†		MIN	TYP**	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 25pF,	R_L = 280Ω		7.5	12.0	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 25pF,	R_L = 280Ω		10.0	15.0	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Load resistor R_L is connected from V_{CC} to the output, and load capacitor C_L is connected from the output to ground.