# GATED FULL ADDER

# S5480
# N7480

S5480–A,F,W • N7480–A,F

DIGITAL 54/74 TTL SERIES

## DESCRIPTION

The S5480/N7480 is a single-bit, high-speed, binary full adder with gated complementary inputs, complementary sum ($\Sigma$ and $\overline{\Sigma}$) outputs and inverted carry output. Designed for medium- and high-speed, multiple-bit, parallel-add/serial-carry applications, the circuit (see schematic diagram) utilizes diode-transistor logic (DTL) for the gated inputs, and high-speed, high-fan-out transistor-transistor logic (TTL) for the sum and carry outputs. The circuit is entirely compatible with both DTL and TTL logic families. The implementation of a single-inversion, high-speed, Darlington-connected serial-carry circuit minimizes the necessity for extensive "look-ahead" and carry-cascading circuits. The power dissipation has been maintained considerably below that attainable with equivalent standard integrated circuits connected to perform full-adder functions.

## TRUTH TABLE (See Notes 1,2, and 3)

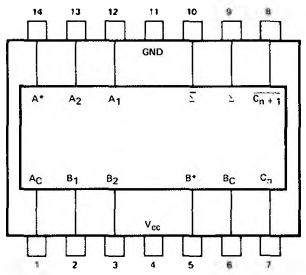
**LOGIC**

| $C_n$ | B | A | $C_{n+1}$ | $\overline{\Sigma}$ | $\Sigma$ |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 1 | 0 |
| 0 | 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 | 1 |

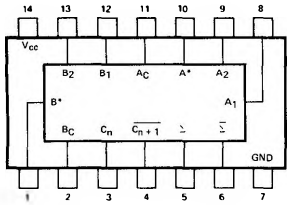
NOTES:
1. $A = \overline{A^* \cdot A_c}$, $B = \overline{B^* \cdot B_c}$ where $A^* = \overline{A_1 \cdot A_2}$, $B^* = \overline{B_1 \cdot B_2}$.
2. When $A^*$ or $B^*$ are used as inputs, $A_1$ and $A_2$ or $B_1$ and $B_2$ respectively, must be connected to GND.
3. When $A_1$ and $A_2$ or $B_1$ and $B_2$ are used as inputs, $A^*$ or $B^*$ respectively, must be open or used to perform Dot-OR logic.
4. The voltages are with respect to ground terminal.
5. Input signals must be zero or positive with respect to network ground terminal.

## PIN CONFIGURATIONS

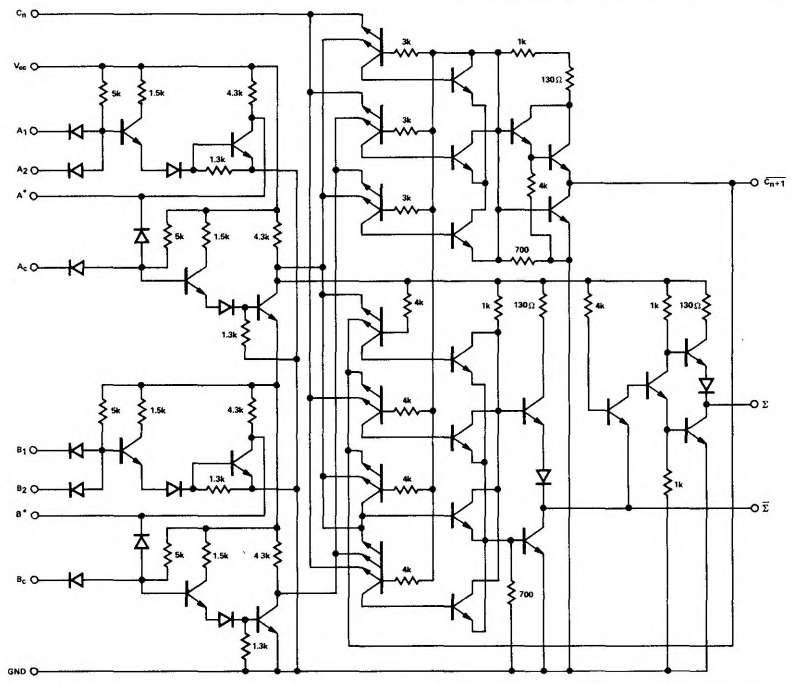
**W PACKAGE**




**A,F PACKAGE**




## SCHEMATIC DIAGRAM



## RECOMMENDED OPERATING CONDITIONS

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply Voltage $V_{CC}$: | S5480 Circuits | 4.5 | 5 | 5.25 | V |
| | N7480 Circuits | 4.75 | 5 | 5.25 | V |
| **Normalized Fan-Out from Outputs:** | $\overline{C_n+1}$, N | | | 5 | |
| | $\Sigma$ or $\overline{\Sigma}$, N | | | 10 | |
| | A* or B*, N | | | 3 | |
| Operating Free-Air Temperature Range, $T_A$: | S5480 Circuits | -55 | 25 | 125 | °C |
| | N7480 Circuits | 0 | 25 | 70 | °C |

## ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

| PARAMETER | | TEST CONDITIONS* | | | MIN | TYP** | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{in(1)}$ | Logical 1 input voltage | $V_{CC}$ = MIN | | | 2 | | | V |
| $V_{in(0)}$ | Logical 0 input voltage | $V_{CC}$ = MIN | | | | | 0.8 | V |
| $V_{out(1)}$ | Logical 1 output voltage | $V_{CC}$ = MIN | | | 2.4 | 3.5 | | V |
| $V_{out(0)}$ | Logical 0 output voltage | $V_{CC}$ = MIN | | | | 0.22 | 0.4 | V |
| $I_{in(0)}$ | Logical 0 level input current at $A_1$, $A_2$, $B_1$, $B_2$, $A_c$ or $B_c$ | $V_{CC}$ = MAX, | $V_{in}$ = 0.4V | | | | -1.6 | mA |
| $I_{in(0)}$ | Logical 0 level input current at A* or B* | $V_{CC}$ = MAX, | $V_{in}$ = 0.4V | | | | -2.6 | mA |
| $I_{in(0)}$ | Logical 0 level input current at $C_n$ | $V_{CC}$ = MAX, | $V_{in}$ = 0.4V | | | | -8 | mA |
| $I_{in(1)}$ | Logical 1 level input current at $A_1$, $A_2$, $B_1$, $B_2$, $A_c$ or $B_c$ | $V_{CC}$ = MAX,<br>$V_{CC}$ = MAX | $V_{in}$ = 2.4V<br>$V_{in}$ = 5.5V | | | | 15<br>1 | µA<br>mA |
| $I_{in(1)}$ | Logical 1 level input current at $C_n$ | $V_{CC}$ = MAX,<br>$V_{CC}$ = MAX, | $V_{in}$ = 2.4V<br>$V_{in}$ = 5.5V | | | | 200<br>1 | µA<br>mA |
| $I_{OS}$ | Short circuit output current at $\Sigma$ or $\overline{\Sigma}$† | $V_{CC}$ = MAX, | | S5480<br>N7480 | -20<br>-18 | | -57<br>-57 | mA<br>mA |
| $I_{OS}$ | Short circuit output current at $\overline{C_{n+1}}$† | $V_{CC}$ = MAX, | | S5480<br>N7480 | -20<br>-18 | | -70<br>-70 | mA<br>mA |
| $I_{CC}$ | Supply current | $V_{CC}$ = MAX, | | S5480<br>N7480 | | 21<br>21 | 31<br>35 | mA<br>mA |

## SWITCHING CHARACTERISTICS, $V_{CC}$ = 5V, $T_A$ = 25°C

| PARAMETER¶ | FROM INPUT | TO OUTPUT | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $t_{pd1}$ | $C_n$ | $\overline{C_{n+1}}$ | $C_L$ = 15pF, | $R_L$ = 780Ω | | 13 | 17 | ns |
| $t_{pd0}$ | | | $C_L$ = 15pF, | $R_L$ = 780Ω | | 8 | 12 | ns |
| $t_{pd1}$ | $B_C$ | $\overline{C_{n+1}}$ | $C_L$ = 15pF, | $R_L$ = 780Ω | | 18 | 25 | ns |
| $t_{pd0}$ | | | $C_L$ = 15pF, | $R_L$ = 780Ω | | 38 | 55 | ns |
| $t_{pd1}$ | $A_C$ | $\Sigma$ | $C_L$ = 15pF, | $R_L$ = 400Ω | | 52 | 70 | ns |
| $t_{pd0}$ | | | $C_L$ = 15pF, | $R_L$ = 400Ω | | 62 | 80 | ns |
| $t_{pd1}$ | $B_C$ | $\overline{\Sigma}$ | $C_L$ = 15pF, | $R_L$ = 400Ω | | 38 | 55 | ns |
| $t_{pd0}$ | | | $C_L$ = 15pF, | $R_L$ = 400Ω | | 56 | 75 | ns |
| $t_{pd1}$ | $A_1$ | A* | $C_L$ = 15pF | | | 48 | 65 | ns |
| $t_{pd0}$ | | | $C_L$ = 15pF | | | 17 | 25 | ns |
| $t_{pd1}$ | $B_1$ | B* | $C_L$ = 15pF | | | 48 | 65 | ns |
| $t_{pd0}$ | | | $C_L$ = 15pF | | | 17 | 25 | ns |

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at $V_{CC}$ = 5V, $T_A$ = 25°C

† Not more than one output should be shorted at a time.

¶ $t_{pd1}$ is propagation delay time to logical 1 level. $t_{pd0}$ is propagation delay time to logical 0 level.