4-BIT PARALLEL-ACCESS SHIFT REGISTER

S54195 N74195

S54195–B,F,W • N74195–B, F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

These 4-bit registers feature parallel inputs, parallel outputs, J-K serial inputs, shift/load control input, and a direct overriding clear.

The registers have two modes of operation:

Parallel (Broadside) Load

Shift (In direction Q_A toward Q_D)

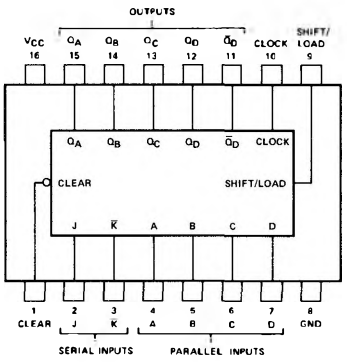
Parallel loading is accomplished by applying the 4 bits of data and taking the shift/load control input low. The data are loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode are entered at the J-K inputs. These inputs permit the first stage to perform as a J-K, D-, or T-type flip-flop as shown in the truth table.

These shift registers are fully compatible with most other TTL and DTL families. All inputs are buffered to lower the drive requirements to one normalized Series 54/74 load, including the clock input. Maximum input clock frequency is typically 39 megahertz and power dissipation is typically 195 milliwatts. The S54195 is characterized for operation over the full military temperature range of -55°C to 125°C; the N74195 is characterized for operation from 0°C to 70°C.

PIN CONFIGURATIONS

B,F,W PACKAGE



TRUTH TABLE

Inputs at t_n		Outputs at t_{n+1}				
J	K	Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
L	H	Q_{An}	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
L	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	L	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

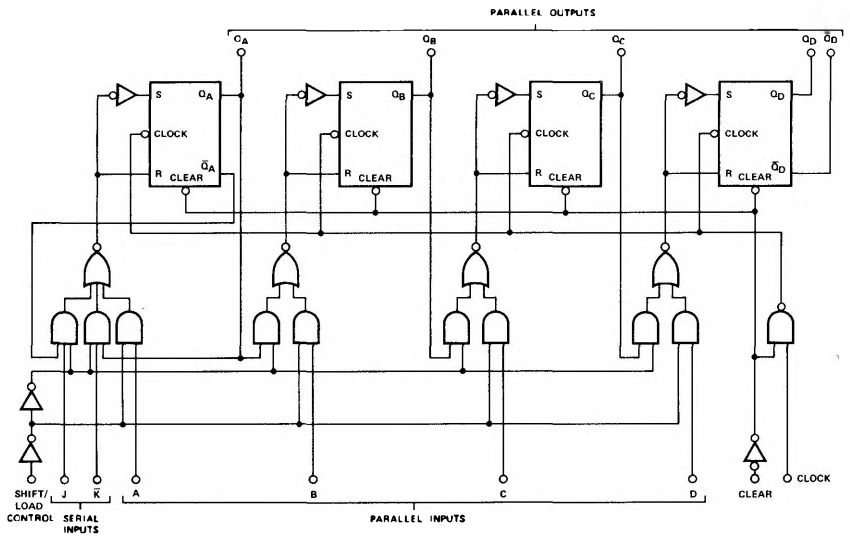
H = High Level, L = Low Level

NOTES A. t_n = bit time before clock pulse

B. t_{n+1} = bit time after clock pulse

C. Q_{An} = state of Q_A at t_n

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

	S54195			N74195			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N: High logic level			20			20	
Low logic level			10			10	
Input Clock Frequency, f_{clock}	0		30	0		30	MHz
Width of Clock Input Pulse, $t_{w(clock)}$	16			16			ns
Width of Clear Input Pulse, $t_{w(clear)}$	12			12			ns
Setup Time, t_{setup}: Shift/load	25			25			
Serial and parallel data	15			15			ns
Clear inactive-state	25			25			
Shift/Load Release Time, $t_{release}$			10			10	ns
Serial and Parallel Data Hold Time, t_{hold}	0			0			ns
Operating Free-Air Temperature, T_A	-55		125	0		70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS *			MIN	TYP**	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = -12mA				-1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OH} = -800μA		2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OL} = 16mA				0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4V				40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4V				-1.6	mA
I_{OS}	Short-circuit output current†	V_{CC} = MAX		S54195	-20		-57	mA
				N74195	-18		-57	
I_{CC}	Supply current	V_{CC} = MAX,	See Note			39	63	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	Maximum input clock frequency	C_L = 15pF,	R_L = 400Ω	30	39		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear				19	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			6	14	22	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			7	17	26	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.

NOTE With all outputs open, shift/load grounded, and 4.5V applied to the J, $\overline{R}$, and data inputs, I_{CC} is measured by applying a momentary ground, followed by 4.5V, to clear, and then applying a momentary ground, followed by 4.5V, to clock.