QUADRUPLE D-TYPE EDGE-TRIGGERED FLIP-FLOPS

S54175
N74175

S54175–B,F,W • N74175–B,F

DIGITAL 54/74 TTL SERIES

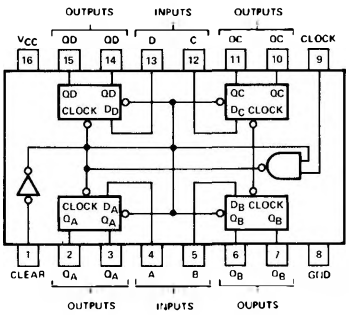
DESCRIPTION

These monolithic, positive-edge-triggered flip-flops utilize TTL circuits to implement the D-type flip-flop logic. Information at input D is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D-input signal has no effect.

These circuits are fully compatible for use with most TTL or DTL circuits. A full fan-out to 10 low logic-level loads and 20 high-logic-level loads is available from each of the outputs. This simplifies system design by allowing unused inputs to be tied to driven inputs. Maximum clock frequency is typically 25 megahertz, with a typical power dissipation of 38 milliwatts per flip-flop.

PIN CONFIGURATION

B,F,W PACKAGE



TRUTH TABLE

INPUT	OUTPUT
t_n	$t_n + 1$
D	Q
H	H
L	L

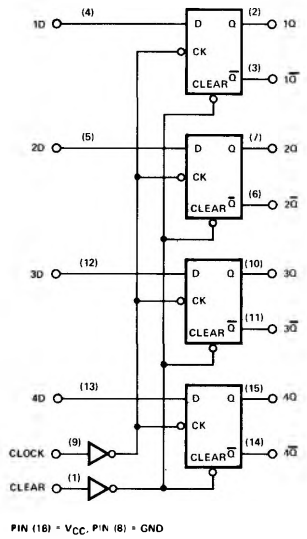
t_n = Bit time before clock pulse transition.
$t_n + 1$ = Bit time after clock pulse transition.

ABSOLUTE MAXIMUM RATINGS (over operating free-air temperature range unless otherwise noted)

Supply voltage V_{CC} (See Note 1)	7 V
Input voltage (See Note 1)	5.5 V
Operating free-air temperature range:	
54175 Circuits	−55°C to 125°C
74175 Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1:
Voltage values are with respect to network ground terminal.

LOGIC DIAGRAM



PIN (16) = V_{CC}, PIN (8) = GND

RECOMMENDED OPERATING CONDITIONS

	54175			74175			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N — High Logic Level			20			20	
Low Logic Level			10			10	
Input clock frequency, f_{clock}	0		25	0		25	MHz
Width of clock or clear pulse, t_W	20			20			ns
Data setup time, t_{setup}	20			20			ns
Hold time t_{hold}	0			0			ns
Operating free-air temperature, T_A	-55	25	125	0	25	70	°C
Clear release setup, $t_{release}$	25			25			ns

ELECTRICAL CHARACTERISTICS (over operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS†		54175			74175			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MAX,	I_I = -12 mA			-1.5			-1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, J_{OH} = -800 μA	2.4			2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2V, J_{OL} = 16 mA			0.4			0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			-1.6			-1.6	mA
I_{OS}	Short-circuit output current	V_{CC} = MAX		-20		-57	-18		-57	mA
I_{CC}	Supply current	V_{CC} = MAX								
		Note 1	54175							
			74175		30	45		30	45	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum input clock frequency		25	35		MHz
t_{PHL}	Propagation delay time, high-to-low-level output Q from clear	C_L = 15 pF R_L = 400		23	35	ns
t_{PLH}	Propagation delay time low-to-high-level output Q from clear (54175, 74175)			16	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			21	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			20	30	ns