Document Number: S32V234RMAD
Rev. 3, 04/2018

S32V234 Supported STCU2 BIST Sequences

Contents

1 Introduction

This document provides information on S32V234 Supported STCU2 BIST Sequences. This is supplementary to the S32V234 Reference Manual available. Read Reference Manual in conjunction with the addendum for a comprehensive understanding. Following Excel sheets are attached in this:

- STCU2_GCR.xls-these registers provide different configuration for self-test
- Self_test_ctrl.xls-Self Test Control configurations

2 MBIST partitions

The memory on this chip that can be tested by STCU2 is partitioned as follows:

MBIST partitions

MBIST partition	Subpartition	Module or other on-chip system	Memory	Beginning address	Ending address
0	0	Cortex-A53 core 0	L1 D-cache data RAM bank 0		
0	1	Cortex-A53 core 0	L1 D-cache data RAM bank 1		
0	2	Cortex-A53 core 0	L1 D-cache data RAM bank 2		
0	3	Cortex-A53 core 0	L1 D-cache data RAM bank 3		
0	4	Cortex-A53 core 0	L1 D-cache data RAM bank 4		
0	5	Cortex-A53 core 0	L1 D-cache data RAM bank 5		
0	6	Cortex-A53 core 0	L1 D-cache data RAM bank 6		
0	7	Cortex-A53 core 0	L1 D-cache data RAM bank 7		
0	8	Cortex-A53 core 0	L1 D-cache tag RAM bank 0		
0	9	Cortex-A53 core 0	L1 D-cache tag RAM bank 1		
0	10	Cortex-A53 core 0	L1 D-cache tag RAM bank 2		
0	11	Cortex-A53 core 0	L1 D-cache tag RAM bank 3		
0	12	Cortex-A53 core 0	L1 D-cache dirty RAM		
0	13	Cortex-A53 core 0	L1 I-cache data RAM bank 0		
0	14	Cortex-A53 core 0	L1 I-cache data RAM bank 1		
0	15	Cortex-A53 core 0	BTAC stage 0 RAM		
0	16	Cortex-A53 core 0	BTAC stage 1 RAM		
0	17	Cortex-A53 core 0	L1 I-cache tag RAM bank 0		
0	18	Cortex-A53 core 0	L1 I-cache tag RAM bank 1		
0	19	Cortex-A53 core 0	TLB RAM bank 0		
0	20	Cortex-A53 core 0	TLB RAM bank 1		
0	21	Cortex-A53 core 0	TLB RAM bank 2		
0	22	Cortex-A53 core 0	TLB RAM bank 3		
0	23	Cortex-A53 core 0	SCU duplicate tag RAM bank 0		
0	24	Cortex-A53 core 0	SCU duplicate tag RAM bank 1		
0	25	Cortex-A53 core 0	SCU duplicate tag RAM bank 2		

Table continues on the next page...

MBIST partition	Subpartition	Module or other on-chip system	Memory	Beginning address	Ending address
0	26	Cortex-A53 core 0	SCU duplicate tag RAM bank 3		
0	27	Cortex-A53-based cluster 0	L2 cache tag RAM bank 0		
0	28	Cortex-A53-based cluster 0	L2 cache tag RAM bank 1		
0	29	Cortex-A53-based cluster 0	L2 cache tag RAM bank 2		
0	30	Cortex-A53-based cluster 0	L2 cache tag RAM bank 3		
0	31	Cortex-A53-based cluster 0	L2 cache tag RAM bank 4		
0	32	Cortex-A53-based cluster 0	L2 cache tag RAM bank 5		
0	33	Cortex-A53-based cluster 0	L2 cache tag RAM bank 6		
0	34	Cortex-A53-based cluster 0	L2 cache tag RAM bank 7		
0	35	Cortex-A53-based cluster 0	L2 cache tag RAM bank 8		
0	36	Cortex-A53-based cluster 0	L2 cache tag RAM bank 9		
0	37	Cortex-A53-based cluster 0	L2 cache tag RAM bank 10		
0	38	Cortex-A53-based cluster 0	L2 cache tag RAM bank 11		
0	39	Cortex-A53-based cluster 0	L2 cache tag RAM bank 12		
0	40	Cortex-A53-based cluster 0	L2 cache tag RAM bank 13		
0	41	Cortex-A53-based cluster 0	L2 cache tag RAM bank 14		
0	42	Cortex-A53-based cluster 0	L2 cache tag RAM bank 15		
0	43	Cortex-A53-based cluster 0	L2 cache victim RAM		
0	44	Cortex-A53 core 1	L1 D-cache data RAM bank 0		
0	45	Cortex-A53 core 1	L1 D-cache data RAM bank 1		
0	46	Cortex-A53 core 1	L1 D-cache data RAM bank 2		
0	47	Cortex-A53 core 1	L1 D-cache data RAM bank 3		
0	48	Cortex-A53 core 1	L1 D-cache data RAM bank 4		

Table continues on the next page...

MBIST partitions

MBIST partition	Subpartition	Module or other on-chip system	Memory	Beginning address	Ending address
0	49	Cortex-A53 core 1	L1 D-cache data RAM bank 5		
0	50	Cortex-A53 core 1	L1 D-cache data RAM bank 6		
0	51	Cortex-A53 core 1	L1 D-cache data RAM bank 7		
0	52	Cortex-A53 core 1	L1 D-cache tag RAM bank 0		
0	53	Cortex-A53 core 1	L1 D-cache tag RAM bank 1		
0	54	Cortex-A53 core 1	L1 D-cache tag RAM bank 2		
0	55	Cortex-A53 core 1	L1 D-cache tag RAM bank 3		
0	56	Cortex-A53 core 1	L1 D-cache dirty RAM		
0	57	Cortex-A53 core 1	L1 I-cache data RAM bank 0		
0	58	Cortex-A53 core 1	L1 I-cache data RAM bank 1		
0	59	Cortex-A53 core 1	BTAC stage 0 RAM		
0	60	Cortex-A53 core 1	BTAC stage 1 RAM		
0	61	Cortex-A53 core 1	L1 I-cache tag RAM bank 0		
0	62	Cortex-A53 core 1	L1 I-cache tag RAM bank 1		
0	63	Cortex-A53 core 1	TLB RAM bank 0		
0	64	Cortex-A53 core 1	TLB RAM bank 1		
0	65	Cortex-A53 core 1	TLB RAM bank 2		
0	66	Cortex-A53 core 1	TLB RAM bank 3		
0	67	Cortex-A53 core 1	SCU duplicate tag RAM bank 0		
0	68	Cortex-A53 core 1	SCU duplicate tag RAM bank 1		
0	69	Cortex-A53 core 1	SCU duplicate tag RAM bank 2		
0	70	Cortex-A53 core 1	SCU duplicate tag RAM bank 3		
1	0	Cortex-A53 core 2	L1 D-cache data RAM bank 0		
1	1	Cortex-A53 core 2	L1 D-cache data RAM bank 1		
1	2	Cortex-A53 core 2	L1 D-cache data RAM bank 2		
1	3	Cortex-A53 core 2	L1 D-cache data RAM bank 3		

Table continues on the next page...

MBIST partition	Subpartition	Module or other on-chip system	Memory	Beginning address	Ending address
1	4	Cortex-A53 core 2	L1 D-cache data RAM bank 4		
1	5	Cortex-A53 core 2	L1 D-cache data RAM bank 5		
1	6	Cortex-A53 core 2	L1 D-cache data RAM bank 6		
1	7	Cortex-A53 core 2	L1 D-cache data RAM bank 7		
1	8	Cortex-A53 core 2	L1 D-cache tag RAM bank 0		
1	9	Cortex-A53 core 2	L1 D-cache tag RAM bank 1		
1	10	Cortex-A53 core 2	L1 D-cache tag RAM bank 2		
1	11	Cortex-A53 core 2	L1 D-cache tag RAM bank 3		
1	12	Cortex-A53 core 2	L1 D-cache dirty RAM		
1	13	Cortex-A53 core 2	L1 I-cache data RAM bank 0		
1	14	Cortex-A53 core 2	L1 I-cache data RAM bank 1		
1	15	Cortex-A53 core 2	BTAC stage 0 RAM		
1	16	Cortex-A53 core 2	BTAC stage 1 RAM		
1	17	Cortex-A53 core 2	L1 I-cache tag RAM bank 0		
1	18	Cortex-A53 core 2	L1 I-cache tag RAM bank 1		
1	19	Cortex-A53 core 2	TLB RAM bank 0		
1	20	Cortex-A53 core 2	TLB RAM bank 1		
1	21	Cortex-A53 core 2	TLB RAM bank 2		
1	22	Cortex-A53 core 2	TLB RAM bank 3		
1	23	Cortex-A53 core 2	SCU duplicate tag RAM bank 0		
1	24	Cortex-A53 core 2	SCU duplicate tag RAM bank 1		
1	25	Cortex-A53 core 2	SCU duplicate tag RAM bank 2		
1	26	Cortex-A53 core 2	SCU duplicate tag RAM bank 3		
1	27	Cortex-A53-based cluster 1	L2 cache tag RAM bank 0		
1	28	Cortex-A53-based cluster 1	L2 cache tag RAM bank 1		
1	29	Cortex-A53-based cluster 1	L2 cache tag RAM bank 2		

Table continues on the next page...

MBIST partitions

MBIST partition	Subpartition	Module or other on-chip system	Memory	Beginning address	Ending address
1	30	Cortex-A53-based cluster 1	L2 cache tag RAM bank 3		
1	31	Cortex-A53-based cluster 1	L2 cache tag RAM bank 4		
1	32	Cortex-A53-based cluster 1	L2 cache tag RAM bank 5		
1	33	Cortex-A53-based cluster 1	L2 cache tag RAM bank 6		
1	34	Cortex-A53-based cluster 1	L2 cache tag RAM bank 7		
1	35	Cortex-A53-based cluster 1	L2 cache tag RAM bank 8		
1	36	Cortex-A53-based cluster 1	L2 cache tag RAM bank 9		
1	37	Cortex-A53-based cluster 1	L2 cache tag RAM bank 10		
1	38	Cortex-A53-based cluster 1	L2 cache tag RAM bank 11		
1	39	Cortex-A53-based cluster 1	L2 cache tag RAM bank 12		
1	40	Cortex-A53-based cluster 1	L2 cache tag RAM bank 13		
1	41	Cortex-A53-based cluster 1	L2 cache tag RAM bank 14		
1	42	Cortex-A53-based cluster 1	L2 cache tag RAM bank 15		
1	43	Cortex-A53-based cluster 1	L2 cache victim RAM		
1	44	Cortex-A53 core 3	L1 D-cache data RAM bank 0		
1	45	Cortex-A53 core 3	L1 D-cache data RAM bank 1		
1	46	Cortex-A53 core 3	L1 D-cache data RAM bank 2		
1	47	Cortex-A53 core 3	L1 D-cache data RAM bank 3		
1	48	Cortex-A53 core 3	L1 D-cache data RAM bank 4		
1	49	Cortex-A53 core 3	L1 D-cache data RAM bank 5		
1	50	Cortex-A53 core 3	L1 D-cache data RAM bank 6		
1	51	Cortex-A53 core 3	L1 D-cache data RAM bank 7		
1	52	Cortex-A53 core 3	L1 D-cache tag RAM bank 0		

Table continues on the next page...

MBIST partition	Subpartition	Module or other on-chip system	Memory	Beginning address	Ending address
1	53	Cortex-A53 core 3	L1 D-cache tag RAM bank 1		
1	54	Cortex-A53 core 3	L1 D-cache tag RAM bank 2		
1	55	Cortex-A53 core 3	L1 D-cache tag RAM bank 3		
1	56	Cortex-A53 core 3	L1 D-cache dirty RAM		
1	57	Cortex-A53 core 3	L1 I-cache data RAM bank 0		
1	58	Cortex-A53 core 3	L1 I-cache data RAM bank 1		
1	59	Cortex-A53 core 3	BTAC stage 0 RAM		
1	60	Cortex-A53 core 3	BTAC stage 1 RAM		
1	61	Cortex-A53 core 3	L1 I-cache tag RAM bank 0		
1	62	Cortex-A53 core 3	L1 I-cache tag RAM bank 1		
1	63	Cortex-A53 core 3	TLB RAM bank 0		
1	64	Cortex-A53 core 3	TLB RAM bank 1		
1	65	Cortex-A53 core 3	TLB RAM bank 2		
1	66	Cortex-A53 core 3	TLB RAM bank 3		
1	67	Cortex-A53 core 3	SCU duplicate tag RAM bank 0		
1	68	Cortex-A53 core 3	SCU duplicate tag RAM bank 1		
1	69	Cortex-A53 core 3	SCU duplicate tag RAM bank 2		
1	70	Cortex-A53 core 3	SCU duplicate tag RAM bank 3		
2	0	Cortex-A53-based cluster 0	L2 cache data RAM banks 0–1		
2	1	Cortex-A53-based cluster 0	L2 cache data RAM banks 2–3		
2	2	Cortex-A53-based cluster 0	L2 cache data RAM banks 4–5		
2	3	Cortex-A53-based cluster 0	L2 cache data RAM banks 6–7		
3	0	Cortex-A53-based cluster 1	L2 cache data RAM banks 0–1		
3	1	Cortex-A53-based cluster 1	L2 cache data RAM banks 2–3		
3	2	Cortex-A53-based cluster 1	L2 cache data RAM banks 4–5		
3	3	Cortex-A53-based cluster 1	L2 cache data RAM banks 6–7		

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MBIST partitions

MBIST partition	Subpartition	Module or other on-chip system	Memory	Beginning address	Ending address
4	0	VIULite_0	FIFO SRAM	—	—
5	0	VIULite_1	FIFO SRAM	—	—
6	0	Boot ROM	ROM	0000_0000h	007F_FFFFh
7	0	(Reserved)	(Reserved)	—	—
7	1	DCU (2D-ACE)	Gamma R RAM	4002_B000h	4002_B3FFh
7	2	DCU (2D-ACE)	Gamma B RAM	4002_B800h	4002_BBFFh
7	3	DCU (2D-ACE)	Gamma G RAM	4002_B400h	4002_B7FFh
7	4	DCU (2D-ACE)	Input buffer MEM bank 0		
7	5	DCU (2D-ACE)	Input buffer MEM bank 1		
7	6	DCU (2D-ACE)	Input buffer MEM bank 2		
7	7	DCU (2D-ACE)	Input buffer MEM bank 3		
7	8	DCU (2D-ACE)	Layer MEM		
7	9	DCU (2D-ACE)	Palette MEM	4002_9000h	4002_AFFFh
7	10	DCU (2D-ACE)	Tile MEM bank 0		
7	11	DCU (2D-ACE)	Tile MEM bank 1		
8	0	PCIE	Master composition MEM		
8	1	PCIE	Receive queue data MEM		
8	2	PCIE	Receive queue header MEM bank 0		
8	3	PCIE	Receive queue header MEM bank 1		
8	4	PCIE	Transmit retry buffer MEM		
8	5	PCIE	Read buffer MEM		
9	0	FR (FlexRay)	Flexray-133 DRAM bank 0		
9	1	FR (FlexRay)	Flexray-133 DRAM bank 1		
10	0	Cortex-A53-based cluster 0	ETF RAM bank 0		
11	0	Cortex-A53-based cluster 1	ETF RAM bank 1		
12	0	CAN_0 (FlexCAN)	MEM bank 0		
12	1	CAN_0 (FlexCAN)	MEM bank 1		
13	0	CAN_1 (FlexCAN)	MEM bank 0		
13	1	CAN_1 (FlexCAN)	MEM bank 1		
14	0	Cortex-M4 core	D-cache DRAM bank 0		
14	1	Cortex-M4 core	D-cache DRAM bank 1		

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MBIST partition	Subpartition	Module or other on-chip system	Memory	Beginning address	Ending address
14	2	Cortex-M4 core	D-cache TRAM bank 0		
14	3	Cortex-M4 core	D-cache TRAM bank 1		
14	4	Cortex-M4 core	ETF RAM		
14	5	Cortex-M4 core	I-cache DRAM bank 0		
14	6	Cortex-M4 core	I-cache DRAM bank 1		
14	7	Cortex-M4 core	I-cache TRAM bank 0		
14	8	Cortex-M4 core	I-cache TRAM bank 1		
14	9	Cortex-M4 core	TCM upper MEM bank 0		
14	10	Cortex-M4 core	TCM lower MEM bank 0		
15	0	(Reserved)	(Reserved)		
16	0	ENET	Receive MEM		
16	1	ENET	RXP L MEM		
16	2	ENET	RXP U MEM		
16	3	ENET	Transmit MEM		
17	0	FDMA	Transmit buffer MEM bank 0		
17	1	FDMA	Transmit buffer MEM bank 1		
18	0	FR (FlexRay)	Flexray-80 DRAM		
19	0	IPSU	IPUS0 HIST MEM		
19	1	IPSU	IPUS1 HIST MEM		
19	2	IPSU	IPUS2 HIST MEM		
19	3	IPSU	IPUS2 LUT MEM		
19	4	IPSU	IPUS3 HIST MEM		
19	5	IPSU	IPUS3 LUT MEM		
19	6	IPSU	IPUS7 STAT MEM		
20	0	JPEG (JPEG Decoder)	Quantization table 1 MEM		
20	1	JPEG (JPEG Decoder)	Quantization table 2 MEM		
20	2	JPEG (JPEG Decoder)	Quantization table 3 MEM		
20	3	JPEG (JPEG Decoder)	Quantization table 4 MEM		
20	4	JPEG (JPEG Decoder)	Huffman decoder FIFO output MEM		
20	5	JPEG (JPEG Decoder)	Huffman table MEM		
21	0	MMDC_0 and MMDC_1	ETF MEM		
22	0	QuadSPI	Buffer MEM		
23	0	VSEQ	PRAM		
23	1	VSEQ	CRAM		

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MBIST partitions

MBIST partition	Subpartition	Module or other on-chip system	Memory	Beginning address	Ending address
24	0	SRAM-1M (0-3)	Segment 1 bank 0		
24	1	SRAM-1M (0-3)	Segment 1 bank 1		
24	2	SRAM-1M (0-3)	Segment 1 bank 2		
24	3	SRAM-1M (0-3)	Segment 1 bank 3		
25	0	SRAM-1M (4-7)	Segment 1 bank 4		
25	1	SRAM-1M (4-7)	Segment 1 bank 5		
25	2	SRAM-1M (4-7)	Segment 1 bank 6		
25	3	SRAM-1M (4-7)	Segment 1 bank 7		
26	0	SRAM-1M (8-11)	Segment 2 bank 0		
26	1	SRAM-1M (8-11)	Segment 2 bank 1		
26	2	SRAM-1M (8-11)	Segment 2 bank 2		
26	3	SRAM-1M (8-11)	Segment 2 bank 3		
27	0	SRAM-1M (12-15)	Segment 2 bank 4		
27	1	SRAM-1M (12-15)	Segment 2 bank 5		
27	2	SRAM-1M (12-15)	Segment 2 bank 6		
27	3	SRAM-1M (12-15)	Segment 2 bank 7		
28	0	SRAM-3M (0-3)	Segment 0 bank 0		
28	1	SRAM-3M (0-3)	Segment 0 bank 1		
28	2	SRAM-3M (0-3)	Segment 0 bank 2		
28	3	SRAM-3M (0-3)	Segment 0 bank 3		
29	0	SRAM-3M (4-7)	Segment 0 bank 4		
29	1	SRAM-3M (4-7)	Segment 0 bank 5		
29	2	SRAM-3M (4-7)	Segment 0 bank 6		
29	3	SRAM-3M (4-7)	Segment 0 bank 7		
30	0	SRAM-3M (8-11)	Segment 0 bank 8		
30	1	SRAM-3M (8-11)	Segment 0 bank 9		
30	2	SRAM-3M (8-11)	Segment 0 bank 10		
30	3	SRAM-3M (8-11)	Segment 0 bank 11		
31	0	SRAM-3M (12-15)	Segment 0 bank 12		
31	1	SRAM-3M (12-15)	Segment 0 bank 13		
31	2	SRAM-3M (12-15)	Segment 0 bank 14		
31	3	SRAM-3M (12-15)	Segment 0 bank 15		
32	0	SRAM-3M (16-19)	Segment 0 bank 16		
32	1	SRAM-3M (16-19)	Segment 0 bank 17		
32	2	SRAM-3M (16-19)	Segment 0 bank 18		
32	3	SRAM-3M (16-19)	Segment 0 bank 19		
33	0	SRAM-3M (20-23)	Segment 0 bank 20		
33	1	SRAM-3M (20-23)	Segment 0 bank 21		
33	2	SRAM-3M (20-23)	Segment 0 bank 22		
33	3	SRAM-3M (20-23)	Segment 0 bank 23		

Table continues on the next page...

MBIST partition	Subpartition	Module or other on-chip system	Memory	Beginning address	Ending address
34	0	APEX_0 (APEX-CL)	CMEM bank 0		
34	1	APEX_0 (APEX-CL)	CMEM bank 1		
34	2	APEX_0 (APEX-CL)	CMEM bank 2		
34	3	APEX_0 (APEX-CL)	CMEM bank 3		
34	4	APEX_0 (APEX-CL)	CMEM bank 4		
34	5	APEX_0 (APEX-CL)	CMEM bank 5		
34	6	APEX_0 (APEX-CL)	CMEM bank 6		
34	7	APEX_0 (APEX-CL)	CMEM bank 7		
34	8	APEX_0 (APEX-CL)	CMEM bank 8		
34	9	APEX_0 (APEX-CL)	CMEM bank 9		
34	10	APEX_0 (APEX-CL)	CMEM bank 10		
34	11	APEX_0 (APEX-CL)	CMEM bank 11		
34	12	APEX_0 (APEX-CL)	CMEM bank 12		
34	13	APEX_0 (APEX-CL)	CMEM bank 13		
34	14	APEX_0 (APEX-CL)	CMEM bank 14		
34	15	APEX_0 (APEX-CL)	CMEM bank 15		
34	16	APEX_0 (APEX-CL)	DMEM bank 0		
34	17	APEX_0 (APEX-CL)	DMEM bank 1		
34	18	APEX_0 (APEX-CL)	IMEM bank 0		
34	19	APEX_0 (APEX-CL)	IMEM bank 1		
35	0	APEX_1 (APEX-CL)	CMEM bank 0		
35	1	APEX_1 (APEX-CL)	CMEM bank 1		
35	2	APEX_1 (APEX-CL)	CMEM bank 2		
35	3	APEX_1 (APEX-CL)	CMEM bank 3		
35	4	APEX_1 (APEX-CL)	CMEM bank 4		
35	5	APEX_1 (APEX-CL)	CMEM bank 5		
35	6	APEX_1 (APEX-CL)	CMEM bank 6		
35	7	APEX_1 (APEX-CL)	CMEM bank 7		
35	8	APEX_1 (APEX-CL)	CMEM bank 8		
35	9	APEX_1 (APEX-CL)	CMEM bank 9		
35	10	APEX_1 (APEX-CL)	CMEM bank 10		
35	11	APEX_1 (APEX-CL)	CMEM bank 11		
35	12	APEX_1 (APEX-CL)	CMEM bank 12		
35	13	APEX_1 (APEX-CL)	CMEM bank 13		
35	14	APEX_1 (APEX-CL)	CMEM bank 14		
35	15	APEX_1 (APEX-CL)	CMEM bank 15		
35	16	APEX_1 (APEX-CL)	DMEM bank 0		
35	17	APEX_1 (APEX-CL)	DMEM bank 1		
35	18	APEX_1 (APEX-CL)	IMEM bank 0		
35	19	APEX_1 (APEX-CL)	IMEM bank 1		

Table continues on the next page...

MBIST partitions

MBIST partition	Subpartition	Module or other on-chip system	Memory	Beginning address	Ending address
36	0	H264_ENC	Core 1 IPR MEM		
36	1	H264_ENC	Core 1 IPR MEM		
36	2	H264_ENC	Core 1 IPR MEM		
36	3	H264_ENC	Core 1 IPR MEM		
36	4	H264_ENC	Core 1 IPR MEM		
36	5	H264_ENC	Core 1 IPR MEM		
36	6	H264_ENC	Core 1 IPR MEM		
36	7	H264_ENC	Core 1 IPR MEM		
36	8	H264_ENC	Core 1 IPR MEM		
36	9	H264_ENC	Core 1 IPR MEM		
36	10	H264_ENC	Core 1 IPR MEM		
37	0	DEC200	Encoder MEM bank 0		
37	1	DEC200	Encoder MEM bank 1_0		
37	2	DEC200	Encoder MEM bank 1_1		
38	-	(Reserved)	(Reserved)	—	—
39	0	FDMA (FastDMA)	Queue MEM bank 0		
39	1	FDMA (FastDMA)	Queue MEM bank 1		
40	0	VSEQ	KRAM		
41	0	EDMA	DMA RAM		
42	0	H264_DEC	Reconstruction double buffer channel 3 MEM A bank 0		
42	1	H264_DEC	Reconstruction double buffer channel 3 MEM A bank 1		
42	2	H264_DEC	Reconstruction double buffer channel 0 MEM A bank 0		
42	3	H264_DEC	Reconstruction double buffer channel 0 MEM A bank 1		
42	4	H264_DEC	Reconstruction double buffer channel 0 MEM B bank 0		
42	5	H264_DEC	Reconstruction double buffer channel 0 MEM B bank 1		
42	6	H264_DEC	Reconstruction double buffer channel 1 MEM A bank 0		
42	7	H264_DEC	Reconstruction double buffer channel 1 MEM A bank 1		

Table continues on the next page...

MBIST partition	Subpartition	Module or other on-chip system	Memory	Beginning address	Ending address
42	8	H264_DEC	Reconstruction double buffer channel 1 MEM B bank 0		
42	9	H264_DEC	Reconstruction double buffer channel 1 MEM B bank 1		
42	10	H264_DEC	Reconstruction double buffer channel 2 MEM A bank 0		
42	11	H264_DEC	Reconstruction double buffer channel 2 MEM A bank 1		
42	12	H264_DEC	Reconstruction double buffer channel 2 MEM B bank 0		
42	13	H264_DEC	Reconstruction double buffer channel 2 MEM B bank 1		
42	14	H264_DEC	Reconstruction double buffer channel 3 MEM B bank 0		
42	15	H264_DEC	Reconstruction double buffer channel 3 MEM B bank 1		
43	0	H264_ENC	Core 0 VLC MEM		
43	1	H264_ENC	Core 0 VLC MEM		
43	2	H264_ENC	Core 1 VLC MEM		
43	3	H264_ENC	Core 1 VLC MEM		
43	4	H264_ENC	Core 0 VLC MEM		
43	5	H264_ENC	Core 0 VLC MEM		
43	6	H264_ENC	Core 0 VLC MEM		
43	7	H264_ENC	Core 0 VLC MEM		
43	8	H264_ENC	Core 1 VLC MEM		
44	0	H264_ENC	Core 0 IPR MEM		
44	1	H264_ENC	Core 0 IPR MEM		
44	2	H264_ENC	Core 0 IPR MEM		
44	3	H264_ENC	Core 0 IPR MEM		
44	4	H264_ENC	Core 0 IPR MEM		
44	5	H264_ENC	Core 0 IPR MEM		
44	6	H264_ENC	Core 0 IPR MEM		
44	7	H264_ENC	Core 0 IPR MEM		
44	8	H264_ENC	Core 0 IPR MEM		
44	9	H264_ENC	Core 0 IPR MEM		
44	10	H264_ENC	Core 0 IPR MEM		
45	0	H264_ENC	Core 0 VLC MEM		

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MBIST partitions

MBIST partition	Subpartition	Module or other on-chip system	Memory	Beginning address	Ending address
45	1	H264_ENC	Core 0 VLC MEM		
45	2	H264_ENC	Core 0 VLC MEM		
45	3	H264_ENC	Core 0 VLC MEM		
45	4	H264_ENC	Core 1 VLC MEM		
45	5	H264_ENC	Core 1 VLC MEM		
45	6	H264_ENC	Core 1 VLC MEM		
45	7	H264_ENC	Core 1 VLC MEM		
45	8	H264_ENC	Core 1 VLC MEM		
45	9	H264_ENC	Core 1 VLC MEM		
45	10	H264_ENC	Core 1 VLC MEM		
45	11	H264_ENC	Core 0 bit-stream buffer bank 0		
45	12	H264_ENC	Core 0 bit-stream buffer bank 1		
45	13	H264_ENC	Core 1 bit-stream buffer bank 0		
45	14	H264_ENC	Core 1 bit-stream buffer bank 1		
45	15	H264_ENC	Common emulation prevention FIFO MEM bank 0		
45	16	H264_ENC	Common emulation prevention FIFO MEM bank 1		
45	17	H264_ENC	Common bitstream buffer MEM		
46	0	H264_DEC	Residual MEM bank 0		
46	1	H264_DEC	Residual MEM bank 1		
46	2	H264_DEC	Residual MEM bank 2		
46	3	H264_DEC	Residual MEM bank 3		
47	0	H264_DEC	IPR border pixel row MEM bank 0		
47	1	H264_DEC	IPR border pixel row MEM bank 1		
47	2	H264_DEC	IPR border pixel row MEM bank 2		
47	3	H264_DEC	IPR border pixel row MEM bank 3		
48	0	H264_DEC	AXI write bridge FIFO MEM		
48	1	H264_DEC	Deblocking filter MEM bank 0		
48	2	H264_DEC	Deblocking filter MEM bank 1		

Table continues on the next page...

MBIST partition	Subpartition	Module or other on-chip system	Memory	Beginning address	Ending address
48	3	H264_DEC	Deblocking filter MEM bank 2		
48	4	H264_DEC	Deblocking filter MEM bank 3		
48	5	H264_DEC	AXI read bridge FIFO MEM		
48	6	H264_DEC	AXI read bridge FIFO MEM		
48	7	H264_DEC	AXI write bridge FIFO MEM		
48	8	H264_DEC	AXI write bridge FIFO MEM		
48	9	H264_DEC	Port splitter A FIFO MEM bank 0		
48	10	H264_DEC	Port splitter B FIFO MEM bank 0		
48	11	H264_DEC	Port splitter C FIFO MEM bank 0		
48	12	H264_DEC	Port splitter D FIFO MEM bank 0		
48	13	H264_DEC	Port splitter A FIFO MEM bank 1		
48	14	H264_DEC	Port splitter B FIFO MEM bank 1		
48	15	H264_DEC	Port splitter C FIFO MEM bank 1		
48	16	H264_DEC	Port splitter D FIFO MEM bank 1		
49	0	H264_DEC	VLD 0 MEM		
49	1	H264_DEC	VLD 0 MEM		
49	2	H264_DEC	VLD 0 MEM		
49	3	H264_DEC	VLD 0 MEM		
49	4	H264_DEC	VLD 1 MEM		
49	5	H264_DEC	VLD 1 MEM		
49	6	H264_DEC	VLD 1 MEM		
49	7	H264_DEC	VLD 1 MEM		
49	8	H264_DEC	VLD 2 MEM		
49	9	H264_DEC	VLD 2 MEM		
49	10	H264_DEC	VLD 2 MEM		
49	11	H264_DEC	VLD 2 MEM		
49	12	H264_DEC	VLD 3 MEM		
49	13	H264_DEC	VLD 3 MEM		
49	14	H264_DEC	VLD 3 MEM		
49	15	H264_DEC	VLD 3 MEM		

Table continues on the next page...

MBIST partitions

MBIST partition	Subpartition	Module or other on-chip system	Memory	Beginning address	Ending address
50	0	H264_DEC	VLD 0 MEM		
50	1	H264_DEC	VLD 0 MEM		
50	2	H264_DEC	MC output data MEM		
50	3	H264_DEC	VLD 0 MEM		
50	4	H264_DEC	VLD 0 MEM		
50	5	H264_DEC	VLD 1 MEM		
50	6	H264_DEC	VLD 2 MEM		
50	7	H264_DEC	VLD 3 MEM		
50	8	H264_DEC	VLD 0 MEM		
50	9	H264_DEC	VLD 1 MEM		
50	10	H264_DEC	VLD 2 MEM		
50	11	H264_DEC	VLD 3 MEM		
51	0	H264_DEC	MC cache data MEM bank 0		
51	1	H264_DEC	MC cache data MEM bank 1		
51	2	H264_DEC	Video output 0 MEM A bank 0		
51	3	H264_DEC	Video output 0 MEM A bank 1		
51	4	H264_DEC	Video output 0 MEM B bank 0		
51	5	H264_DEC	Video output 0 MEM B bank 1		
51	6	H264_DEC	Video output 1 MEM A bank 0		
51	7	H264_DEC	Video output 1 MEM A bank 1		
51	8	H264_DEC	Video output 1 MEM B bank 0		
51	9	H264_DEC	Video output 1 MEM B bank 1		
51	10	H264_DEC	Video output 2 MEM A bank 0		
51	11	H264_DEC	Video output 2 MEM A bank 1		
51	12	H264_DEC	Video output 2 MEM B bank 0		
51	13	H264_DEC	Video output 2 MEM B bank 1		
51	14	H264_DEC	Video output 3 MEM A bank 0		
51	15	H264_DEC	Video output 3 MEM A bank 1		

Table continues on the next page...

MBIST partition	Subpartition	Module or other on-chip system	Memory	Beginning address	Ending address
51	16	H264_DEC	Video output 3 MEM B bank 0		
51	17	H264_DEC	Video output 3 MEM B bank 1		
52	0	H264_ENC	Core 0 IPR MEM		
52	1	H264_ENC	Core 0 IPR MEM		
52	2	H264_ENC	Core 1 IPR MEM		
52	3	H264_ENC	Core 1 IPR MEM		
52	4	H264_ENC	Core 0 IPR MEM		
52	5	H264_ENC	Core 0 IPR MEM		
52	6	H264_ENC	Core 0 IPR MEM		
52	7	H264_ENC	Core 0 IPR MEM		
52	8	H264_ENC	Core 1 IPR MEM		
52	9	H264_ENC	Core 1 IPR MEM		
52	10	H264_ENC	Core 1 IPR MEM		
52	11	H264_ENC	Core 1 IPR MEM		
53	0	H264_ENC	Core 0 IPR ROM		
53	1	H264_ENC	Core 1 IPR ROM		
54	0	H264_DEC	Deblocking filter ROM bank 0		
54	1	H264_DEC	Deblocking filter ROM bank 1		
54	2	H264_DEC	Deblocking filter ROM bank 2		
54	3	H264_DEC	Deblocking filter ROM bank 3		
55	0	H264_DEC	Deblocking filter MEM 0		
55	1	H264_DEC	Deblocking filter MEM 0		
55	2	H264_DEC	Deblocking filter MEM 0		
55	3	H264_DEC	Deblocking filter MEM 0		
55	4	H264_DEC	Deblocking filter MEM 0		
55	5	H264_DEC	Deblocking filter MEM 0		
55	6	H264_DEC	Deblocking filter MEM 0		
55	7	H264_DEC	Deblocking filter MEM 0		
55	8	H264_DEC	Deblocking filter MEM 1		
55	9	H264_DEC	Deblocking filter MEM 1		
55	10	H264_DEC	Deblocking filter MEM 1		
55	11	H264_DEC	Deblocking filter MEM 1		
55	12	H264_DEC	Deblocking filter MEM 1		
55	13	H264_DEC	Deblocking filter MEM 1		
55	14	H264_DEC	Deblocking filter MEM 1		
55	15	H264_DEC	Deblocking filter MEM 1		

Table continues on the next page...

MBIST partitions

MBIST partition	Subpartition	Module or other on-chip system	Memory	Beginning address	Ending address
56	0	H264_DEC	Deblocking filter MEM 2		
56	1	H264_DEC	Deblocking filter MEM 2		
56	2	H264_DEC	Deblocking filter MEM 2		
56	3	H264_DEC	Deblocking filter MEM 2		
56	4	H264_DEC	Deblocking filter MEM 2		
56	5	H264_DEC	Deblocking filter MEM 2		
56	6	H264_DEC	Deblocking filter MEM 2		
56	7	H264_DEC	Deblocking filter MEM 2		
56	8	H264_DEC	Deblocking filter MEM 3		
56	9	H264_DEC	Deblocking filter MEM 3		
56	10	H264_DEC	Deblocking filter MEM 3		
56	11	H264_DEC	Deblocking filter MEM 3		
56	12	H264_DEC	Deblocking filter MEM 3		
56	13	H264_DEC	Deblocking filter MEM 3		
56	14	H264_DEC	Deblocking filter MEM 3		
56	15	H264_DEC	Deblocking filter MEM 3		
57	0	GC3000	RAM0_MEM0		
57	1	GC3000	RAM1_MEM0		
57	2	GC3000	RAM2_MEM0		
57	3	GC3000	RAM3_MEM0		
57	4	GC3000	RAM4_MEM0		
57	5	GC3000	RAM5_MEM0		
57	6	GC3000	RAM6_MEM0		
57	7	GC3000	RAM7_MEM0		
57	8	GC3000	RAM8_MEM0		
57	9	GC3000	RAM9_MEM0		
57	10	GC3000	RAM10_MEM0		
58	0	GC3000	RAM15_MEM0		
58	1	GC3000	RAM16_MEM0		
58	2	GC3000	RAM17_MEM0		
58	3	GC3000	RAM18_MEM0		
58	4	GC3000	RAM19_MEM0		
58	5	GC3000	RAM20_MEM0		
58	6	GC3000	RAM21_MEM0		
58	7	GC3000	RAM22_MEM0		
58	8	GC3000	RAM23_MEM0		
58	9	GC3000	RAM24_MEM0		
58	10	GC3000	RAM25_MEM0		
58	11	GC3000	RAM26_MEM0		
58	12	GC3000	RAM27_MEM0		

Table continues on the next page...

MBIST partition	Subpartition	Module or other on-chip system	Memory	Beginning address	Ending address
58	13	GC3000	RAM28_MEM1		
58	14	GC3000	RAM29_MEM0		
58	15	GC3000	RAM30_MEM1		
58	16	GC3000	RAM31_MEM0		
58	17	GC3000	RAM32_MEM0		
58	18	GC3000	RAM33_MEM0		
58	19	GC3000	RAM34_MEM0		
59	0	GC3000	RAM35_MEM0		
59	1	GC3000	RAM36_MEM0		
59	2	GC3000	RAM37_MEM0		
59	3	GC3000	RAM38_MEM0		
59	4	GC3000	RAM39_MEM0		
59	5	GC3000	RAM40_MEM0		
59	6	GC3000	RAM41_MEM0		
59	7	GC3000	RAM42_MEM0		
59	8	GC3000	RAM43_MEM0		
59	9	GC3000	RAM44_MEM0		
59	10	GC3000	RAM45_MEM1		
59	11	GC3000	RAM46_MEM0		
59	12	GC3000	RAM47_MEM1		
59	13	GC3000	RAM48_MEM0		
59	14	GC3000	RAM49_MEM0		
59	15	GC3000	RAM50_MEM0		
59	16	GC3000	RAM51_MEM0		
60	0	GC3000	RAM52_MEM0		
60	1	GC3000	RAM53_MEM1		
60	2	GC3000	RAM54_MEM2		
60	3	GC3000	RAM55_MEM3		
60	4	GC3000	RAM56_MEM0		
60	5	GC3000	RAM57_MEM1		
60	6	GC3000	RAM58_MEM2		
60	7	GC3000	RAM59_MEM3		
60	8	GC3000	RAM80_MEM0		
60	9	GC3000	RAM81_MEM0		
60	10	GC3000	RAM82_MEM0		
60	11	GC3000	RAM83_MEM0		
60	12	GC3000	RAM84_MEM0		
61	0	GC3000	RAM86_MEM0		
61	1	GC3000	RAM87_MEM0		
61	2	GC3000	RAM88_MEM0		

Table continues on the next page...

MBIST partitions

MBIST partition	Subpartition	Module or other on-chip system	Memory	Beginning address	Ending address
61	3	GC3000	RAM89_MEM0		
61	4	GC3000	RAM90_MEM0		
61	5	GC3000	RAM91_MEM0		
61	6	GC3000	RAM92_MEM0		
61	7	GC3000	RAM93_MEM0		
61	8	GC3000	RAM94_MEM1		
62	0	DEC200	Decoder MEM bank 0		
62	1	DEC200	Decoder MEM bank 1		
63	0	GC3000	RAM97_MEM0		
63	1	GC3000	RAM98_MEM0		
63	2	GC3000	RAM99_MEM0		
63	3	GC3000	RAM100_MEM1		
63	4	GC3000	RAM101_MEM0		
63	5	GC3000	RAM102_MEM1		
63	6	GC3000	RAM103_MEM0		
63	7	GC3000	RAM104_MEM1		
63	8	GC3000	RAM105_MEM0		
63	9	GC3000	RAM106_MEM1		
63	10	GC3000	RAM107_MEM0		
63	11	GC3000	RAM108_MEM0		
64	0	GC3000	RAM11_MEM0		
64	1	GC3000	RAM12_MEM0		
64	2	GC3000	RAM13_MEM0		
64	3	GC3000	RAM14_MEM0		
65	0	GC3000	RAM142_MEM0		
65	1	GC3000	RAM143_MEM1		
65	2	GC3000	RAM144_MEM0		
66	0	GC3000	RAM184_MEM0		
66	1	GC3000	RAM185_MEM0		
66	2	GC3000	RAM186_MEM0		
66	3	GC3000	RAM186_MEM1		
66	4	GC3000	RAM186_MEM2		
66	5	GC3000	RAM186_MEM3		
66	6	GC3000	RAM187_MEM0		
67	0	GC3000	RAM109_MEM0		
67	1	GC3000	RAM110_MEM0		
67	2	GC3000	RAM111_MEM1		
67	3	GC3000	RAM112_MEM0		
67	4	GC3000	RAM113_MEM1		
67	5	GC3000	RAM114_MEM0		

Table continues on the next page...

MBIST partition	Subpartition	Module or other on-chip system	Memory	Beginning address	Ending address
67	6	GC3000	RAM115_MEM1		
67	7	GC3000	RAM116_MEM0		
67	8	GC3000	RAM117_MEM1		
67	9	GC3000	RAM118_MEM0		
67	10	GC3000	RAM119_MEM0		
68	0	GC3000	RAM120_MEM0		
68	1	GC3000	RAM121_MEM0		
68	2	GC3000	RAM122_MEM1		
68	3	GC3000	RAM123_MEM0		
68	4	GC3000	RAM124_MEM1		
68	5	GC3000	RAM125_MEM0		
68	6	GC3000	RAM126_MEM1		
68	7	GC3000	RAM127_MEM0		
68	8	GC3000	RAM128_MEM1		
68	9	GC3000	RAM129_MEM0		
68	10	GC3000	RAM130_MEM0		
69	0	GC3000	RAM131_MEM0		
69	1	GC3000	RAM132_MEM0		
69	2	GC3000	RAM133_MEM1		
69	3	GC3000	RAM134_MEM0		
69	4	GC3000	RAM135_MEM1		
69	5	GC3000	RAM136_MEM0		
69	6	GC3000	RAM137_MEM1		
69	7	GC3000	RAM138_MEM0		
69	8	GC3000	RAM139_MEM1		
69	9	GC3000	RAM140_MEM0		
69	10	GC3000	RAM141_MEM0		
70	0	GC3000	RAM145_MEM0		
70	1	GC3000	RAM146_MEM0		
70	2	GC3000	RAM147_MEM0		
70	3	GC3000	RAM148_MEM0		
71	0	GC3000	RAM149_MEM0		
71	1	GC3000	RAM150_MEM0		
71	2	GC3000	RAM151_MEM0		
71	3	GC3000	RAM152_MEM0		
71	4	GC3000	RAM153_MEM0		
71	5	GC3000	RAM154_MEM0		
71	6	GC3000	RAM155_MEM0		
71	7	GC3000	RAM156_MEM0		
71	8	GC3000	RAM157_MEM0		

Table continues on the next page...

MBIST partitions

MBIST partition	Subpartition	Module or other on-chip system	Memory	Beginning address	Ending address
71	9	GC3000	RAM158_MEM0		
71	10	GC3000	RAM159_MEM0		
71	11	GC3000	RAM160_MEM0		
71	12	GC3000	RAM162_MEM0		
71	13	GC3000	RAM164_MEM0		
71	14	GC3000	RAM165_MEM0		
71	15	GC3000	RAM166_MEM0		
71	16	GC3000	RAM167_MEM0		
71	17	GC3000	RAM168_MEM0		
71	18	GC3000	RAM169_MEM0		
72	0	GC3000	RAM172_MEM0		
72	1	GC3000	RAM173_MEM0		
72	2	GC3000	RAM174_MEM0		
72	3	GC3000	RAM175_MEM0		
72	4	GC3000	RAM176_MEM0		
72	5	GC3000	RAM177_MEM0		
72	6	GC3000	RAM178_MEM0		
72	7	GC3000	RAM179_MEM0		
72	8	GC3000	RAM180_MEM0		
72	9	GC3000	RAM181_MEM0		
72	10	GC3000	RAM182_MEM0		
72	11	GC3000	RAM183_MEM0		
73	0	GC3000	RAM170_MEM0		
73	1	GC3000	RAM171_MEM0		
74	0	GC3000	RAM188_MEM0		
74	1	GC3000	RAM189_MEM1		
74	2	GC3000	RAM190_MEM0		
74	3	GC3000	RAM191_MEM0		
74	4	GC3000	RAM192_MEM0		
74	5	GC3000	RAM193_MEM0		
74	6	GC3000	RAM194_MEM0		
74	7	GC3000	RAM195_MEM0		
74	8	GC3000	RAM196_MEM0		
74	9	GC3000	RAM197_MEM0		
74	10	GC3000	RAM198_MEM0		
74	11	GC3000	RAM199_MEM0		
74	12	GC3000	RAM200_MEM0		
74	13	GC3000	RAM201_MEM0		
74	14	GC3000	RAM202_MEM0		
74	15	GC3000	RAM203_MEM0		

Table continues on the next page...

MBIST partition	Subpartition	Module or other on-chip system	Memory	Beginning address	Ending address
74	16	GC3000	RAM204_MEM0		
74	17	GC3000	RAM205_MEM0		
74	18	GC3000	RAM206_MEM0		
74	19	GC3000	RAM207_MEM0		
75	0	GC3000	RAM85_MEM0		
75	1	GC3000	RAM95_MEM0		
75	2	GC3000	RAM96_MEM1		
75	3	GC3000	RAM208_MEM0		
76	0	GC3000	RAM60_MEM0		
76	1	GC3000	RAM61_MEM1		
76	2	GC3000	RAM62_MEM0		
76	3	GC3000	RAM63_MEM1		
76	4	GC3000	RAM64_MEM0		
76	5	GC3000	RAM65_MEM1		
76	6	GC3000	RAM66_MEM0		
76	7	GC3000	RAM67_MEM1		
76	8	GC3000	RAM68_MEM0		
76	9	GC3000	RAM69_MEM1		
77	0	GC3000	RAM70_MEM0		
77	1	GC3000	RAM71_MEM1		
77	2	GC3000	RAM72_MEM0		
77	3	GC3000	RAM73_MEM1		
77	4	GC3000	RAM74_MEM0		
77	5	GC3000	RAM75_MEM1		
77	6	GC3000	RAM76_MEM0		
77	7	GC3000	RAM77_MEM1		
77	8	GC3000	RAM78_MEM0		
77	9	GC3000	RAM79_MEM1		

3 STCU2 L/MBIST mapping

The below table lists the LBIST Mapping.

Table 1. LBIST Mapping

BIST ID	BIST Instance Name	DESCRIPTION	MODULES
0	LBIST0	DDR_0	MMDC0 CORE
1	LBIST1	DDR_1	MMDC1 CORE
2	LBIST2	APEX2_0_A	APEX2_0_A

Table continues on the next page...

Table 1. LBIST Mapping (continued)

3	LBIST3	APEX2_0_B	APEX2_0_B
4	LBIST4	APEX2_1_A	APEX2_1_A
5	LBIST5	APEX2_1_B	APEX2_1_B
6	LBIST6	CLUSTER0	CLUSTER0
7	LBIST7	CLUSTER1	CLUSTER1
8	LBIST8	XBAR_SUBSYS	XRDC_SDAC7
			XRDC_PDAC0
			XRDC_MDAC_M17-23
			WKPU
			AXBS
			SWT_1
			SWT_0
			STM_0
			SSE
			SPP_DMA0
			SIUL
			PIT_RTI_0
			LINFLEX_0
			INTM
			I2C_0
			FLEXTIMER_0
			FLEXRAY
			SPI_2
			SPI_0
			DMA_CH_MUX_0
			CRC_0
			CMU3
			CAN_0
			AIPS0
			Cortex-M4
9	LBIST9	CHKR	XRDC_PDAC1
			USDHC
			SWT_4
			SWT_3
			SWT_2
			STM_1
			SPP_DMA2C
			SEMA42_IPS
			RCCU2
			RCCU1

Table continues on the next page...

Table 1. LBIST Mapping (continued)

			QUADSPI_0
			PIT_RTI_1
			OTFAD_QUADSPI
			MSCM
			MEMU
			LINFLEX_1
			I2C_2
			I2C_1
			FOSU
			FLEXTIMER_1
			FCCU
			SPI_3
			SPI_1
			DMA_CH_MUX_1
			CRC_1
			CMU8
			CMU1
			CMU7
			CAN_1
			AIPS1
			ACP_ERM
			ACP_EIM
10	LBIST10	VISION_H264DEC	H264DECODER
			CMU5
11	LBIST11	VISION_H264ENC_MIPI	MIPI_CSI2_0
			MIPI_CSI2_1
			H264ENCODER
			DEC200_ENCODER
			CMU6
12	LBIST12	VISION_IPUV_JPEG_HPSMI	IPUV_0
			IPUV_1
			IPUV_2
			IPUV_3
			HPSMI_LSB
			CMU10
			JPEGDECODER
13	LBIST13	VISION_IPUS_SEQ	IPUS_0
			IPUS_1
			IPUS_2
			IPUS_3

Table continues on the next page...

Table 1. LBIST Mapping (continued)

			IPUS_4
			IPUS_5
			IPUS_6
			IPUS_7
			FASTDMA_0
			CMU9
			VISIONSEQUENCER
14	LBIST14	HPSMI_MSB	HPSMI_MSB
			CMU13
15	LBIST15	NIC301	NIC301
16	LBIST16	ENET_DCU	XRDC_MDAC_M3
			XRDC_MDAC_M14
			XRDC_MDAC_M13
			MTR
			ENET
			DCU
			CMU4
17	LBIST17	SOG_REST	XRDC_SDAC0
			XRDC_SDAC4
			XRDC_SDAC5
			XRDC_SDAC6
			XRDC_MDAC_M0
			XRDC_MDAC_M1
			XRDC_MDAC_M10
			XRDC_MDAC_M11
			XRDC_MDAC_M12
			XRDC_MDAC_M2
			XRDC_MDAC_M4
			XRDC_MDAC_M5
			XRDC_MDAC_M6
			XRDC_MDAC_M7
			XRDC_MDAC_M8
			XRDC_MDAC_M9
			VIU_0
			VIU_1
			TSENS
			SJC
			SIPI
			RCCU_FASTDMA
			PCIE

Table continues on the next page...

Table 1. LBIST Mapping (continued)

			OCOTP_CTRL_WRAPPER
			MMDC_ECC_WTPS_0
			MMDC_ECC_WTPS_1
			MC_ME
			IOMUX
			IOMUXC
			FASTDMA_1
			DIGRF_TOP
			CMU12
			CMU11
			CMU2
			CMU0
			ADC_BIST_TOP
			ADC_0
			ACP_XRDC
18	LBIST18	B2D_PM	GPU B2D_PM
19	LBIST19	B3D_REST	GPU B3D_REST
20	LBIST20	B3D_SH	GPU B3D_SH
21	LBIST21	CCI_GIC	XRDC_MDAC_M15
			XRDC_MDAC_M16
			CCI400
			GIC400
22	LBIST22	SDAC_XRDC	XRDC_SDAC1
			XRDC_SDAC2
			XRDC_SDAC3
23	LBIST23	Cortex-A53_0_CORE0	Cortex-A53_0_CORE0
24	LBIST24	Cortex-A53_0_CORE1	Cortex-A53_0_CORE1
25	LBIST25	Cortex-A53_1_CORE0	Cortex-A53_1_CORE0
26	LBIST26	Cortex-A53_1_CORE1	Cortex-A53_1_CORE1

The below table lists the MBIST mapping of the device.

Table 2. MBIST Mapping

BIST ID (NMCUT BIST)	BIST Name	BIST Position Corresponding to the NMCUT for the BIST in STCU2_MBSSW	Comments	Description
0	BIST-00	0	L1 data data RAM	Cortex-A53-0 CORE
0	BIST-00	0	L1 data data RAM	Cortex-A53-0 CORE
0	BIST-00	1	L1 data data RAM	Cortex-A53-0 CORE
0	BIST-00	1	L1 data data RAM	Cortex-A53-0 CORE

Table continues on the next page...

Table 2. MBIST Mapping (continued)

0	BIST-00	2	L1 data data RAM	Cortex-A53-0 CORE
0	BIST-00	2	L1 data data RAM	Cortex-A53-0 CORE
0	BIST-00	3	L1 data data RAM	Cortex-A53-0 CORE
0	BIST-00	3	L1 data data RAM	Cortex-A53-0 CORE
0	BIST-00	4	L1 data data RAM	Cortex-A53-0 CORE
0	BIST-00	4	L1 data data RAM	Cortex-A53-0 CORE
0	BIST-00	5	L1 data data RAM	Cortex-A53-0 CORE
0	BIST-00	5	L1 data data RAM	Cortex-A53-0 CORE
0	BIST-00	6	L1 data data RAM	Cortex-A53-0 CORE
0	BIST-00	6	L1 data data RAM	Cortex-A53-0 CORE
0	BIST-00	7	L1 data data RAM	Cortex-A53-0 CORE
0	BIST-00	7	L1 data data RAM	Cortex-A53-0 CORE
0	BIST-00	8	L1 data tag RAM	Cortex-A53-0 CORE
0	BIST-00	9	L1 data tag RAM	Cortex-A53-0 CORE
0	BIST-00	10	L1 data tag RAM	Cortex-A53-0 CORE
0	BIST-00	11	L1 data tag RAM	Cortex-A53-0 CORE
0	BIST-00	12	L1 data dirty RAM	Cortex-A53-0 CORE
0	BIST-00	12	L1 data dirty RAM	Cortex-A53-0 CORE
0	BIST-00	13	L1 instruction data RAM	Cortex-A53-0 CORE
0	BIST-00	13	L1 instruction data RAM	Cortex-A53-0 CORE
0	BIST-00	14	L1 instruction data RAM	Cortex-A53-0 CORE
0	BIST-00	14	L1 instruction data RAM	Cortex-A53-0 CORE
0	BIST-00	15	BTAC Stage 0 RAM	Cortex-A53-0 CORE
0	BIST-00	16	BTAC Stage 1 RAM	Cortex-A53-0 CORE
0	BIST-00	17	L1 instruction tag RAM	Cortex-A53-0 CORE
0	BIST-00	18	L1 instruction tag RAM	Cortex-A53-0 CORE
0	BIST-00	19	TLB RAM	Cortex-A53-0 CORE
0	BIST-00	20	TLB RAM	Cortex-A53-0 CORE
0	BIST-00	21	TLB RAM	Cortex-A53-0 CORE
0	BIST-00	22	TLB RAM	Cortex-A53-0 CORE
0	BIST-00	23	SCU duplicate tag RAM	Cortex-A53-0 CORE
0	BIST-00	23	SCU duplicate tag RAM	Cortex-A53-0 CORE
0	BIST-00	24	SCU duplicate tag RAM	Cortex-A53-0 CORE
0	BIST-00	24	SCU duplicate tag RAM	Cortex-A53-0 CORE
0	BIST-00	25	SCU duplicate tag RAM	Cortex-A53-0 CORE
0	BIST-00	25	SCU duplicate tag RAM	Cortex-A53-0 CORE
0	BIST-00	26	SCU duplicate tag RAM	Cortex-A53-0 CORE
0	BIST-00	26	SCU duplicate tag RAM	Cortex-A53-0 CORE
0	BIST-00	27	L2 tag RAM	Cortex-A53-0 CORE
0	BIST-00	28	L2 tag RAM	Cortex-A53-0 CORE

Table continues on the next page...

Table 2. MBIST Mapping (continued)

0	BIST-00	29	L2 tag RAM	Cortex-A53-0 CORE
0	BIST-00	30	L2 tag RAM	Cortex-A53-0 CORE
0	BIST-00	31	L2 tag RAM	Cortex-A53-0 CORE
0	BIST-00	32	L2 tag RAM	Cortex-A53-0 CORE
0	BIST-00	33	L2 tag RAM	Cortex-A53-0 CORE
0	BIST-00	34	L2 tag RAM	Cortex-A53-0 CORE
0	BIST-00	35	L2 tag RAM	Cortex-A53-0 CORE
0	BIST-00	36	L2 tag RAM	Cortex-A53-0 CORE
0	BIST-00	37	L2 tag RAM	Cortex-A53-0 CORE
0	BIST-00	38	L2 tag RAM	Cortex-A53-0 CORE
0	BIST-00	39	L2 tag RAM	Cortex-A53-0 CORE
0	BIST-00	40	L2 tag RAM	Cortex-A53-0 CORE
0	BIST-00	41	L2 tag RAM	Cortex-A53-0 CORE
0	BIST-00	42	L2 tag RAM	Cortex-A53-0 CORE
0	BIST-00	43	L2 victim RAM	Cortex-A53-0 CORE
0	BIST-00	44	L1 data data RAM	Cortex-A53-0 CORE
0	BIST-00	44	L1 data data RAM	Cortex-A53-0 CORE
0	BIST-00	45	L1 data data RAM	Cortex-A53-0 CORE
0	BIST-00	45	L1 data data RAM	Cortex-A53-0 CORE
0	BIST-00	46	L1 data data RAM	Cortex-A53-0 CORE
0	BIST-00	46	L1 data data RAM	Cortex-A53-0 CORE
0	BIST-00	47	L1 data data RAM	Cortex-A53-0 CORE
0	BIST-00	47	L1 data data RAM	Cortex-A53-0 CORE
0	BIST-00	48	L1 data data RAM	Cortex-A53-0 CORE
0	BIST-00	48	L1 data data RAM	Cortex-A53-0 CORE
0	BIST-00	49	L1 data data RAM	Cortex-A53-0 CORE
0	BIST-00	49	L1 data data RAM	Cortex-A53-0 CORE
0	BIST-00	50	L1 data data RAM	Cortex-A53-0 CORE
0	BIST-00	50	L1 data data RAM	Cortex-A53-0 CORE
0	BIST-00	51	L1 data data RAM	Cortex-A53-0 CORE
0	BIST-00	51	L1 data data RAM	Cortex-A53-0 CORE
0	BIST-00	52	L1 data tag RAM	Cortex-A53-0 CORE
0	BIST-00	53	L1 data tag RAM	Cortex-A53-0 CORE
0	BIST-00	54	L1 data tag RAM	Cortex-A53-0 CORE
0	BIST-00	55	L1 data tag RAM	Cortex-A53-0 CORE
0	BIST-00	56	L1 data dirty RAM	Cortex-A53-0 CORE
0	BIST-00	56	L1 data dirty RAM	Cortex-A53-0 CORE
0	BIST-00	57	L1 instruction data RAM	Cortex-A53-0 CORE
0	BIST-00	57	L1 instruction data RAM	Cortex-A53-0 CORE
0	BIST-00	58	L1 instruction data RAM	Cortex-A53-0 CORE

Table continues on the next page...

Table 2. MBIST Mapping (continued)

0	BIST-00	58	L1 instruction data RAM	Cortex-A53-0 CORE
0	BIST-00	59	BTAC Stage 0 RAM	Cortex-A53-0 CORE
0	BIST-00	60	BTAC Stage 1 RAM	Cortex-A53-0 CORE
0	BIST-00	61	L1 instruction tag RAM	Cortex-A53-0 CORE
0	BIST-00	62	L1 instruction tag RAM	Cortex-A53-0 CORE
0	BIST-00	63	TLB RAM	Cortex-A53-0 CORE
0	BIST-00	64	TLB RAM	Cortex-A53-0 CORE
0	BIST-00	65	TLB RAM	Cortex-A53-0 CORE
0	BIST-00	66	TLB RAM	Cortex-A53-0 CORE
0	BIST-00	67	SCU duplicate tag RAM	Cortex-A53-0 CORE
0	BIST-00	67	SCU duplicate tag RAM	Cortex-A53-0 CORE
0	BIST-00	68	SCU duplicate tag RAM	Cortex-A53-0 CORE
0	BIST-00	68	SCU duplicate tag RAM	Cortex-A53-0 CORE
0	BIST-00	69	SCU duplicate tag RAM	Cortex-A53-0 CORE
0	BIST-00	69	SCU duplicate tag RAM	Cortex-A53-0 CORE
0	BIST-00	70	SCU duplicate tag RAM	Cortex-A53-0 CORE
0	BIST-00	70	SCU duplicate tag RAM	Cortex-A53-0 CORE
1	BIST-01	0	L1 data data RAM	Cortex-A53-1 CORE
1	BIST-01	0	L1 data data RAM	Cortex-A53-1 CORE
1	BIST-01	1	L1 data data RAM	Cortex-A53-1 CORE
1	BIST-01	1	L1 data data RAM	Cortex-A53-1 CORE
1	BIST-01	2	L1 data data RAM	Cortex-A53-1 CORE
1	BIST-01	2	L1 data data RAM	Cortex-A53-1 CORE
1	BIST-01	3	L1 data data RAM	Cortex-A53-1 CORE
1	BIST-01	3	L1 data data RAM	Cortex-A53-1 CORE
1	BIST-01	4	L1 data data RAM	Cortex-A53-1 CORE
1	BIST-01	4	L1 data data RAM	Cortex-A53-1 CORE
1	BIST-01	5	L1 data data RAM	Cortex-A53-1 CORE
1	BIST-01	5	L1 data data RAM	Cortex-A53-1 CORE
1	BIST-01	6	L1 data data RAM	Cortex-A53-1 CORE
1	BIST-01	6	L1 data data RAM	Cortex-A53-1 CORE
1	BIST-01	7	L1 data data RAM	Cortex-A53-1 CORE
1	BIST-01	7	L1 data data RAM	Cortex-A53-1 CORE
1	BIST-01	8	L1 data tag RAM	Cortex-A53-1 CORE
1	BIST-01	9	L1 data tag RAM	Cortex-A53-1 CORE
1	BIST-01	10	L1 data tag RAM	Cortex-A53-1 CORE
1	BIST-01	11	L1 data tag RAM	Cortex-A53-1 CORE
1	BIST-01	12	L1 data dirty RAM	Cortex-A53-1 CORE
1	BIST-01	12	L1 data dirty RAM	Cortex-A53-1 CORE
1	BIST-01	13	L1 instruction data RAM	Cortex-A53-1 CORE

Table continues on the next page...

Table 2. MBIST Mapping (continued)

1	BIST-01	13	L1 instruction data RAM	Cortex-A53-1 CORE
1	BIST-01	14	L1 instruction data RAM	Cortex-A53-1 CORE
1	BIST-01	14	L1 instruction data RAM	Cortex-A53-1 CORE
1	BIST-01	15	BTAC Stage 0 RAM	Cortex-A53-1 CORE
1	BIST-01	16	BTAC Stage 1 RAM	Cortex-A53-1 CORE
1	BIST-01	17	L1 instruction tag RAM	Cortex-A53-1 CORE
1	BIST-01	18	L1 instruction tag RAM	Cortex-A53-1 CORE
1	BIST-01	19	TLB RAM	Cortex-A53-1 CORE
1	BIST-01	20	TLB RAM	Cortex-A53-1 CORE
1	BIST-01	21	TLB RAM	Cortex-A53-1 CORE
1	BIST-01	22	TLB RAM	Cortex-A53-1 CORE
1	BIST-01	23	SCU duplicate tag RAM	Cortex-A53-1 CORE
1	BIST-01	23	SCU duplicate tag RAM	Cortex-A53-1 CORE
1	BIST-01	24	SCU duplicate tag RAM	Cortex-A53-1 CORE
1	BIST-01	24	SCU duplicate tag RAM	Cortex-A53-1 CORE
1	BIST-01	25	SCU duplicate tag RAM	Cortex-A53-1 CORE
1	BIST-01	25	SCU duplicate tag RAM	Cortex-A53-1 CORE
1	BIST-01	26	SCU duplicate tag RAM	Cortex-A53-1 CORE
1	BIST-01	26	SCU duplicate tag RAM	Cortex-A53-1 CORE
1	BIST-01	27	L2 tag RAM	Cortex-A53-1 CORE
1	BIST-01	28	L2 tag RAM	Cortex-A53-1 CORE
1	BIST-01	29	L2 tag RAM	Cortex-A53-1 CORE
1	BIST-01	30	L2 tag RAM	Cortex-A53-1 CORE
1	BIST-01	31	L2 tag RAM	Cortex-A53-1 CORE
1	BIST-01	32	L2 tag RAM	Cortex-A53-1 CORE
1	BIST-01	33	L2 tag RAM	Cortex-A53-1 CORE
1	BIST-01	34	L2 tag RAM	Cortex-A53-1 CORE
1	BIST-01	35	L2 tag RAM	Cortex-A53-1 CORE
1	BIST-01	36	L2 tag RAM	Cortex-A53-1 CORE
1	BIST-01	37	L2 tag RAM	Cortex-A53-1 CORE
1	BIST-01	38	L2 tag RAM	Cortex-A53-1 CORE
1	BIST-01	39	L2 tag RAM	Cortex-A53-1 CORE
1	BIST-01	40	L2 tag RAM	Cortex-A53-1 CORE
1	BIST-01	41	L2 tag RAM	Cortex-A53-1 CORE
1	BIST-01	42	L2 tag RAM	Cortex-A53-1 CORE
1	BIST-01	43	L2 victim RAM	Cortex-A53-1 CORE
1	BIST-01	44	L1 data data RAM	Cortex-A53-1 CORE
1	BIST-01	44	L1 data data RAM	Cortex-A53-1 CORE
1	BIST-01	45	L1 data data RAM	Cortex-A53-1 CORE
1	BIST-01	45	L1 data data RAM	Cortex-A53-1 CORE

Table continues on the next page...

Table 2. MBIST Mapping (continued)

1	BIST-01	46	L1 data data RAM	Cortex-A53-1 CORE
1	BIST-01	46	L1 data data RAM	Cortex-A53-1 CORE
1	BIST-01	47	L1 data data RAM	Cortex-A53-1 CORE
1	BIST-01	47	L1 data data RAM	Cortex-A53-1 CORE
1	BIST-01	48	L1 data data RAM	Cortex-A53-1 CORE
1	BIST-01	48	L1 data data RAM	Cortex-A53-1 CORE
1	BIST-01	49	L1 data data RAM	Cortex-A53-1 CORE
1	BIST-01	49	L1 data data RAM	Cortex-A53-1 CORE
1	BIST-01	50	L1 data data RAM	Cortex-A53-1 CORE
1	BIST-01	50	L1 data data RAM	Cortex-A53-1 CORE
1	BIST-01	51	L1 data data RAM	Cortex-A53-1 CORE
1	BIST-01	51	L1 data data RAM	Cortex-A53-1 CORE
1	BIST-01	52	L1 data tag RAM	Cortex-A53-1 CORE
1	BIST-01	53	L1 data tag RAM	Cortex-A53-1 CORE
1	BIST-01	54	L1 data tag RAM	Cortex-A53-1 CORE
1	BIST-01	55	L1 data tag RAM	Cortex-A53-1 CORE
1	BIST-01	56	L1 data dirty RAM	Cortex-A53-1 CORE
1	BIST-01	56	L1 data dirty RAM	Cortex-A53-1 CORE
1	BIST-01	57	L1 instruction data RAM	Cortex-A53-1 CORE
1	BIST-01	57	L1 instruction data RAM	Cortex-A53-1 CORE
1	BIST-01	58	L1 instruction data RAM	Cortex-A53-1 CORE
1	BIST-01	58	L1 instruction data RAM	Cortex-A53-1 CORE
1	BIST-01	59	BTAC Stage 0 RAM	Cortex-A53-1 CORE
1	BIST-01	60	BTAC Stage 1 RAM	Cortex-A53-1 CORE
1	BIST-01	61	L1 instruction tag RAM	Cortex-A53-1 CORE
1	BIST-01	62	L1 instruction tag RAM	Cortex-A53-1 CORE
1	BIST-01	63	TLB RAM	Cortex-A53-1 CORE
1	BIST-01	64	TLB RAM	Cortex-A53-1 CORE
1	BIST-01	65	TLB RAM	Cortex-A53-1 CORE
1	BIST-01	66	TLB RAM	Cortex-A53-1 CORE
1	BIST-01	67	SCU duplicate tag RAM	Cortex-A53-1 CORE
1	BIST-01	67	SCU duplicate tag RAM	Cortex-A53-1 CORE
1	BIST-01	68	SCU duplicate tag RAM	Cortex-A53-1 CORE
1	BIST-01	68	SCU duplicate tag RAM	Cortex-A53-1 CORE
1	BIST-01	69	SCU duplicate tag RAM	Cortex-A53-1 CORE
1	BIST-01	69	SCU duplicate tag RAM	Cortex-A53-1 CORE
1	BIST-01	70	SCU duplicate tag RAM	Cortex-A53-1 CORE
1	BIST-01	70	SCU duplicate tag RAM	Cortex-A53-1 CORE
2	BIST-02	0	L2 DATA RAM	Cortex-A53-0
2	BIST-02	0	L2 DATA RAM	Cortex-A53-0

Table continues on the next page...

Table 2. MBIST Mapping (continued)

2	BIST-02	0	L2 DATA RAM	Cortex-A53-0
2	BIST-02	0	L2 DATA RAM	Cortex-A53-0
2	BIST-02	1	L2 DATA RAM	Cortex-A53-0
2	BIST-02	1	L2 DATA RAM	Cortex-A53-0
2	BIST-02	1	L2 DATA RAM	Cortex-A53-0
2	BIST-02	1	L2 DATA RAM	Cortex-A53-0
2	BIST-02	2	L2 DATA RAM	Cortex-A53-0
2	BIST-02	2	L2 DATA RAM	Cortex-A53-0
2	BIST-02	2	L2 DATA RAM	Cortex-A53-0
2	BIST-02	2	L2 DATA RAM	Cortex-A53-0
2	BIST-02	3	L2 DATA RAM	Cortex-A53-0
2	BIST-02	3	L2 DATA RAM	Cortex-A53-0
2	BIST-02	3	L2 DATA RAM	Cortex-A53-0
2	BIST-02	3	L2 DATA RAM	Cortex-A53-0
3	BIST-03	0	L2 DATA RAM	Cortex-A53-1
3	BIST-03	0	L2 DATA RAM	Cortex-A53-1
3	BIST-03	0	L2 DATA RAM	Cortex-A53-1
3	BIST-03	0	L2 DATA RAM	Cortex-A53-1
3	BIST-03	1	L2 DATA RAM	Cortex-A53-1
3	BIST-03	1	L2 DATA RAM	Cortex-A53-1
3	BIST-03	1	L2 DATA RAM	Cortex-A53-1
3	BIST-03	1	L2 DATA RAM	Cortex-A53-1
3	BIST-03	2	L2 DATA RAM	Cortex-A53-1
3	BIST-03	2	L2 DATA RAM	Cortex-A53-1
3	BIST-03	2	L2 DATA RAM	Cortex-A53-1
3	BIST-03	2	L2 DATA RAM	Cortex-A53-1
3	BIST-03	3	L2 DATA RAM	Cortex-A53-1
3	BIST-03	3	L2 DATA RAM	Cortex-A53-1
3	BIST-03	3	L2 DATA RAM	Cortex-A53-1
3	BIST-03	3	L2 DATA RAM	Cortex-A53-1
4	BIST-04	0	FIFO MEM	VIU-0
5	BIST-05	0	FIFO MEM	VIU-1
6	BIST-06	0	BAR_ROM_MEM	BOOT ROM
7	BIST-07	0	Reserved	Reserved
7	BIST-07	1	GAMMA R MEM	2D-ACE
7	BIST-07	2	GAMMA B MEM	2D-ACE
7	BIST-07	3	GAMMA G MEM	2D-ACE
7	BIST-07	4	INPUT BUFFER MEM0	2D-ACE
7	BIST-07	5	INPUT BUFFER MEM1	2D-ACE
7	BIST-07	6	INPUT BUFFER MEM2	2D-ACE

Table continues on the next page...

Table 2. MBIST Mapping (continued)

7	BIST-07	7	INPUT BUFFER MEM3	2D-ACE
7	BIST-07	8	LAYER MEM	2D-ACE
7	BIST-07	9	PALETTE MEM	2D-ACE
7	BIST-07	10	TILE MEM0	2D-ACE
7	BIST-07	11	TILE MEM1	2D-ACE
8	BIST-08	0	PCIE MASTER COMPOSITION MEM	PCIE
8	BIST-08	1	PCIE RECEIVE QUEUE DATA MEM	PCIE
8	BIST-08	2	PCIE RECEIVE QUEUE HEADER MEM0	PCIE
8	BIST-08	3	PCIE RECEIVE QUEUE HEADER MEM1	PCIE
8	BIST-08	4	PCIE TRANSMIT RETRY BUFFER MEM	PCIE
8	BIST-08	5	PCIE READ BUFFER MEM	PCIE
9	BIST-09	0	Flexray DRAM MEM0	FLEXRAY-133
9	BIST-09	1	Flexray DRAM MEM1	FLEXRAY-133
10	BIST-10	0	Cortex-A53_ETF_MEM0	Cortex-A53-0 ETF
11	BIST-11	0	Cortex-A53_ETF_MEM1	Cortex-A53-1 ETF
12	BIST-12	0	MEM0	CAN-0
12	BIST-12	1	MEM1	CAN-0
13	BIST-13	0	MEM0	CAN-1
13	BIST-13	1	MEM1	CAN-1
14	BIST-14	0	Cortex-M4_DCACHE_DRAM_MEM_0	Cortex-M4
14	BIST-14	1	Cortex-M4_DCACHE_DRAM_MEM_1	Cortex-M4
14	BIST-14	2	Cortex-M4_DCACHE_TRAM_MEM_0	Cortex-M4
14	BIST-14	3	Cortex-M4_DCACHE_TRAM_MEM_1	Cortex-M4
14	BIST-14	4	Cortex-M4_ETF_RAM_MEM	Cortex-M4
14	BIST-14	5	Cortex-M4_ICACHE_DRAM_MEM_0	Cortex-M4

Table continues on the next page...

Table 2. MBIST Mapping (continued)

14	BIST-14	6	Cortex-M4_ICACHE_DRAM_MEM_1	Cortex-M4
14	BIST-14	7	Cortex-M4_ICACHE_TRAM_MEM_0	Cortex-M4
14	BIST-14	8	Cortex-M4_ICACHE_TRAM_MEM_1	Cortex-M4
14	BIST-14	9	Cortex-M4_TCM_UPPER_MEM_0	Cortex-M4
14	BIST-14	10	Cortex-M4_TCM_LOWER_MEM_0	Cortex-M4
15	BIST-15	0	RESERVED	RESERVED
16	BIST-16	0	ENET RX MEM	ENET
16	BIST-16	1	ENET RXP L MEM	ENET
16	BIST-16	2	ENET RXP U MEM	ENET
16	BIST-16	3	ENET TX MEM	ENET
17	BIST-17	0	Fastdma 0 Transmit Buffer MEM0	FASTDMA
17	BIST-17	1	Fastdma 0 Transmit Buffer MEM1	FASTDMA
18	BIST-18	0	Flexray DRAM MEM	FLEXRAY-80
19	BIST-19	0	IPUS0 HIST MEM	IPSU
19	BIST-19	1	IPUS1 HIST MEM	IPSU
19	BIST-19	2	IPUS2 HIST MEM	IPSU
19	BIST-19	3	IPUS2 LUT MEM	IPSU
19	BIST-19	4	IPUS3 HIST MEM	IPSU
19	BIST-19	5	IPUS3 LUT MEM	IPSU
19	BIST-19	6	IPUS7 STAT MEM	IPSU
20	BIST-20	0	QUANTIZATION TABLE1 MEM	MJPEG
20	BIST-20	1	QUANTIZATION TABLE2 MEM	MJPEG
20	BIST-20	2	QUANTIZATION TABLE3 MEM	MJPEG
20	BIST-20	3	QUANTIZATION TABLE4 MEM	MJPEG
20	BIST-20	4	HUFFMAN DECODER FIFO OUTPUT MEM	MJPEG
20	BIST-20	5	HUFFMAN TABLE MEM	MJPEG
21	BIST-21	0	MMDC ETF MEM	MMDC

Table continues on the next page...

Table 2. MBIST Mapping (continued)

22	BIST-22	0	QUADSPI BUFFER MEM	QUAD
23	BIST-23	0	PRAM	SEQUENCER
23	BIST-23	1	CRAM	SEQUENCER
24	BIST-24	0	SEG1_MEM0	SRAM-1M (0-3)
24	BIST-24	1	SEG1_MEM1	SRAM-1M (0-3)
24	BIST-24	2	SEG1_MEM2	SRAM-1M (0-3)
24	BIST-24	3	SEG1_MEM3	SRAM-1M (0-3)
25	BIST-25	0	SEG1_MEM4	SRAM-1M (4-7)
25	BIST-25	1	SEG1_MEM5	SRAM-1M (4-7)
25	BIST-25	2	SEG1_MEM6	SRAM-1M (4-7)
25	BIST-25	3	SEG1_MEM7	SRAM-1M (4-7)
26	BIST-26	0	SEG2_MEM0	SRAM-1M (8-11)
26	BIST-26	1	SEG2_MEM1	SRAM-1M (8-11)
26	BIST-26	2	SEG2_MEM2	SRAM-1M (8-11)
26	BIST-26	3	SEG2_MEM3	SRAM-1M (8-11)
27	BIST-27	0	SEG2_MEM4	SRAM-1M (12-15)
27	BIST-27	1	SEG2_MEM5	SRAM-1M (12-15)
27	BIST-27	2	SEG2_MEM6	SRAM-1M (12-15)
27	BIST-27	3	SEG2_MEM7	SRAM-1M (12-15)
28	BIST-28	0	SEG0_MEM0	SRAM-3M (0-3)
28	BIST-28	1	SEG0_MEM1	SRAM-3M (0-3)
28	BIST-28	2	SEG0_MEM2	SRAM-3M (0-3)
28	BIST-28	3	SEG0_MEM3	SRAM-3M (0-3)
29	BIST-29	0	SEG0_MEM4	SRAM-3M (4-7)
29	BIST-29	1	SEG0_MEM5	SRAM-3M (4-7)
29	BIST-29	2	SEG0_MEM6	SRAM-3M (4-7)
29	BIST-29	3	SEG0_MEM7	SRAM-3M (4-7)
30	BIST-30	0	SEG0_MEM8	SRAM-3M (8-11)
30	BIST-30	1	SEG0_MEM9	SRAM-3M (8-11)
30	BIST-30	2	SEG0_MEM10	SRAM-3M (8-11)
30	BIST-30	3	SEG0_MEM11	SRAM-3M (8-11)
31	BIST-31	0	SEG0_MEM12	SRAM-3M (12-15)
31	BIST-31	1	SEG0_MEM13	SRAM-3M (12-15)
31	BIST-31	2	SEG0_MEM14	SRAM-3M (12-15)
31	BIST-31	3	SEG0_MEM15	SRAM-3M (12-15)
32	BIST-32	0	SEG0_MEM16	SRAM-3M (16-19)
32	BIST-32	1	SEG0_MEM17	SRAM-3M (16-19)
32	BIST-32	2	SEG0_MEM18	SRAM-3M (16-19)
32	BIST-32	3	SEG0_MEM19	SRAM-3M (16-19)
33	BIST-33	0	SEG0_MEM20	SRAM-3M (20-23)

Table continues on the next page...

Table 2. MBIST Mapping (continued)

33	BIST-33	1	SEG0_MEM21	SRAM-3M (20-23)
33	BIST-33	2	SEG0_MEM22	SRAM-3M (20-23)
33	BIST-33	3	SEG0_MEM23	SRAM-3M (20-23)
34	BIST-34	0	CMEM0	APEX-0
34	BIST-34	1	CMEM1	APEX-0
34	BIST-34	2	CMEM2	APEX-0
34	BIST-34	3	CMEM3	APEX-0
34	BIST-34	4	CMEM4	APEX-0
34	BIST-34	5	CMEM5	APEX-0
34	BIST-34	6	CMEM6	APEX-0
34	BIST-34	7	CMEM7	APEX-0
34	BIST-34	8	CMEM8	APEX-0
34	BIST-34	9	CMEM9	APEX-0
34	BIST-34	10	CMEM10	APEX-0
34	BIST-34	11	CMEM11	APEX-0
34	BIST-34	12	CMEM12	APEX-0
34	BIST-34	13	CMEM13	APEX-0
34	BIST-34	14	CMEM14	APEX-0
34	BIST-34	15	CMEM15	APEX-0
34	BIST-34	16	DMEM0	APEX-0
34	BIST-34	17	DMEM1	APEX-0
34	BIST-34	18	IMEM0	APEX-0
34	BIST-34	19	IMEM1	APEX-0
35	BIST-35	0	CMEM0	APEX-1
35	BIST-35	1	CMEM1	APEX-1
35	BIST-35	2	CMEM2	APEX-1
35	BIST-35	3	CMEM3	APEX-1
35	BIST-35	4	CMEM4	APEX-1
35	BIST-35	5	CMEM5	APEX-1
35	BIST-35	6	CMEM6	APEX-1
35	BIST-35	7	CMEM7	APEX-1
35	BIST-35	8	CMEM8	APEX-1
35	BIST-35	9	CMEM9	APEX-1
35	BIST-35	10	CMEM10	APEX-1
35	BIST-35	11	CMEM11	APEX-1
35	BIST-35	12	CMEM12	APEX-1
35	BIST-35	13	CMEM13	APEX-1
35	BIST-35	14	CMEM14	APEX-1
35	BIST-35	15	CMEM15	APEX-1
35	BIST-35	16	DMEM0	APEX-1

Table continues on the next page...

Table 2. MBIST Mapping (continued)

35	BIST-35	17	DMEM1	APEX-1
35	BIST-35	18	IMEM0	APEX-1
35	BIST-35	19	IMEM1	APEX-1
36	BIST-36	0	CORE1 INTRA-PREDICTION MEM	H264 ENCODER
36	BIST-36	1	CORE1 INTRA-PREDICTION MEM	H264 ENCODER
36	BIST-36	2	CORE1 INTRA-PREDICTION MEM	H264 ENCODER
36	BIST-36	3	CORE1 INTRA-PREDICTION MEM	H264 ENCODER
36	BIST-36	4	CORE1 INTRA-PREDICTION MEM	H264 ENCODER
36	BIST-36	5	CORE1 INTRA-PREDICTION MEM	H264 ENCODER
36	BIST-36	6	CORE1 INTRA-PREDICTION MEM	H264 ENCODER
36	BIST-36	7	CORE1 INTRA-PREDICTION MEM	H264 ENCODER
36	BIST-36	8	CORE1 INTRA-PREDICTION MEM	H264 ENCODER
36	BIST-36	9	CORE1 INTRA-PREDICTION MEM	H264 ENCODER
36	BIST-36	10	CORE1 INTRA-PREDICTION MEM	H264 ENCODER
37	BIST-37	0	ENC_MEM0	DEC 200 Encoder
37	BIST-37	1	ENC_MEM1_0	DEC 200 Encoder
37	BIST-37	2	ENC_MEM1_1	DEC 200 Encoder
38	RESERVED	-	RESERVED	RESERVED
39	BIST-39	0	Fastdma 0 Queue MEM0	FASTDMA - QUE
39	BIST-39	1	Fastdma 0 Queue MEM1	FASTDMA - QUE
40	BIST-40	0	KRAM	VSEQ
41	BIST-41	0	DMA_RAM	EDMA
42	BIST-42	0	RECONSTRUCTION DOUBLE BUFFER CHANNEL3 MEMA_0	H264 DECODER
42	BIST-42	1	RECONSTRUCTION DOUBLE BUFFER CHANNEL3 MEMA_1	H264 DECODER
42	BIST-42	2	RECONSTRUCTION DOUBLE BUFFER CHANNEL0 MEMA_0	H264 DECODER
42	BIST-42	3	RECONSTRUCTION DOUBLE BUFFER CHANNEL0 MEMA_1	H264 DECODER

Table continues on the next page...

Table 2. MBIST Mapping (continued)

42	BIST-42	4	RECONSTRUCTION DOUBLE BUFFER CHANNEL0 MEMB_0	H264 DECODER
42	BIST-42	5	RECONSTRUCTION DOUBLE BUFFER CHANNEL0 MEMB_1	H264 DECODER
42	BIST-42	6	RECONSTRUCTION DOUBLE BUFFER CHANNEL1 MEMA_0	H264 DECODER
42	BIST-42	7	RECONSTRUCTION DOUBLE BUFFER CHANNEL1 MEMA_1	H264 DECODER
42	BIST-42	8	RECONSTRUCTION DOUBLE BUFFER CHANNEL1 MEMB_0	H264 DECODER
42	BIST-42	9	RECONSTRUCTION DOUBLE BUFFER CHANNEL1 MEMB_1	H264 DECODER
42	BIST-42	10	RECONSTRUCTION DOUBLE BUFFER CHANNEL2 MEMA_0	H264 DECODER
42	BIST-42	11	RECONSTRUCTION DOUBLE BUFFER CHANNEL2 MEMA_1	H264 DECODER
42	BIST-42	12	RECONSTRUCTION DOUBLE BUFFER CHANNEL2 MEMB_0	H264 DECODER
42	BIST-42	13	RECONSTRUCTION DOUBLE BUFFER CHANNEL2 MEMB_1	H264 DECODER
42	BIST-42	14	RECONSTRUCTION DOUBLE BUFFER CHANNEL3 MEMB_0	H264 DECODER
42	BIST-42	15	RECONSTRUCTION DOUBLE BUFFER CHANNEL3 MEMB_1	H264 DECODER
43	BIST-43	0	CORE0 VLC MEM	H264 ENCODER
43	BIST-43	1	CORE0 VLC MEM	H264 ENCODER
43	BIST-43	2	CORE1 VLC MEM	H264 ENCODER
43	BIST-43	3	CORE1 VLC MEM	H264 ENCODER
43	BIST-43	4	CORE0 VLC MEM	H264 ENCODER
43	BIST-43	5	CORE0 VLC MEM	H264 ENCODER
43	BIST-43	6	CORE0 VLC MEM	H264 ENCODER
43	BIST-43	7	CORE0 VLC MEM	H264 ENCODER
43	BIST-43	8	CORE1 VLC MEM	H264 ENCODER
44	BIST-44	0	CORE0 INTRA-PREDICTION MEM	H264 ENCODER

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Table 2. MBIST Mapping (continued)

44	BIST-44	1	CORE0 INTRA-PREDICTION MEM	H264 ENCODER
44	BIST-44	2	CORE0 INTRA-PREDICTION MEM	H264 ENCODER
44	BIST-44	3	CORE0 INTRA-PREDICTION MEM	H264 ENCODER
44	BIST-44	4	CORE0 INTRA-PREDICTION MEM	H264 ENCODER
44	BIST-44	5	CORE0 INTRA-PREDICTION MEM	H264 ENCODER
44	BIST-44	6	CORE0 INTRA-PREDICTION MEM	H264 ENCODER
44	BIST-44	7	CORE0 INTRA-PREDICTION MEM	H264 ENCODER
44	BIST-44	8	CORE0 INTRA-PREDICTION MEM	H264 ENCODER
44	BIST-44	9	CORE0 INTRA-PREDICTION MEM	H264 ENCODER
44	BIST-44	10	CORE0 INTRA-PREDICTION MEM	H264 ENCODER
45	BIST-45	0	CORE0 VLC MEM	H264 ENCODER
45	BIST-45	1	CORE0 VLC MEM	H264 ENCODER
45	BIST-45	2	CORE0 VLC MEM	H264 ENCODER
45	BIST-45	3	CORE0 VLC MEM	H264 ENCODER
45	BIST-45	4	CORE1 VLC MEM	H264 ENCODER
45	BIST-45	5	CORE1 VLC MEM	H264 ENCODER
45	BIST-45	6	CORE1 VLC MEM	H264 ENCODER
45	BIST-45	7	CORE1 VLC MEM	H264 ENCODER
45	BIST-45	8	CORE1 VLC MEM	H264 ENCODER
45	BIST-45	9	CORE1 VLC MEM	H264 ENCODER
45	BIST-45	10	CORE1 VLC MEM	H264 ENCODER
45	BIST-45	11	CORE0 BIT-STREAM BUFFER MEM0	H264 ENCODER
45	BIST-45	12	CORE0 BIT-STREAM BUFFER MEM1	H264 ENCODER
45	BIST-45	13	CORE1 BIT-STREAM BUFFER MEM0	H264 ENCODER
45	BIST-45	14	CORE1 BIT-STREAM BUFFER MEM1	H264 ENCODER
45	BIST-45	15	COMMON EMULATION PREVENTION FIFO MEM0	H264 ENCODER

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Table 2. MBIST Mapping (continued)

45	BIST-45	16	COMMON EMULATION PREVENTION FIFO MEM1	H264 ENCODER
45	BIST-45	17	COMMON BIT-STREAM BUFFER MEM	H264 ENCODER
46	BIST-46	0	RESIDUAL MEM0	H264 DECODER
46	BIST-46	1	RESIDUAL MEM1	H264 DECODER
46	BIST-46	2	RESIDUAL MEM2	H264 DECODER
46	BIST-46	3	RESIDUAL MEM3	H264 DECODER
47	BIST-47	0	INTRA-PREDICTION BORDER PIXEL ROW MEM0	H264 DECODER
47	BIST-47	1	INTRA-PREDICTION BORDER PIXEL ROW MEM1	H264 DECODER
47	BIST-47	2	INTRA-PREDICTION BORDER PIXEL ROW MEM2	H264 DECODER
47	BIST-47	3	INTRA-PREDICTION BORDER PIXEL ROW MEM3	H264 DECODER
48	BIST-48	0	AXI WRITE BRIDGE FIFO MEM	H264 DECODER
48	BIST-48	1	DEBLOCK FILTER MEM0	H264 DECODER
48	BIST-48	2	DEBLOCK FILTER MEM1	H264 DECODER
48	BIST-48	3	DEBLOCK FILTER MEM2	H264 DECODER
48	BIST-48	4	DEBLOCK FILTER MEM3	H264 DECODER
48	BIST-48	5	AXI READ BRIDGE FIFO MEM	H264 DECODER
48	BIST-48	6	AXI READ BRIDGE FIFO MEM	H264 DECODER
48	BIST-48	7	AXI WRITE BRIDGE FIFO MEM	H264 DECODER
48	BIST-48	8	AXI WRITE BRIDGE FIFO MEM	H264 DECODER
48	BIST-48	9	PORT SPLITTER_A FIFO MEM0	H264 DECODER
48	BIST-48	10	PORT SPLITTER_B FIFO MEM0	H264 DECODER
48	BIST-48	11	PORT SPLITTER_C FIFO MEM0	H264 DECODER

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Table 2. MBIST Mapping (continued)

48	BIST-48	12	PORT SPLITTER_D FIFO MEM0	H264 DECODER
48	BIST-48	13	PORT SPLITTER_A FIFO MEM1	H264 DECODER
48	BIST-48	14	PORT SPLITTER_B FIFO MEM1	H264 DECODER
48	BIST-48	15	PORT SPLITTER_C FIFO MEM1	H264 DECODER
48	BIST-48	16	PORT SPLITTER_D FIFO MEM1	H264 DECODER
49	BIST-49	0	VARIABLE LENGTH DECODER0 MEM	H264 DECODER
49	BIST-49	1	VARIABLE LENGTH DECODER0 MEM	H264 DECODER
49	BIST-49	2	VARIABLE LENGTH DECODER0 MEM	H264 DECODER
49	BIST-49	3	VARIABLE LENGTH DECODER0 MEM	H264 DECODER
49	BIST-49	4	VARIABLE LENGTH DECODER1 MEM	H264 DECODER
49	BIST-49	5	VARIABLE LENGTH DECODER1 MEM	H264 DECODER
49	BIST-49	6	VARIABLE LENGTH DECODER1 MEM	H264 DECODER
49	BIST-49	7	VARIABLE LENGTH DECODER1 MEM	H264 DECODER
49	BIST-49	8	VARIABLE LENGTH DECODER2 MEM	H264 DECODER
49	BIST-49	9	VARIABLE LENGTH DECODER2 MEM	H264 DECODER
49	BIST-49	10	VARIABLE LENGTH DECODER2 MEM	H264 DECODER
49	BIST-49	11	VARIABLE LENGTH DECODER2 MEM	H264 DECODER
49	BIST-49	12	VARIABLE LENGTH DECODER3 MEM	H264 DECODER
49	BIST-49	13	VARIABLE LENGTH DECODER3 MEM	H264 DECODER
49	BIST-49	14	VARIABLE LENGTH DECODER3 MEM	H264 DECODER
49	BIST-49	15	VARIABLE LENGTH DECODER3 MEM	H264 DECODER
50	BIST-50	0	VARIABLE LENGTH DECODER0 MEM	H264 DECODER
50	BIST-50	1	VARIABLE LENGTH DECODER0 MEM	H264 DECODER

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Table 2. MBIST Mapping (continued)

50	BIST-50	2	MOTION COMPENSATION OUTPUT DATA MEM	H264 DECODER
50	BIST-50	3	VARIABLE LENGTH DECODER0 MEM	H264 DECODER
50	BIST-50	4	VARIABLE LENGTH DECODER0 MEM	H264 DECODER
50	BIST-50	5	VARIABLE LENGTH DECODER1 MEM	H264 DECODER
50	BIST-50	6	VARIABLE LENGTH DECODER2 MEM	H264 DECODER
50	BIST-50	7	VARIABLE LENGTH DECODER3 MEM	H264 DECODER
50	BIST-50	8	VARIABLE LENGTH DECODER0 MEM	H264 DECODER
50	BIST-50	9	VARIABLE LENGTH DECODER1 MEM	H264 DECODER
50	BIST-50	10	VARIABLE LENGTH DECODER2 MEM	H264 DECODER
50	BIST-50	11	VARIABLE LENGTH DECODER3 MEM	H264 DECODER
51	BIST-51	0	MOTION COMPENSATION CACHE DATA MEM0	H264 DECODER
51	BIST-51	1	MOTION COMPENSATION CACHE DATA MEM1	H264 DECODER
51	BIST-51	2	VIDEO OUTPUT0 MEMA_0	H264 DECODER
51	BIST-51	3	VIDEO OUTPUT0 MEMA_1	H264 DECODER
51	BIST-51	4	VIDEO OUTPUT0 MEMB_0	H264 DECODER
51	BIST-51	5	VIDEO OUTPUT0 MEMB_1	H264 DECODER
51	BIST-51	6	VIDEO OUTPUT1 MEMA_0	H264 DECODER
51	BIST-51	7	VIDEO OUTPUT1 MEMA_1	H264 DECODER
51	BIST-51	8	VIDEO OUTPUT1 MEMB_0	H264 DECODER
51	BIST-51	9	VIDEO OUTPUT1 MEMB_1	H264 DECODER
51	BIST-51	10	VIDEO OUTPUT2 MEMA_0	H264 DECODER
51	BIST-51	11	VIDEO OUTPUT2 MEMA_1	H264 DECODER

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Table 2. MBIST Mapping (continued)

51	BIST-51	12	VIDEO OUTPUT2 MEMB_0	H264 DECODER
51	BIST-51	13	VIDEO OUTPUT2 MEMB_1	H264 DECODER
51	BIST-51	14	VIDEO OUTPUT3 MEMA_0	H264 DECODER
51	BIST-51	15	VIDEO OUTPUT3 MEMA_1	H264 DECODER
51	BIST-51	16	VIDEO OUTPUT3 MEMB_0	H264 DECODER
51	BIST-51	17	VIDEO OUTPUT3 MEMB_1	H264 DECODER
52	BIST-52	0	CORE0 INTRA-PREDICTION MEM	H264 ENCODER
52	BIST-52	1	CORE0 INTRA-PREDICTION MEM	H264 ENCODER
52	BIST-52	2	CORE1 INTRA-PREDICTION MEM	H264 ENCODER
52	BIST-52	3	CORE1 INTRA-PREDICTION MEM	H264 ENCODER
52	BIST-52	4	CORE0 INTRA-PREDICTION MEM	H264 ENCODER
52	BIST-52	5	CORE0 INTRA-PREDICTION MEM	H264 ENCODER
52	BIST-52	6	CORE0 INTRA-PREDICTION MEM	H264 ENCODER
52	BIST-52	7	CORE0 INTRA-PREDICTION MEM	H264 ENCODER
52	BIST-52	8	CORE1 INTRA-PREDICTION MEM	H264 ENCODER
52	BIST-52	9	CORE1 INTRA-PREDICTION MEM	H264 ENCODER
52	BIST-52	10	CORE1 INTRA-PREDICTION MEM	H264 ENCODER
52	BIST-52	11	CORE1 INTRA-PREDICTION MEM	H264 ENCODER
53	BIST-53	0	CORE0 INTRA-PREDICTION MEM	H264 ENCODER ROM
53	BIST-53	1	CORE1 INTRA-PREDICTION MEM	H264 ENCODER ROM
54	BIST-54	0	DEBLOCK FILTER MEM0	H264 DECODER ROM
54	BIST-54	1	DEBLOCK FILTER MEM1	H264 DECODER ROM
54	BIST-54	2	DEBLOCK FILTER MEM2	H264 DECODER ROM

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Table 2. MBIST Mapping (continued)

54	BIST-54	3	DEBLOCK FILTER MEM3	H264 DECODER ROM
55	BIST-55	0	DEBLOCK FILTER MEM0	H264 DECODER
55	BIST-55	1	DEBLOCK FILTER MEM0	H264 DECODER
55	BIST-55	2	DEBLOCK FILTER MEM0	H264 DECODER
55	BIST-55	3	DEBLOCK FILTER MEM0	H264 DECODER
55	BIST-55	4	DEBLOCK FILTER MEM0	H264 DECODER
55	BIST-55	5	DEBLOCK FILTER MEM0	H264 DECODER
55	BIST-55	6	DEBLOCK FILTER MEM0	H264 DECODER
55	BIST-55	7	DEBLOCK FILTER MEM0	H264 DECODER
55	BIST-55	8	DEBLOCK FILTER MEM1	H264 DECODER
55	BIST-55	9	DEBLOCK FILTER MEM1	H264 DECODER
55	BIST-55	10	DEBLOCK FILTER MEM1	H264 DECODER
55	BIST-55	11	DEBLOCK FILTER MEM1	H264 DECODER
55	BIST-55	12	DEBLOCK FILTER MEM1	H264 DECODER
55	BIST-55	13	DEBLOCK FILTER MEM1	H264 DECODER
55	BIST-55	14	DEBLOCK FILTER MEM1	H264 DECODER
55	BIST-55	15	DEBLOCK FILTER MEM1	H264 DECODER
56	BIST-56	0	DEBLOCK FILTER MEM2	H264 DECODER
56	BIST-56	1	DEBLOCK FILTER MEM2	H264 DECODER
56	BIST-56	2	DEBLOCK FILTER MEM2	H264 DECODER
56	BIST-56	3	DEBLOCK FILTER MEM2	H264 DECODER
56	BIST-56	4	DEBLOCK FILTER MEM2	H264 DECODER
56	BIST-56	5	DEBLOCK FILTER MEM2	H264 DECODER

Table continues on the next page...

Table 2. MBIST Mapping (continued)

56	BIST-56	6	DEBLOCK FILTER MEM2	H264 DECODER
56	BIST-56	7	DEBLOCK FILTER MEM2	H264 DECODER
56	BIST-56	8	DEBLOCK FILTER MEM3	H264 DECODER
56	BIST-56	9	DEBLOCK FILTER MEM3	H264 DECODER
56	BIST-56	10	DEBLOCK FILTER MEM3	H264 DECODER
56	BIST-56	11	DEBLOCK FILTER MEM3	H264 DECODER
56	BIST-56	12	DEBLOCK FILTER MEM3	H264 DECODER
56	BIST-56	13	DEBLOCK FILTER MEM3	H264 DECODER
56	BIST-56	14	DEBLOCK FILTER MEM3	H264 DECODER
56	BIST-56	15	DEBLOCK FILTER MEM3	H264 DECODER
57	BIST-57	0	RAM0_MEM0	GC3000
57	BIST-57	1	RAM1_MEM0	GC3000
57	BIST-57	2	RAM2_MEM0	GC3000
57	BIST-57	3	RAM3_MEM0	GC3000
57	BIST-57	4	RAM4_MEM0	GC3000
57	BIST-57	5	RAM5_MEM0	GC3000
57	BIST-57	6	RAM6_MEM0	GC3000
57	BIST-57	7	RAM7_MEM0	GC3000
57	BIST-57	8	RAM8_MEM0	GC3000
57	BIST-57	9	RAM9_MEM0	GC3000
57	BIST-57	10	RAM10_MEM0	GC3000
58	BIST-58	0	RAM15_MEM0	GC3000
58	BIST-58	1	RAM16_MEM0	GC3000
58	BIST-58	2	RAM17_MEM0	GC3000
58	BIST-58	3	RAM18_MEM0	GC3000
58	BIST-58	4	RAM19_MEM0	GC3000
58	BIST-58	5	RAM20_MEM0	GC3000
58	BIST-58	6	RAM21_MEM0	GC3000
58	BIST-58	7	RAM22_MEM0	GC3000
58	BIST-58	8	RAM23_MEM0	GC3000
58	BIST-58	9	RAM24_MEM0	GC3000
58	BIST-58	10	RAM25_MEM0	GC3000
58	BIST-58	11	RAM26_MEM0	GC3000

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Table 2. MBIST Mapping (continued)

58	BIST-58	12	RAM27_MEM0	GC3000
58	BIST-58	13	RAM28_MEM1	GC3000
58	BIST-58	14	RAM29_MEM0	GC3000
58	BIST-58	15	RAM30_MEM1	GC3000
58	BIST-58	16	RAM31_MEM0	GC3000
58	BIST-58	17	RAM32_MEM0	GC3000
58	BIST-58	18	RAM33_MEM0	GC3000
58	BIST-58	19	RAM34_MEM0	GC3000
59	BIST-59	0	RAM35_MEM0	GC3000
59	BIST-59	1	RAM36_MEM0	GC3000
59	BIST-59	2	RAM37_MEM0	GC3000
59	BIST-59	3	RAM38_MEM0	GC3000
59	BIST-59	4	RAM39_MEM0	GC3000
59	BIST-59	5	RAM40_MEM0	GC3000
59	BIST-59	6	RAM41_MEM0	GC3000
59	BIST-59	7	RAM42_MEM0	GC3000
59	BIST-59	8	RAM43_MEM0	GC3000
59	BIST-59	9	RAM44_MEM0	GC3000
59	BIST-59	10	RAM45_MEM1	GC3000
59	BIST-59	11	RAM46_MEM0	GC3000
59	BIST-59	12	RAM47_MEM1	GC3000
59	BIST-59	13	RAM48_MEM0	GC3000
59	BIST-59	14	RAM49_MEM0	GC3000
59	BIST-59	15	RAM50_MEM0	GC3000
59	BIST-59	16	RAM51_MEM0	GC3000
60	BIST-60	0	RAM52_MEM0	GC3000
60	BIST-60	1	RAM53_MEM1	GC3000
60	BIST-60	2	RAM54_MEM2	GC3000
60	BIST-60	3	RAM55_MEM3	GC3000
60	BIST-60	4	RAM56_MEM0	GC3000
60	BIST-60	5	RAM57_MEM1	GC3000
60	BIST-60	6	RAM58_MEM2	GC3000
60	BIST-60	7	RAM59_MEM3	GC3000
60	BIST-60	8	RAM80_MEM0	GC3000
60	BIST-60	9	RAM81_MEM0	GC3000
60	BIST-60	10	RAM82_MEM0	GC3000
60	BIST-60	11	RAM83_MEM0	GC3000
60	BIST-60	12	RAM84_MEM0	GC3000
61	BIST-61	0	RAM86_MEM0	GC3000
61	BIST-61	1	RAM87_MEM0	GC3000

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Table 2. MBIST Mapping (continued)

61	BIST-61	2	RAM88_MEM0	GC3000
61	BIST-61	3	RAM89_MEM0	GC3000
61	BIST-61	4	RAM90_MEM0	GC3000
61	BIST-61	5	RAM91_MEM0	GC3000
61	BIST-61	6	RAM92_MEM0	GC3000
61	BIST-61	7	RAM93_MEM0	GC3000
61	BIST-61	8	RAM94_MEM1	GC3000
62	BIST-62	0	DEC_MEM0	DEC 200 Decoder
62	BIST-62	1	DEC_MEM1	DEC 200 Decoder
63	BIST-63	0	RAM97_MEM0	GC3000
63	BIST-63	1	RAM98_MEM0	GC3000
63	BIST-63	2	RAM99_MEM0	GC3000
63	BIST-63	3	RAM100_MEM1	GC3000
63	BIST-63	4	RAM101_MEM0	GC3000
63	BIST-63	5	RAM102_MEM1	GC3000
63	BIST-63	6	RAM103_MEM0	GC3000
63	BIST-63	7	RAM104_MEM1	GC3000
63	BIST-63	8	RAM105_MEM0	GC3000
63	BIST-63	9	RAM106_MEM1	GC3000
63	BIST-63	10	RAM107_MEM0	GC3000
63	BIST-63	11	RAM108_MEM0	GC3000
64	BIST-64	0	RAM11_MEM0	GC3000
64	BIST-64	1	RAM12_MEM0	GC3000
64	BIST-64	2	RAM13_MEM0	GC3000
64	BIST-64	3	RAM14_MEM0	GC3000
65	BIST-65	0	RAM142_MEM0	GC3000
65	BIST-65	1	RAM143_MEM1	GC3000
65	BIST-65	2	RAM144_MEM0	GC3000
66	BIST-66	0	RAM184_MEM0	GC3000
66	BIST-66	1	RAM185_MEM0	GC3000
66	BIST-66	2	RAM186_MEM0	GC3000
66	BIST-66	3	RAM186_MEM1	GC3000
66	BIST-66	4	RAM186_MEM2	GC3000
66	BIST-66	5	RAM186_MEM3	GC3000
66	BIST-66	6	RAM187_MEM0	GC3000
67	BIST-67	0	RAM109_MEM0	GC3000
67	BIST-67	1	RAM110_MEM0	GC3000
67	BIST-67	2	RAM111_MEM1	GC3000
67	BIST-67	3	RAM112_MEM0	GC3000
67	BIST-67	4	RAM113_MEM1	GC3000

Table continues on the next page...

Table 2. MBIST Mapping (continued)

67	BIST-67	5	RAM114_MEM0	GC3000
67	BIST-67	6	RAM115_MEM1	GC3000
67	BIST-67	7	RAM116_MEM0	GC3000
67	BIST-67	8	RAM117_MEM1	GC3000
67	BIST-67	9	RAM118_MEM0	GC3000
67	BIST-67	10	RAM119_MEM0	GC3000
68	BIST-68	0	RAM120_MEM0	GC3000
68	BIST-68	1	RAM121_MEM0	GC3000
68	BIST-68	2	RAM122_MEM1	GC3000
68	BIST-68	3	RAM123_MEM0	GC3000
68	BIST-68	4	RAM124_MEM1	GC3000
68	BIST-68	5	RAM125_MEM0	GC3000
68	BIST-68	6	RAM126_MEM1	GC3000
68	BIST-68	7	RAM127_MEM0	GC3000
68	BIST-68	8	RAM128_MEM1	GC3000
68	BIST-68	9	RAM129_MEM0	GC3000
68	BIST-68	10	RAM130_MEM0	GC3000
69	BIST-69	0	RAM131_MEM0	GC3000
69	BIST-69	1	RAM132_MEM0	GC3000
69	BIST-69	2	RAM133_MEM1	GC3000
69	BIST-69	3	RAM134_MEM0	GC3000
69	BIST-69	4	RAM135_MEM1	GC3000
69	BIST-69	5	RAM136_MEM0	GC3000
69	BIST-69	6	RAM137_MEM1	GC3000
69	BIST-69	7	RAM138_MEM0	GC3000
69	BIST-69	8	RAM139_MEM1	GC3000
69	BIST-69	9	RAM140_MEM0	GC3000
69	BIST-69	10	RAM141_MEM0	GC3000
70	BIST-70	0	RAM145_MEM0	GC3000
70	BIST-70	1	RAM146_MEM0	GC3000
70	BIST-70	2	RAM147_MEM0	GC3000
70	BIST-70	3	RAM148_MEM0	GC3000
71	BIST-71	0	RAM149_MEM0	GC3000
71	BIST-71	1	RAM150_MEM0	GC3000
71	BIST-71	2	RAM151_MEM0	GC3000
71	BIST-71	3	RAM152_MEM0	GC3000
71	BIST-71	4	RAM153_MEM0	GC3000
71	BIST-71	5	RAM154_MEM0	GC3000
71	BIST-71	6	RAM155_MEM0	GC3000
71	BIST-71	7	RAM156_MEM0	GC3000

Table continues on the next page...

Table 2. MBIST Mapping (continued)

71	BIST-71	8	RAM157_MEM0	GC3000
71	BIST-71	9	RAM158_MEM0	GC3000
71	BIST-71	10	RAM159_MEM0	GC3000
71	BIST-71	11	RAM160_MEM0	GC3000
71	BIST-71	12	RAM162_MEM0	GC3000
71	BIST-71	13	RAM164_MEM0	GC3000
71	BIST-71	14	RAM165_MEM0	GC3000
71	BIST-71	15	RAM166_MEM0	GC3000
71	BIST-71	16	RAM167_MEM0	GC3000
71	BIST-71	17	RAM168_MEM0	GC3000
71	BIST-71	18	RAM169_MEM0	GC3000
72	BIST-72	0	RAM172_MEM0	GC3000
72	BIST-72	1	RAM173_MEM0	GC3000
72	BIST-72	2	RAM174_MEM0	GC3000
72	BIST-72	3	RAM175_MEM0	GC3000
72	BIST-72	4	RAM176_MEM0	GC3000
72	BIST-72	5	RAM177_MEM0	GC3000
72	BIST-72	6	RAM178_MEM0	GC3000
72	BIST-72	7	RAM179_MEM0	GC3000
72	BIST-72	8	RAM180_MEM0	GC3000
72	BIST-72	9	RAM181_MEM0	GC3000
72	BIST-72	10	RAM182_MEM0	GC3000
72	BIST-72	11	RAM183_MEM0	GC3000
73	BIST-73	0	RAM170_MEM0	GC3000
73	BIST-73	1	RAM171_MEM0	GC3000
74	BIST-74	0	RAM188_MEM0	GC3000
74	BIST-74	1	RAM189_MEM1	GC3000
74	BIST-74	2	RAM190_MEM0	GC3000
74	BIST-74	3	RAM191_MEM0	GC3000
74	BIST-74	4	RAM192_MEM0	GC3000
74	BIST-74	5	RAM193_MEM0	GC3000
74	BIST-74	6	RAM194_MEM0	GC3000
74	BIST-74	7	RAM195_MEM0	GC3000
74	BIST-74	8	RAM196_MEM0	GC3000
74	BIST-74	9	RAM197_MEM0	GC3000
74	BIST-74	10	RAM198_MEM0	GC3000
74	BIST-74	11	RAM199_MEM0	GC3000
74	BIST-74	12	RAM200_MEM0	GC3000
74	BIST-74	13	RAM201_MEM0	GC3000
74	BIST-74	14	RAM202_MEM0	GC3000

Table continues on the next page...

Table 2. MBIST Mapping (continued)

74	BIST-74	15	RAM203_MEM0	GC3000
74	BIST-74	16	RAM204_MEM0	GC3000
74	BIST-74	17	RAM205_MEM0	GC3000
74	BIST-74	18	RAM206_MEM0	GC3000
74	BIST-74	19	RAM207_MEM0	GC3000
75	BIST-75	0	RAM85_MEM0	GC3000
75	BIST-75	1	RAM95_MEM0	GC3000
75	BIST-75	2	RAM96_MEM1	GC3000
75	BIST-75	3	RAM208_MEM0	GC3000
76	BIST-76	0	RAM60_MEM0	GC3000
76	BIST-76	1	RAM61_MEM1	GC3000
76	BIST-76	2	RAM62_MEM0	GC3000
76	BIST-76	3	RAM63_MEM1	GC3000
76	BIST-76	4	RAM64_MEM0	GC3000
76	BIST-76	5	RAM65_MEM1	GC3000
76	BIST-76	6	RAM66_MEM0	GC3000
76	BIST-76	7	RAM67_MEM1	GC3000
76	BIST-76	8	RAM68_MEM0	GC3000
76	BIST-76	9	RAM69_MEM1	GC3000
77	BIST-77	0	RAM70_MEM0	GC3000
77	BIST-77	1	RAM71_MEM1	GC3000
77	BIST-77	2	RAM72_MEM0	GC3000
77	BIST-77	3	RAM73_MEM1	GC3000
77	BIST-77	4	RAM74_MEM0	GC3000
77	BIST-77	5	RAM75_MEM1	GC3000
77	BIST-77	6	RAM76_MEM0	GC3000
77	BIST-77	7	RAM77_MEM1	GC3000
77	BIST-77	8	RAM78_MEM0	GC3000
77	BIST-77	9	RAM79_MEM1	GC3000

NOTE

- Refer to DDR Contents Retention during Self-Test (See MMDC chapter in S32V234RM, Rev 3).
- MBIST only selftest should be followed by reset. The SRC_GPR27[RST_AFT_MBISTONLY_SLFTST] can be used for reset assertion after MBIST execution.
- SRC_GPR27[RST_AFT_MBISTONLY_SLFTST] bit also issues a long functional reset to the device in case selftest gets aborted during MBIST execution or before the start of LBIST execution in an LBIST enabled selftest. Therefore, it is highly recommended to always program this bit to 1 before running any selftest.
- To assert the RESET pin, during the Selftest initiated by STCU, SRC_GPR27[EXT_RST_ASSERT_DIS] bit can be used.
    - It is mandatory to assert the RESET pin during the LBIST initiated by STCU.
- MBIST initiated by STCU causes the clock gating of all the IPs except for GPU.

- MBIST initiated by MTR/MCT does not cause clock gating of IPs.
- When the Cortex-A53 is powered down, the MSEL should be deselected to ensure the non-failure of MBIST due to these memories.
- After Selftest, the STCU CF status should be checked if the FCCU reaction is not set (If the FCCU reaction is disabled and the RGM reset is disabled through the SRC_GPR27[STCU_UF_RST_DIS]).
- STCU interrupts cannot be serviced in between the self test run.
- If GPU GC3000 BIST tests are excluded and for this reason the GPU is disabled, the BIST_BSTAT register may show wrong values for the GPU. This does not have any adverse effect since the results of the GPU should be ignored.

4 Clocking requirement

To ensure proper BIST-sequence execution, before executing a BIST sequence, make sure to program all of the PLL clock selectors to use FXOSC_CLK.

5 Part Number and STCU configuration

This table gives the Part number mapping with STCU2 configuration.

Part Number	STCU2 configuration
FS32V234CMN1VUB	STCU2 FULL
FS32V234CON1VUB	STCU2 FULL
FS32V234BMN1VUB	STCU2 FULL
FS32V234BJN1VUB	STCU2 FULL Option 1
FS32V232BMN1VUB	STCU2 FULL Option 2
FS32V234BLN1VUB	STCU2 FULL Option 1

6 Supported Online BIST Sequence

6.1 Supported Online BIST Sequence

6.1.1 Specifications

This table gives the specifications for the supported online built-in self-test (BIST) sequences.

Specification	Sequence 1	Sequence 2	Sequence 3	Sequence 4	—
Description	Full	Full + Option 1	Full + Option 2	Full + Option 1 + Option 2	—

Table continues on the next page...

Specification		Sequence 1	Sequence 2	Sequence 3	Sequence 4	—
Execution time (ms)[1]	BSCCHK + MEMINIT	38.9	34.2	38.9	34.2	—
	March C +Single (MCPS) BSCCHK MEMINIT	44.20	39.5	44.20	39.5	—
LBIST coverage, stuck-at, minimum (%)[2]		90	90	90	90	—
LBIST coverage, transition, minimum (%)[2]		—	—	—	—	—
Configuration		See Online BIST sequence 1 configuration.	See Online BIST sequence 2 configuration.	See Online BIST sequence 3 configuration.	See Online BIST sequence 4 configuration.	—

Specification		Sequence 5	Sequence 6	Sequence 7	Sequence 8	Sequence 9
Description		Full Fast—same as sequence 1 but with less extensive LBIST coverage, resulting in a lower execution time	Full Fast + Option 1—same as sequence 2 but with less extensive LBIST coverage, resulting in a lower execution time	Full Fast + Option 2—same as sequence 3 but with less extensive LBIST coverage, resulting in a lower execution time	Full Fast + Option 1 + Option 2—same as sequence 4 but with less extensive LBIST coverage, resulting in a lower execution time	Sensor Fusion
Execution time (ms)[1]	BSCCHK + MEMINIT	21.5	20.5	21.35	20.6	29.2
	March C +Single (MCPS) + BSCCHK + MEMINIT	26.7	25.8	26.7	25.8	34.5
LBIST coverage, stuck-at, minimum (%)[2]		80	80	80	80	90
LBIST coverage, transition, minimum (%)[2]		—	—	—	—	—
Configuration		See Online BIST sequence 5 configuration.	See Online BIST sequence 6 configuration.	See Online BIST sequence 7 configuration.	See Online BIST sequence 8 configuration.	See Online BIST sequence 9 configuration.

1. The time it takes to execute the BIST sequence using the specified MBIST algorithm with all of the PLL-derived clocks programmed for the frequencies shown in [[Table 22-1]] (and the ENET-PLL DFS3 clock programmed for 320 MHz) and with all of the system clocks and all of the module clocks for modules included in the BIST sequence programmed for the frequencies shown in [[Table 22-6]]. These tables can be found in S32V234 Reference Manual, Rev3.
2. A sequence can be configured to test stuck-at coverage or transition coverage but not both. A dash (—) indicates that this type of test coverage is not the objective of the sequence.

Important

NXP has validated and therefore supports only the online BIST sequences in the table above.

6.2 Online BIST sequence 1 configuration

6.2.1 MBISTs executed

For online built-in self-test (BIST) sequence 1, STCU2 executes the following MBISTs in the order shown:

Phase	MBISTs executed
0	11, 24 , 29, 34, 42, 43, 51, 52, 57, 66, 72, 77
1	17, 21, 25, 30, 35, 36, 46, 53, 58, 61, 62, 63, 70
2	7, 10, 19, 26, 31, 38, 40, 45, 50, 54, 59, 68, 74
3	4, 9, 12, 14, 16, 27, 32, 48, 56, 60, 69, 75
4	5, 8, 15, 20, 28, 37, 41, 47, 55, 65, 71, 76
5	6, 13, 18, 22, 23, 33, 39, 44, 49, 64, 67, 73
6	0, 1, 2, 3

6.2.2 LBISTs executed

For online built-in self-test (BIST) sequence 1, STCU2 executes the following LBISTs in the order shown with the indicated coverage:

Phase	LBISTs executed	Coverage, stuck-at (%)
7	6	90
	23	90
	24	90
8	7	90
	25	90
	26	90
9	3	90
	5	90
10	2	90
	4	90
11	10	90
	12	90
12	11	90
	13	90
13	9	90
	17	90
14	15	90

Table continues on the next page...

Phase	LBISTs executed	Coverage, stuck-at (%)
	22	90
15	8	90
	16	90
	21	90
16	0	90
	1	90
	14	90
17	18	90
18	19	90
19	20	90

6.3 Online BIST sequence 2 configuration

6.3.1 MBISTs executed

For online built-in self-test (BIST) sequence 2, STCU2 executes the following MBISTs in the order shown:

Phase	MBISTs executed
0	11, 24, 29, 34, 42, 43, 51, 52
1	17, 21, 25, 30, 35, 36, 46, 53, 62
2	7, 10, 19, 26, 31, 38, 40, 45, 50, 54
3	4, 9, 12, 14, 16, 27, 32, 48, 56
4	5, 8, 15, 20, 28, 37, 41, 47, 55
5	6, 13, 18, 22, 23, 33, 39, 44, 49
6	0, 1, 2, 3

6.3.2 LBISTs executed

For online built-in self-test (BIST) sequence 2, STCU2 executes the following LBISTs in the order shown with the indicated coverage:

Phase	LBISTs executed	Coverage, stuck-at (%)
7	6	90
	23	90
	24	90
8	7	90

Table continues on the next page...

Phase	LBISTs executed	Coverage, stuck-at (%)
	25	90
	26	90
9	3	90
	5	90
10	2	90
	4	90
11	10	90
	12	90
12	11	90
	13	90
13	9	90
	17	90
14	15	90
	22	90
15	8	90
	16	90
	21	90
16	0	90
	1	90
	14	90

6.4 Online BIST sequence 3 configuration

6.4.1 MBISTs executed

For online built-in self-test (BIST) sequence 3, STCU2 executes the following MBISTs in the order shown:

Phase	MBISTs executed
0	11, 24, 29, 34, 42, 43, 51, 52, 57, 66, 72, 77
1	17, 21, 25, 30, 35, 36, 46, 53, 58, 61, 62, 63, 70
2	7, 10, 19, 26, 31, 38, 40, 45, 50, 54, 59, 68, 74
3	4, 9, 12, 14, 16, 27, 32, 48, 56, 60, 69, 75
4	5, 8, 15, 20, 28, 37, 41, 47, 55, 65, 71, 76
5	6, 13, 18, 22, 23, 33, 39, 44, 49, 64, 67, 73
6	0, 1, 2, 3

6.4.2 LBISTs executed

For online built-in self-test (BIST) sequence 3, STCU2 executes the following LBISTs in the order shown with the indicated coverage:

Phase	LBISTs executed	Coverage, stuck-at (%)
7	6	90
	23	90
8	7	90
	25	90
9	3	90
	5	90
10	2	90
	4	90
11	10	90
	12	90
12	11	90
	13	90
13	9	90
	17	90
14	15	90
	22	90
15	8	90
	16	90
	21	90
16	0	90
	1	90
	14	90
17	18	90
18	19	90
19	20	90

6.5 Online BIST sequence 4 configuration

6.5.1 MBISTs executed

For online built-in self-test (BIST) sequence 4, STCU2 executes the following MBISTs in the order shown:

Phase	MBISTs executed
0	11, 24, 29, 34 42, 43, 51, 52

Table continues on the next page...

Phase	MBISTs executed
1	17, 21, 25, 30, 35, 36, 46, 53, 62
2	7, 10, 19, 26, 31, 38, 40, 45, 50
3	4, 9, 12, 14, 16, 27, 32, 48, 56
4	5, 8, 15, 20, 28, 37, 41, 47, 55
5	6, 13, 18, 22, 23, 33, 39, 44, 49
6	0, 1, 2, 3

6.5.2 LBISTs executed

For online built-in self-test (BIST) sequence 4, STCU2 executes the following LBISTs in the order shown with the indicated coverage:

Phase	LBISTs executed	Coverage, stuck-at (%)
7	6	90
	23	90
8	7	90
	25	90
9	3	90
	5	90
10	2	90
	4	90
11	10	90
	12	90
12	11	90
	13	90
13	9	90
	17	90
14	15	90
	22	90
15	8	90
	16	90
	21	90
16	0	90
	1	90
	14	90

6.6 Online BIST sequence 5 configuration

6.6.1 MBISTs executed

For online built-in self-test (BIST) sequence 5, STCU2 executes the following MBISTs in the order shown:

Phase	MBISTs executed
0	11, 24 , 29, 34, 42, 43, 51, 52, 57, 66, 72, 77
1	17, 21, 25, 30, 35, 36, 46, 53, 58, 61, 62, 63, 70
2	7, 10, 19, 26, 31, 38, 40, 45, 50, 54, 59, 68, 74
3	4, 9, 12, 14, 16, 27, 32, 48, 56, 60, 69, 75
4	5, 8, 15, 20, 28, 37, 41, 47, 55, 65, 71, 76
5	6, 13, 18, 22, 23, 33, 39, 44, 49, 64, 67, 73
6	0, 1, 2, 3

6.6.2 LBISTs executed

For online built-in self-test (BIST) sequence 5, STCU2 executes the following LBISTs in the order shown with the indicated coverage:

Phase	LBISTs executed	Coverage, stuck-at (%)
7	6	90
	23	90
	24	90
8	7	90
	25	90
	26	90
9	3	80
	5	80
10	2	80
	4	80
11	10	80
	12	80
12	11	80
	13	80
13	9	80
	17	80
14	15	80
	22	80

Table continues on the next page...

Phase	LBISTs executed	Coverage, stuck-at (%)
15	8	80
	16	80
	21	90
16	0	80
	1	80
	14	80
17	18	80
18	19	80
19	20	80

6.7 Online BIST sequence 6 configuration

6.7.1 MBISTs executed

For online built-in self-test (BIST) sequence 6, STCU2 executes the following MBISTs in the order shown:

Phase	MBISTs executed
0	11, 24, 29, 34, 42, 43, 51, 52
1	17, 21, 25, 30, 35, 36, 46, 53, 62
2	7, 10, 19, 26, 31, 38, 40, 45, 50, 54
3	4, 9, 12, 14, 16, 27, 32, 48, 56
4	5, 8, 15, 20, 28, 37, 41, 47, 55
5	6, 13, 18, 22, 23, 33, 39, 44, 49
6	0, 1, 2, 3

6.7.2 LBISTs executed

For online built-in self-test (BIST) sequence 6, STCU2 executes the following LBISTs in the order shown with the indicated coverage:

Phase	LBISTs executed	Coverage, stuck-at (%)
7	6	90
	23	90
	24	90
8	7	90
	25	90
	26	90

Table continues on the next page...

Phase	LBISTs executed	Coverage, stuck-at (%)
9	3	80
	5	80
10	2	80
	4	80
11	10	80
	12	80
12	11	80
	13	80
13	9	80
	17	80
14	15	80
	22	80
15	8	80
	16	80
	21	90
16	0	80
	1	80
	14	80

6.8 Online BIST sequence 7 configuration

6.8.1 MBISTs executed

For online built-in self-test (BIST) sequence 7, STCU2 executes the following MBISTs in the order shown:

Phase	MBISTs executed
0	11, 24, 29, 34, 42, 43, 51, 52, 57, 66, 72, 77
1	17, 21, 25, 30, 35, 36, 46, 53, 58, 61, 62, 63, 70
2	7, 10, 19, 26, 31, 38, 40, 45, 50, 54, 59, 68, 74
3	4, 9, 12, 14, 16, 27, 32, 48, 56, 60, 69, 75
4	5, 8, 15, 20, 28, 37, 41, 47, 55, 65, 71, 76
5	6, 13, 18, 22, 23, 33, 39, 44, 49, 64, 67, 73
6	0, 1, 2, 3

6.8.2 LBISTs executed

For online built-in self-test (BIST) sequence 7, STCU2 executes the following LBISTs in the order shown with the indicated coverage:

Phase	LBISTs executed	Coverage, stuck-at (%)
7	6	90
	23	90
8	7	90
	25	90
9	3	80
	5	80
10	2	80
	4	80
11	10	80
	12	80
12	11	80
	13	80
13	9	80
	17	80
14	15	80
	22	80
15	8	80
	16	80
	21	90
16	0	80
	1	80
	14	80
17	18	80
18	19	80
19	20	80

6.9 Online BIST sequence 8 configuration

6.9.1 MBISTs executed

For online built-in self-test (BIST) sequence 8, STCU2 executes the following MBISTs in the order shown:

Phase	MBISTs executed
0	11, 24, 29, 34 42, 43, 51, 52

Table continues on the next page...

Phase	MBISTs executed
1	17, 21, 25, 30, 35, 36, 46, 53, 62
2	7, 10, 19, 26, 31, 38, 40, 45, 50
3	4, 9, 12, 14, 16, 27, 32, 48, 56
4	5, 8, 15, 20, 28, 37, 41, 47, 55
5	6, 13, 18, 22, 23, 33, 39, 44, 49
6	0, 1, 2, 3

6.9.2 LBISTs executed

For online built-in self-test (BIST) sequence 8, STCU2 executes the following LBISTs in the order shown with the indicated coverage:

Phase	LBISTs executed	Coverage, stuck-at (%)
7	6	90
	23	90
8	7	90
	25	90
9	3	80
	5	80
10	2	80
	4	80
11	10	80
	12	80
12	11	80
	13	80
13	9	80
	17	80
14	15	80
	22	80
15	8	80
	16	80
	21	90
16	0	80
	1	80
	14	80

6.10 Online BIST sequence 9 configuration

6.10.1 MBISTs executed

For online built-in self-test (BIST) sequence 9, STCU2 executes the following MBISTs in the order shown:

Phase	MBISTs executed
0	11, 24 , 29, 34, 42, 43, 51, 52, 57, 66, 72, 77
1	17, 21, 25, 30, 35, 36, 46, 53, 58, 61, 62, 63, 70
2	7, 10, 19, 26, 31, 38, 40, 45, 50, 54, 59, 68, 74
3	4, 9, 12, 14, 16, 27, 32, 48, 56, 60, 69, 75
4	5, 8, 15, 20, 28, 37, 41, 47, 55, 65, 71, 76
5	6, 13, 18, 22, 23, 33, 39, 44, 49, 64, 67, 73
6	0, 1, 2, 3

6.10.2 LBISTs executed

For online built-in self-test (BIST) sequence 9, STCU2 executes the following LBISTs in the order shown with the indicated coverage:

Phase	LBISTs executed	Coverage, stuck-at (%)
7	6	90
	23	90
	24	90
8	7	90
	25	90
	26	90
9	12	90
10	13	90
11	9	90
	17	90
12	15	90
	22	90
13	8	90
	16	90
	21	90
14	0	90
	1	90
	14	90

7 Release notes for revision 3

General change throughout the document • Updated the docuemnt footer to remove "Preliminary" and "Confidential Proprietary".
Clocking requirement • For proper BIST sequence execution, the PLL clock shall use FXOSC_CLK.
Specifications • In the table footnote 1, corrected the table numbers in the S32V234 Reference Manual, Rev3.

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Document Number S32V234RMAD
Revision 3, 04/2018