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CMOS 2-WIRED SERIAL EEPROM S-24C01B/02B/04B

The S-24C01B/02B/04B are series of 2-wired, low power 1K/2K/4K-bit EEPROMs with a wide operating range. They are organized as 128-word×8-bit, 256-word×8-bit, and 512-word×8-bit, respectively. Each is capable of page write, and sequential read.

■ Features

- Low power consumption
  Standby: 1.0 µA Max. (V_{CC}=5.5 V)
  Operating: 0.8 mA Max. (V_{CC}=5.5 V)
  0.3 mA Max. (V_{CC}=3.3 V)
- Wide operating voltage range
  2.0 to 5.5 V
- Page write
  8 bytes (S-24C01B, S-24C02B)
  16 bytes (S-24C04B)
- Sequential read capable
- 400KHz (V_{CC}=5V±10%)
- Endurance: 10^6 cycles/word
- Data retention: 10 years
- Write protection: S-24C01B : 100%
  S-24C02B/04B : 50%
- S-24C01B: 1 Kbits
- S-24C02B: 2 Kbits
- S-24C04B: 4 Kbits

■ Pin Assignment

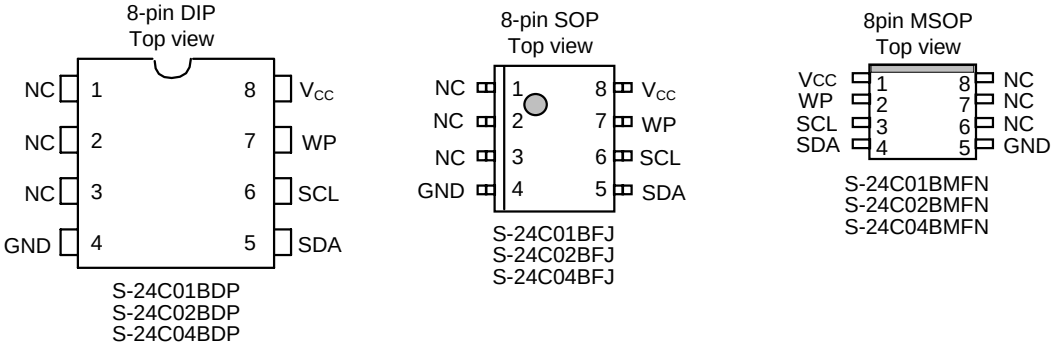

Figure 1

■ Pin Functions

Table 1

Name	Pin Number		Function
	DIP, SOP	MSOP	
NC	1	8	No Connection*
NC	2	7	No Connection*
NC	3	6	No Connection*
GND	4	5	Ground
SDA	5	4	Serial data input/output
SCL	6	3	Serial clock input
WP	7	2	Write Protection pin Connected to Vcc: Protection valid Connected to GND: Protection invalid
V_{CC}	8	1	Power supply

* This pin must be connected to either Vcc or GND.

■ Block Diagram

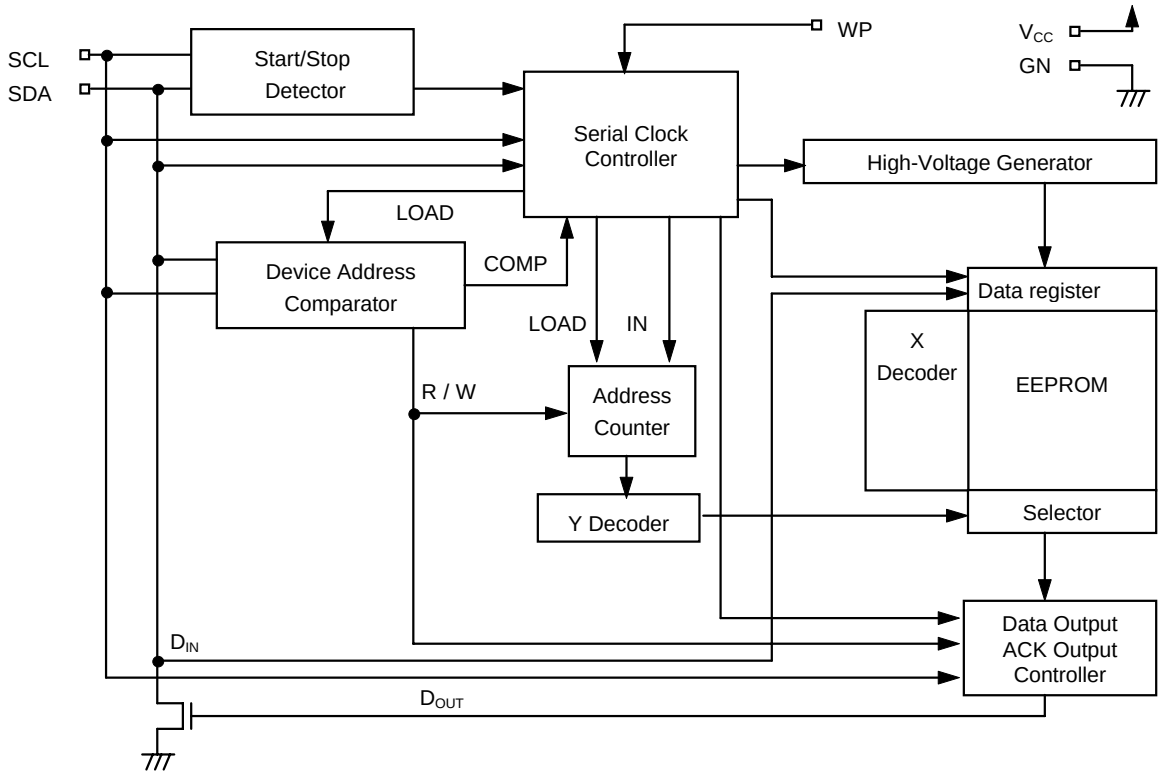

Figure 2

■ Absolute Maximum Ratings

Table 2

Parameter	Symbol	Ratings	Unit
Power supply voltage	V_{CC}	-0.3 to +7.0	V
Input voltage	V_{IN}	-0.3 to V_{CC}+0.3	V
Output voltage	V_{OUT}	-0.3 to V_{CC}	V
Storage temperature under bias	T_{bias}	-50 to +95	°C
Storage temperature	T_{stg}	-65 to +150	°C

■ Recommended Operating Conditions

Table 3

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltage	VCC	Read Operation	2.0	--	5.5	V
High level input voltage	V_{IH}	V_{CC}=2.5 to 5.5V	0.7×V_{CC}	--	V_{CC}	V
		V_{CC}=2.0 to 2.5V	0.8×V_{CC}	--	V_{CC}	V
Low level input voltage	V_{IL}	V_{CC}=2.5 to 5.5V	0.0	--	0.3×V_{CC}	V
		V_{CC}=2.0 to 2.5V	0.0	--	0.2×V_{CC}	V
Operating temperature	T_{opr}	--	-40	--	+85	°C

■ Pin Capacitance

Table 4

(Ta=25 °C, f=1.0 MHz, V_{CC}=5 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}	V_{IN}=0 V (SCL, WP)	--	--	10	pF
Input/output capacitance	$C_{I/O}$	$V_{I/O}$=0 V (SDA)	--	--	10	pF

■ Endurance

Table 5

Parameter	Symbol	Min.	Typ.	Max.	Unit
Endurance	N_W	10^6	--	--	cycles/word

■ DC Electrical Characteristics

Table 6

Parameter	Symbol	Conditions	VCC=4.5 to 5.5 V			V_{CC}=2.5 to 4.5 V			V_{CC}=2.0 to 2.5 V			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Current consumption (READ)	I_{CC1}	f=100 kHz	--	--	0.8*	--	--	0.3	--	--	0.2	mA
Current consumption (PROGRAM)	I_{CC2}	f=100 kHz	--	--	4.0	--	--	1.5	--	--	1.5	mA

* f = 400KHz

Table 7

Parameter	Symbol	Conditions	V_{CC}=4.5 V to 5.5 V			V_{CC}=2.5 to 4.5 V			V_{CC}=2.0 to 2.5 V			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Standby current consumption	I_{SB}	V_{IN}=V_{CC} or GND	--	--	1.0	--	--	0.6	--	--	0.4	mA
Input leakage current	I_{LI}	V_{IN}=GND to V_{CC}	--	0.1	1.0	--	0.1	1.0	--	0.1	1.0	mA
Output leakage current	I_{LO}	V_{OUT}=GND to V_{CC}	--	0.1	1.0	--	0.1	1.0	--	0.1	1.0	mA
Low level output voltage	V_{OL}	I_{OL}=3.2 mA	--	--	0.4	--	--	0.4	--	--	--	V
		I_{OL}=1.5 mA	--	--	0.3	--	--	0.3	--	--	0.5	V
Current address retention voltage	V_{AH}	--	1.5	--	5.5	1.5	--	4.5	1.5	--	2.5	V

■ AC Electrical Characteristics

Table 8 Measurement Conditions

Input pulse voltage	$0.1\times V_{CC}$ to $0.9\times V_{CC}$
Input pulse rising/falling time	20 ns
Output judgment voltage	$0.5\times V_{CC}$
Output load	100 pF+ Pullup resistance 1.0 KΩ¶

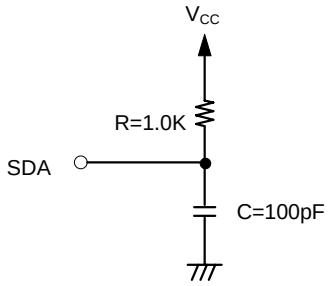

Figure 3 Output Load Circuit

Table 9

Parameter	Symbol	V_{CC}=4.5V to 5.5V			V_{CC}=2.0V to 4.5V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	0	--	400	0	--	100	KHz
SCL clock time "L"	t_{LOW}	1.0	--	--	4.7	--	--	µs
SCL clock time "H"	t_{HIGH}	0.9	--	--	4.0	--	--	µs
SDA output delay time	t_{AA}	0.1	--	0.9	0.1	--	3.5	µs
SDA output hold time	t_{DH}	50	--	--	100	--	--	ns
Start condition setup time	$t_{SU.STA}$	0.6	--	--	4.7	--	--	µs
Start condition hold time	$t_{HD.STA}$	0.6	--	--	4.0	--	--	µs
Data input setup time	$t_{SU.DAT}$	100	--	--	200	--	--	ns
Data input hold time	$t_{HD.DAT}$	0	--	--	0	--	--	ns
Stop condition setup time	$t_{SU.STO}$	0.6	--	--	4.7	--	--	µs
SCL • SDA rising time	t_R	--	--	0.3	--	--	1.0	µs
SCL • SDA falling time	t_F	--	--	0.3	--	--	0.3	µs
Bus release time	t_{BUF}	1.3	--	--	4.7	--	--	µs
Noise suppression time	t_I	--	--	50	--	--	100	ns

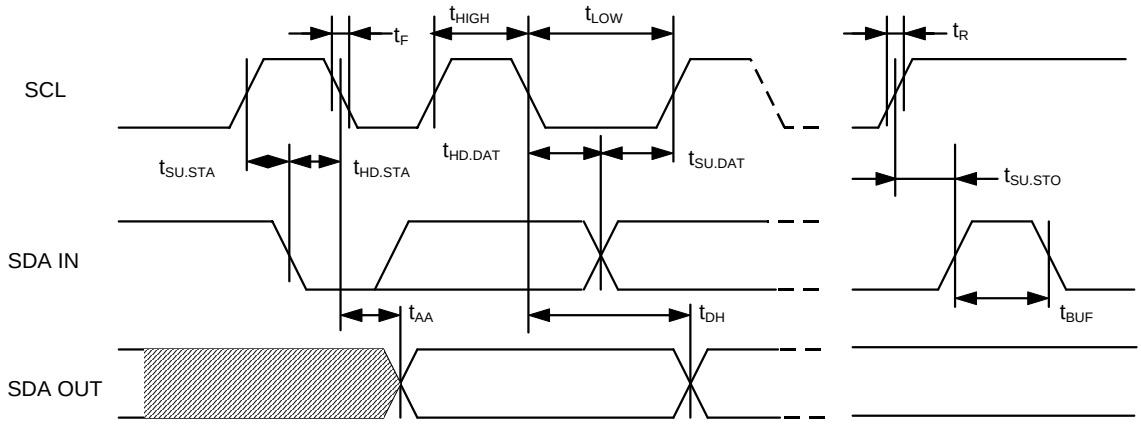

Figure 4 Bus Timing

Table 10

Item	Symbol	Min.	Typ.	Max.	Unit
Write time	t_{WR}	--	4.0	10.0	ms

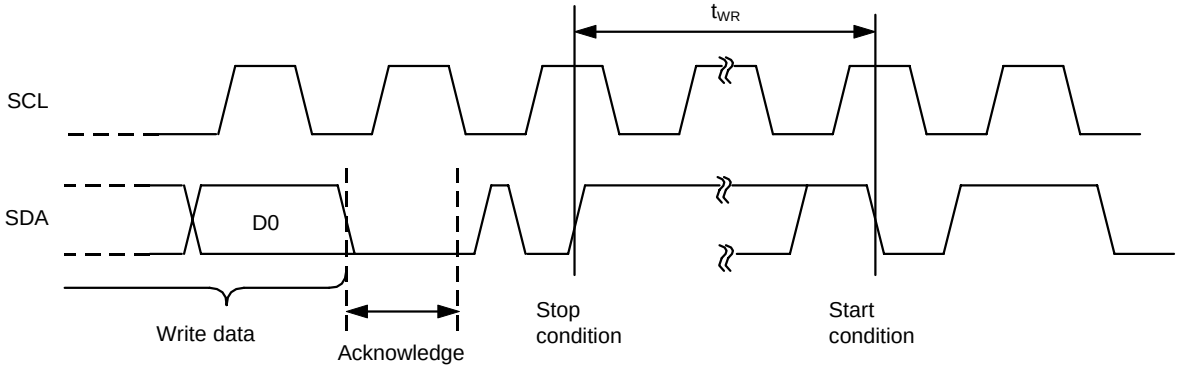

Figure 5 Write Cycle

■ Pin Functions

1. SDA (Serial Data Input/Output) Pin

The SDA pin is used for bilateral transmission of serial data. It consists of a signal input pin and an Nch open-drain transistor output pin.
Usually pull up the SDA line via resistance to the V_{CC}, and use it with other open-drain or open-collector output devices connected in a wired OR configuration.

2. SCL (Serial Clock Input) Pin

The SCL pin is used for serial clock input. It is capable of processing signals at the rising and falling edges of the SCL clock input signal. Make sure the rising time and falling time conform to the specifications.

3. WP Pin

The WP pin is used for write protection. When there is no need for write protection, connect the pin to the GND; when there is a need for write protection, connect the pin to the Vcc.

■ Operation

1. Start Condition

When the SCL line is “H” the SDA line changes from “H” to “L”. This allows the device to go to the start condition.

All operations begin from the start condition.

2. Stop Condition

When the SCL line is “H” the SDA line changes from “L” to “H”. This allows the device to go to the stop condition.

When the device receives the stop condition signal during a read sequence, the read operation is interrupted, and the device goes to standby mode.

When the device receives the stop condition signal during write sequence, the retrieval of write data is halted, and the EEPROM initiates rewrite.

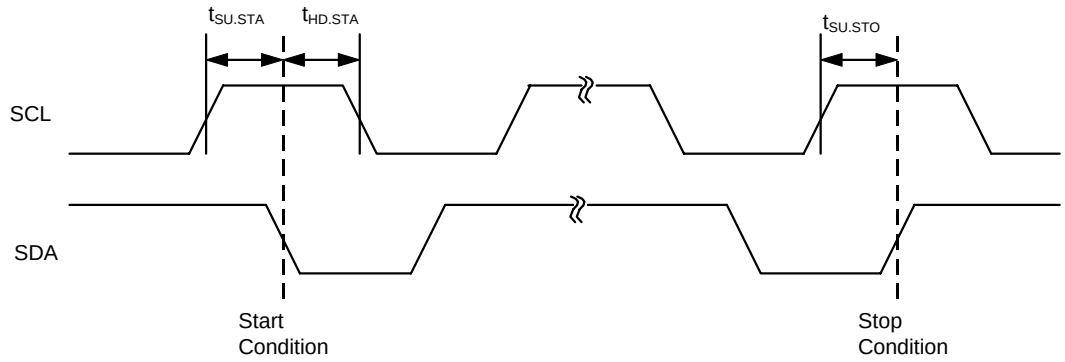

Figure 6 Start/Stop Conditions

3. Data Transmission

Changing the SDA line while the SCL line is “L” allows the data to be transmitted. A start or stop condition is recognized when the SDA line changes while the SCL line is “H”.

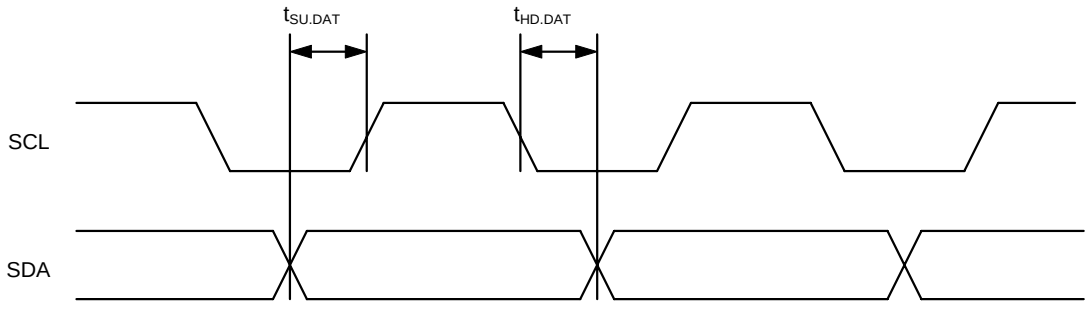

Figure 7 Data Transmission Timing

4. Acknowledgment

The unit of data transmission is 8 bits. By turning the SDA line "L" the slave device mounted on the system bus which receives the data during the 9th clock cycle outputs the acknowledgment signal verifying the data reception.

When the EEPROM is rewriting, the device does not output the acknowledgment signal.

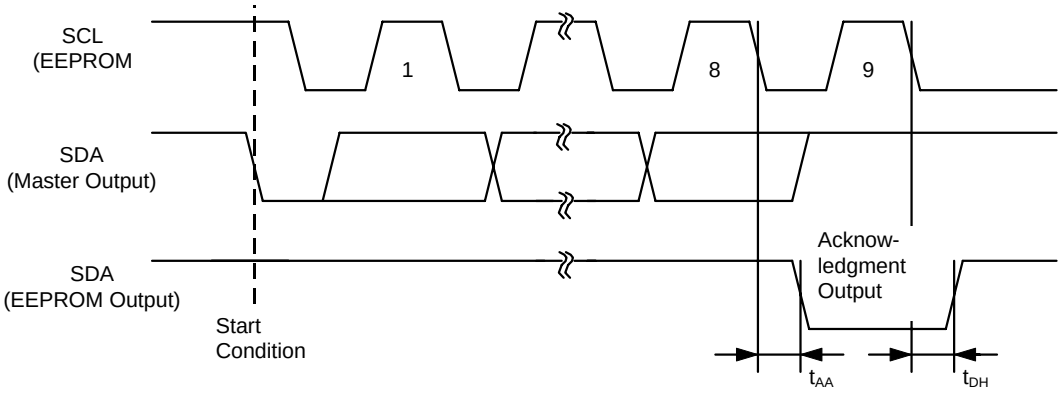

Figure 8 Acknowledgment Output Timing

5. Device Addressing

To perform data communications, the master device mounted on the system outputs the start condition signal to the slave device. Next, the master device outputs 7-bit length device address and a 1-bit length read/write instruction code onto the SDA bus.

Upper 4 bits of the device address are called the "Device Code", and set to "1010". Successive 3 bits are "don't care" bits.

When the comparison results match, the slave device outputs the acknowledgment signal during the 9th clock cycle.

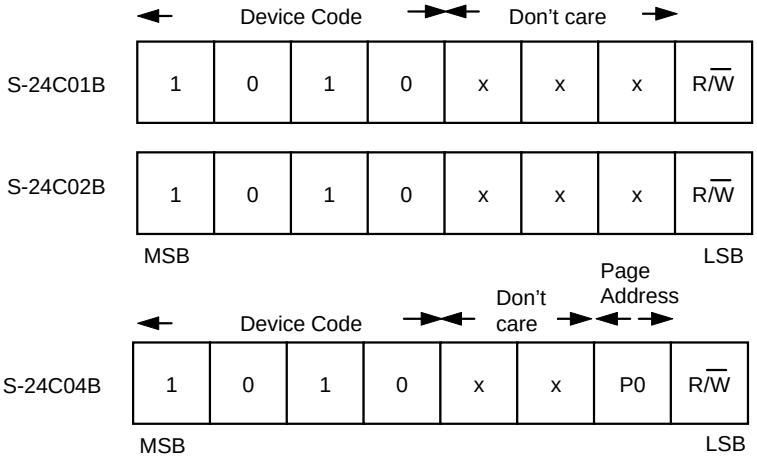

Figure 9 Device Address

In the S-24C04A, 7th bit becomes "P0". "P0" is a page address bit and is equivalent to an additional uppermost bit of the word address. Accordingly, when P0="0", the former half area corresponding to 2 kbits (addresses from 000h to 0FFh) in the entire memory are selected; when P0="1", the latter half area corresponding to 2 kbits (addresses from 100h to 1FFh) in all areas of the memory are selected.

6. Write

6.1 Byte Write

When the EEPROM receives a 7-bit length device address and a 1-bit read/write instruction code “0”, following the start condition signal, it outputs the acknowledgment signal. Next, when the EEPROM receives an 8-bit length word address, it outputs the acknowledgment signal.
After the EEPROM receives 8-bit write data and outputs the acknowledgment signal, it receives the stop condition signal. Next, the EEPROM at the specified memory address starts to rewrite.

When the EEPROM is rewriting, all operations are prohibited and the acknowledgment signal is not output.

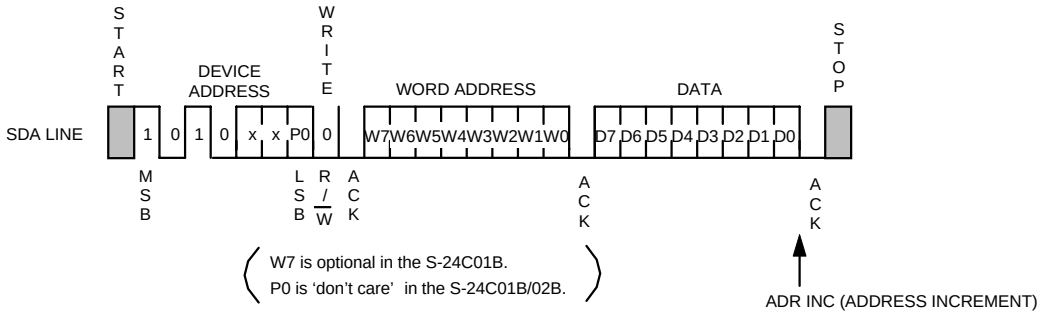

Figure 10 Byte Write

6.2 Page Write

Up to 8 bytes per page can be written in the S-24C01B and S-24C02B.
Up to 16 bytes per page can be written in the S-24C04B.

Basic data transmission procedures are the same as those in the “Byte Write”. However, when the EEPROM receives 8-bit write data which corresponds to the page size, the page can be written.

When the EEPROM receives a 7-bit length device address and a 1-bit read/write instruction code “0”, following the start condition signal, it outputs the acknowledgment signal. When the EEPROM receives an 8-bit length word address, it outputs the acknowledgment signal.

After the EEPROM receives 8-bit write data and outputs the acknowledgment signal, it receives 8-bit write data corresponding to the next word address, and outputs the acknowledgment signal. The EEPROM repeats reception of 8-bit write data and output of the acknowledgment signal in succession. It is capable of receiving write data corresponding to the maximum page size.

When the EEPROM receives the stop condition signal, it starts to rewrite, corresponding to the size of the page, on which write data, starting from the specified memory address, is received.

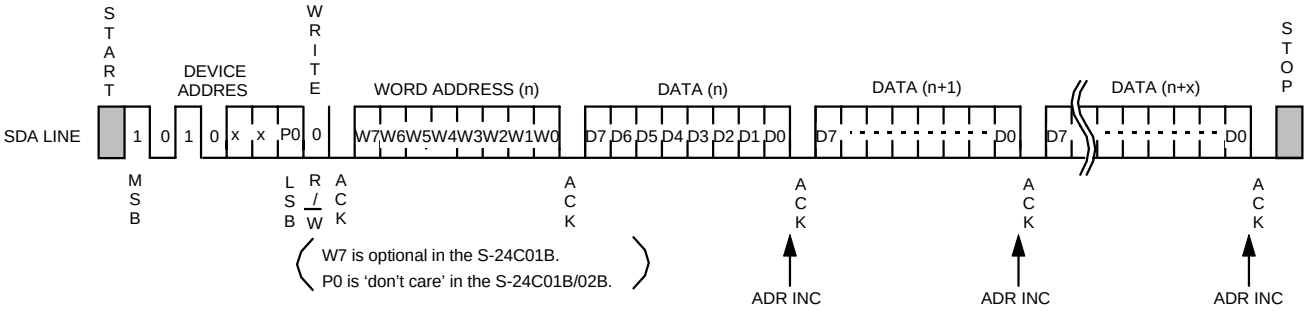

Figure 11 Page Write

In the S-24C01B or S-24C02B, the lower 3 bits of the word address are automatically incremented each when the EEPROM receives 8-bit write data.
Even if the write data exceeds 8 bytes, the upper 5 bits at the word address remain unchanged, the lower 3 bits are rolled over and overwritten.

In the S-24C04B, the lower 4 bits at the word address are automatically incremented each when the EEPROM receives 8 bit write data.
Even when the write data exceeds 16 bytes, the upper 4 bits of the word address and page address P0 remain unchanged, and the lower 4 bits are rolled over and overwritten.

6.3 Acknowledgment Polling

Acknowledgment polling is used to know when the rewriting of the EEPROM is finished.
After the EEPROM receives the stop condition signal and once it starts to rewrite, all operations are prohibited. Also, the EEPROM cannot respond to the signal transmitted by the master device.
Accordingly, the master device transmits the start condition signal and the device address read/write instruction code to the EEPROM (namely, the slave device) to detect the response of the slave device. This allows users to know when the rewriting of the EEPROM is finished.

That is, if the slave device does not output the acknowledgment signal, it means that the EEPROM is rewriting; when the slave device outputs the acknowledgment signal, you can know that rewriting has been completed. It is recommended to use read instruction "1" for the read/write instruction code transmitted by the master device.

6.4 Write Protection

The S-24C01B/02B/04B are capable of protecting the memory. When the WP pin is connected to V_{CC}, writing to all memory area is prohibite in the S-24C01B, writing to 50% of the latter half of memory area is prohibited in the S-24C02B and S-24C04B. (prohibited adress are 080h to 0FFh in the S-24C02B; 100h to 1FFh in the S-24C04B) Even when writing is prohibited, since the controller inside the IC is operating, the response to the signal transmitted by the master device is not available during the time of writing (t_{WR}).

When the WP pin is connected to GND, the write protection becomes invalid, and writing in all memory area becomes available. However, when there is no need for using write protection, always connect the WP pin to GND.

7. Read

7.1 Current Address Read

The EEPROM is capable of storing the last accessed memory address during both writing and reading. The memory address is stored as long as the power voltage is more than the retention voltage V_{AH}.

Accordingly, when the master device recognizes the position of the address pointer inside the EEPROM, data can be read from the memory address of the current address pointer without assigning a word address. This is called “Current Address Read”.

“Current Address Read” is explained for when the address counter inside the EEPROM is an “n” address.

When the EEPROM receives a 7-bit length device address and a 1-bit read/write instruction code “1”, following the start condition signal, it outputs the acknowledgment signal. However, in the S-24C04B, page address P0 becomes invalid, and the memory address of the current address pointer becomes valid.
Next, 8-bit length data at an “n” address is output from the EEPROM, in synchronization with the SCL clock. The address counter is incremented at the falling edge of the SCL clock by which the 8th bit of data is output, and the address counter goes to address n+1.

The master device does not output the acknowledgment signal and transmits the stop condition signal to finish reading.

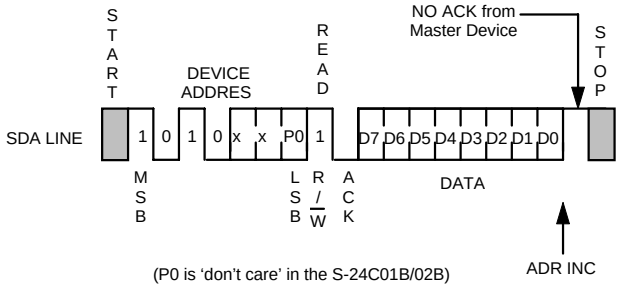

Figure 12 Current Address Read

For recognition of the address pointer inside the EEPROM, take into consideration the following:
The memory address counter inside the EEPROM is automatically incremented for every falling edge of the SCL clock by which the 8th bit of data is output during the time of reading. During the time of writing, upper bits of the memory address (upper 5 bits of the word address in the S-24C01B and S-24C02B; upper 4 bits of the word address and page address P0 in the S-24C04B) are left unchanged and are not incremented.

7.2 Random Read

Random read is a mode used when the data is read from arbitrary memory addresses.
To load a memory address into the address counter inside the EEPROM, first perform a dummy write according to the following procedures:

When the EEPROM receives a 7-bit length device address and a 1-bit read/write instruction code “0”, following the start condition signal, it outputs the acknowledgment signal.
Next, the EEPROM receives an 8-bit length word address and outputs the acknowledgment signal. Last, the memory address is loaded into the address counter of the EEPROM.
the EEPROM receives the write data during byte or page writing. However, data reception is not performed during dummy write.

The memory address is loaded into the memory address counter inside the EEPROM during dummy write. After that, the master device can read the data starting from the arbitrary memory address by transmitting a new start condition signal and performing the same operation as that in the “Current Read”.

That is, when the EEPROM receives a 7-bit length device address and a 1-bit read/write instruction code “1”, following the start condition signal, it outputs the acknowledgment signal.
Next, 8-bit length data is output from the EEPROM, in synchronization with the SCL clock. The master device does not output an acknowledgment signal and transmits the stop condition signal to finish reading.

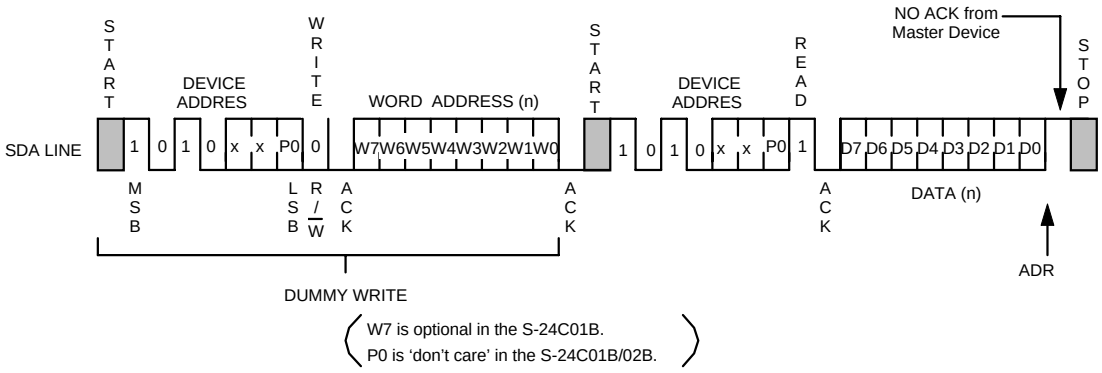

Figure 13 Random Read

7.3 Sequential Read

When the EEPROM receives a 7-bit length device address and a 1-bit read/write instruction code “1” in both current and random read operations, following the start condition signal, it outputs the acknowledgment signal.

When 8-bit length data is output from the EEPROM, in synchronization with the SCL clock, the memory address counter inside the EEPROM is automatically incremented at the falling edge of the SCL clock, by which the 8th data is output.
When the master device transmits the acknowledgment signal, the next memory address data is output.

When the master device transmits the acknowledgment signal, the memory address counter inside the EEPROM is incremented and read data in succession. This is called “Sequential Read”.

When the master device does not output an acknowledgement signal and transmits the stop condition signal, the read operation is finished.

Data can be read in the “Sequential Read” mode in succession. When the memory address counter reaches the last word address, it rolls over to the first memory address.

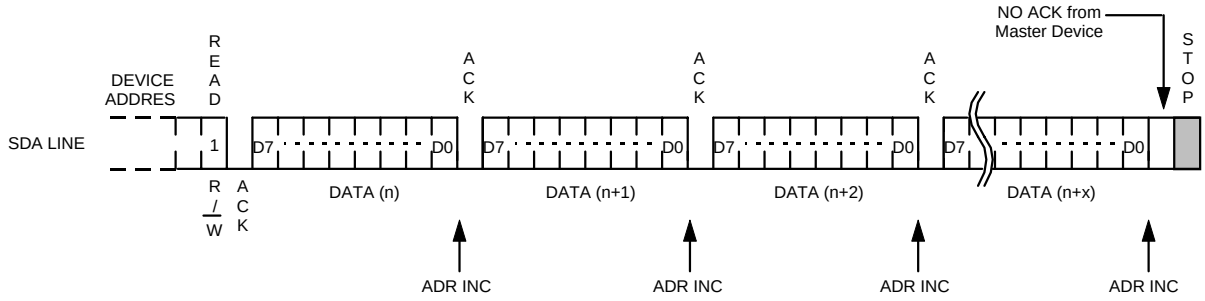

Figure 14 Sequential Read

8. Address Increment Timing

The address increment timing is as follows. See Figures 15 and 16. During reading operation, the memory address counter is automatically incremented at the falling edge of the SCL clock (the 8th read data is output).

During writing operation, the memory address counter is also automatically incremented at the falling edge of the SCL clock when the 8th bit write data is fetched.

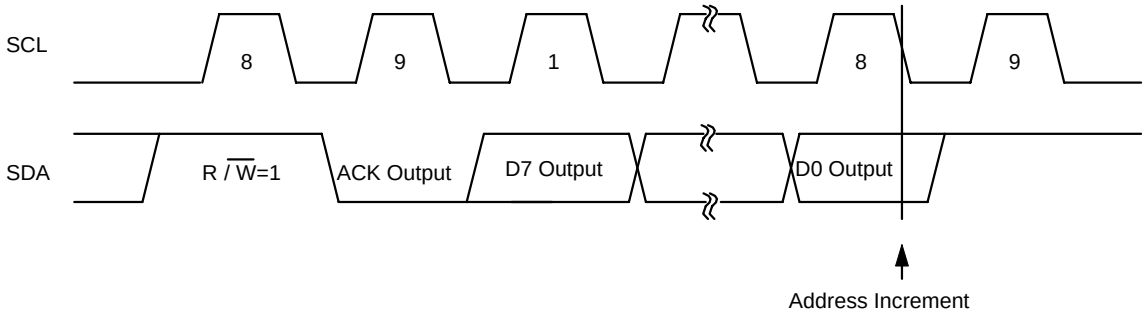

Figure 15 Address Increment Timing During Reading

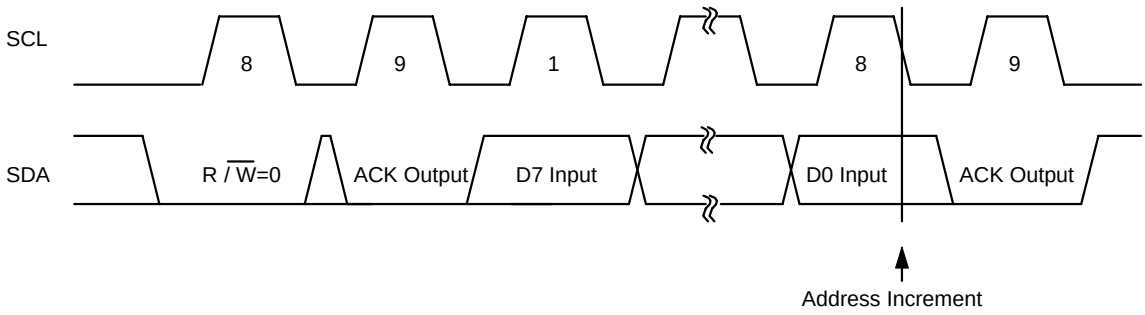

Figure 16 Address Increment Timing During Writing

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Please note that any product or system incorporating this IC may infringe upon the Philips I^2C Bus Patent Rights depending upon its configuration.

In the event that such product or system incorporating the I^2C Bus infringes upon the Philips Patent Rights, Seiko Instruments Inc. shall not bear any responsibility for any matters with regard to and arising from such patent infringement.

■ **Physical Dimensions** (Unit: mm)

1. 8-pin DIP

S-24C01BDP-1A
S-24C02BDP-1A
S-24C04BDP-1A

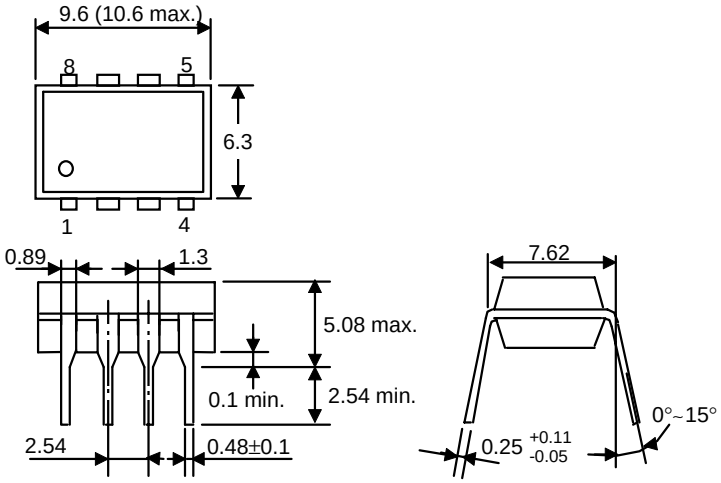
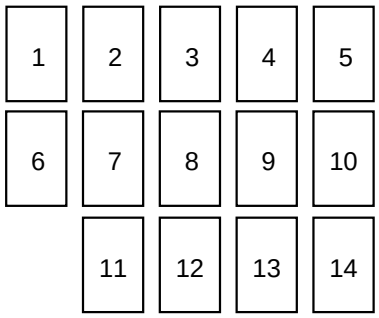


Figure 17

Markings



1 to 7	:	Product name	“S24C01B”
			“S24C02B”
			“S24C04B”
8	:	Assembly code	
9	:	Year of assembly (Last digit of the year)	
10	:	Month of assembly (1 to 9, X, Y, Z)	
11 to 14	:	Lot No.	

Figure 18

2. 8-pin SOP

S-24C01BFJ-TB
S-24C02BFJ-TB
S-24C04BFJ-TB

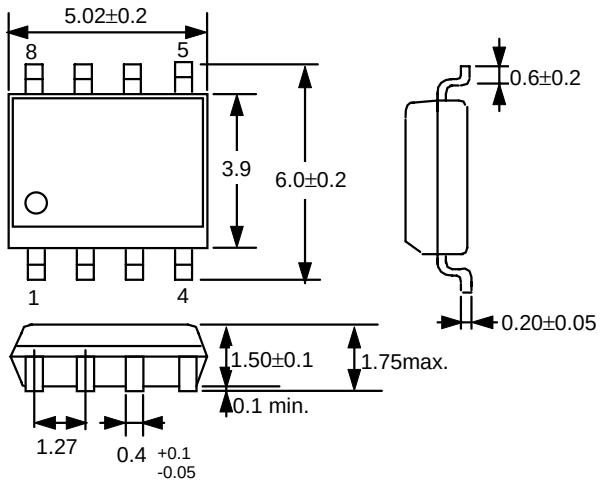
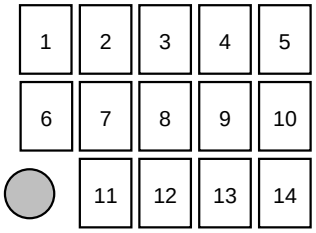


Figure 19

Markings



1 to 7	:	Product name “S24C01B” “S24C02B” “S24C04B”
8	:	Assembly code
9	:	Year of assembly (Last digit of the year)
10	:	Month of assembly (1 to 9, X, Y, Z)
11 to 14	:	Lot No.

Figure 20

3. 8-pin MSOP

S-24C01BMFN-TB
S-24C02BMFN-TB
S-24C04BMFN-TB

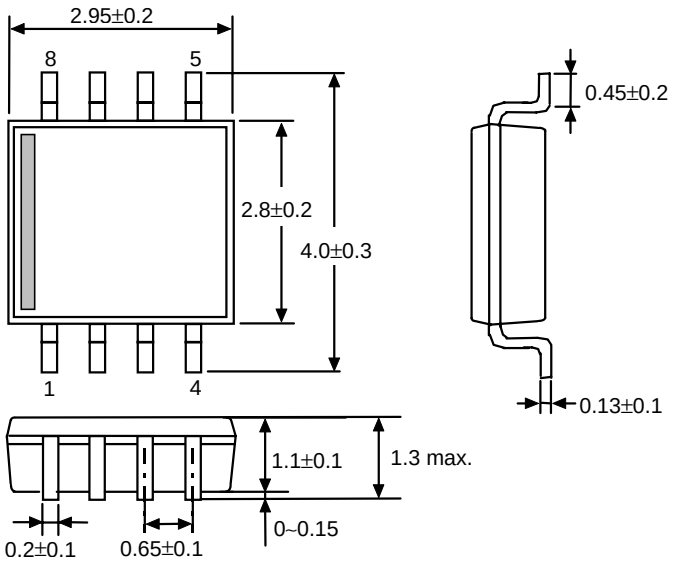
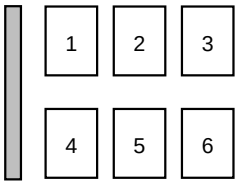


Figure 21

Markings



1 to 3 : Product name "01M" in the case of "S-24C01B"
"02M" in the case of "S-24C02B"
"04M" in the case of "S-24C04B"
4 : Year of assembly (Last digit of the year)
5 to 6 : Lot No.

Figure 22

■ Ordering Information

S-24C0XB XXX - YY

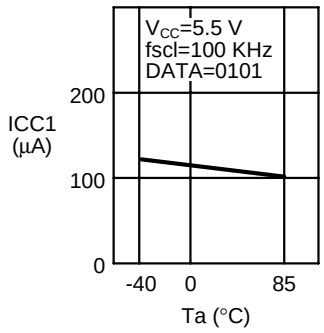
Package
- DP-1A : DIP
- FJ-TB : SOP Tape
- MFN-TB : MSOP Tape

Product name
- S-24C01B: 1K bits
- S-24C02B: 2K bits
- S-24C04B: 4K bits

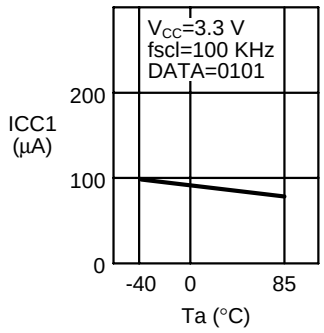
■ Characteristics

1. DC Characteristics

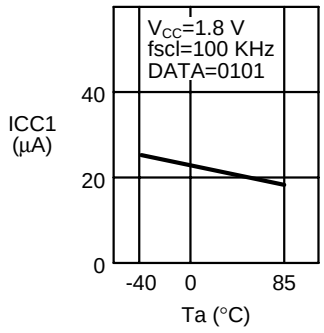
1.1 Current consumption (READ) I_{CC1} -- Ambient temperature Ta



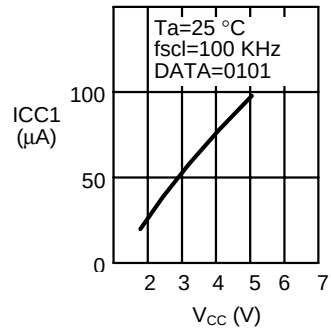
1.2 Current consumption (READ) I_{CC1} -- Ambient temperature Ta



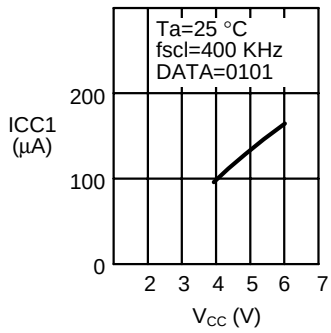
1.3 Current consumption (READ) I_{CC1} -- Ambient temperature Ta



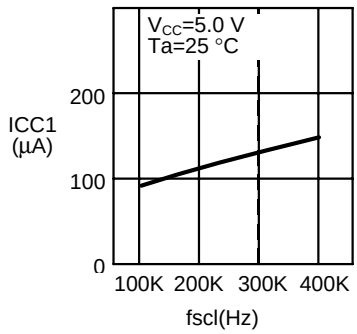
1.4 Current consumption (READ) I_{CC1} -- Power supply voltage V_{CC}



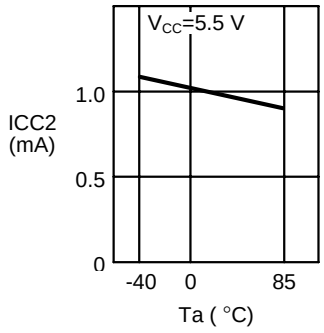
1.5 Current consumption (READ) I_{CC1} -- Power supply voltage V_{CC}



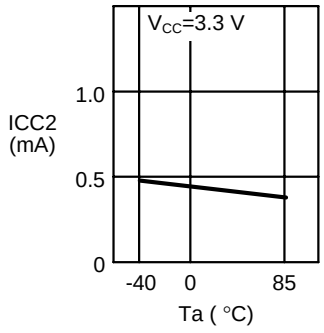
1.6 Current consumption (READ) I_{CC1} -- Clock frequency fscl



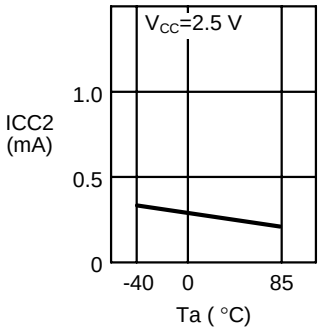
1.7 Current consumption (PROGRAM) I_{CC2} -- Ambient temperature Ta



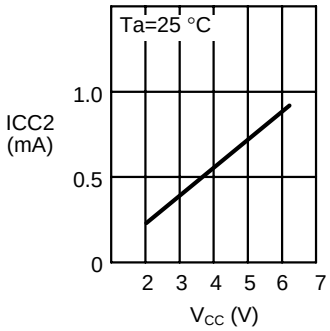
1.8 Current consumption (PROGRAM) I_{CC2} -- Ambient temperature Ta



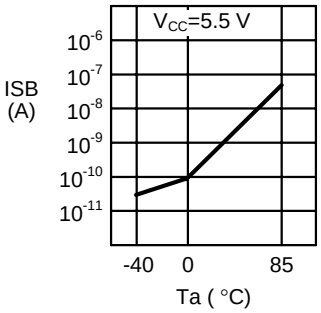
1.9 Current consumption (PROGRAM) I_{CC2} -- Ambient temperature Ta



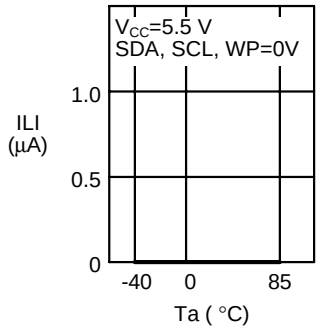
1.10 Current consumption (PROGRAM) I_{CC2} -- Power supply voltage V_{CC}



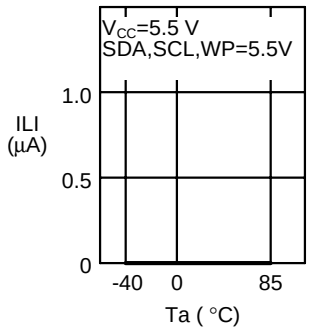
1.11 Standby current consumption I_{SB} -- Ambient temperature Ta



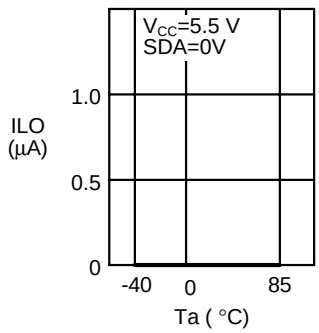
1.12 Input leakage current I_{LI} -- Ambient temperature Ta



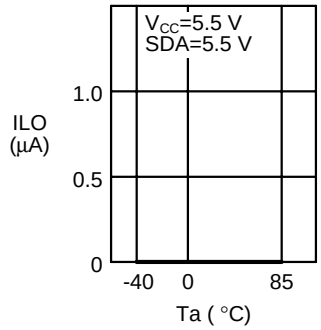
1.13 Input leakage current I_{LI} -- Ambient temperature Ta



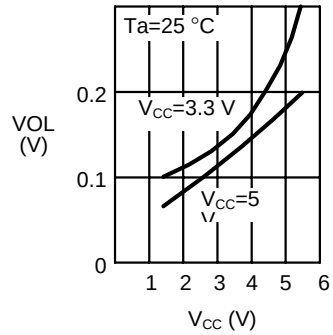
1.14 Output leakage current I_{LO} -- Ambient temperature Ta



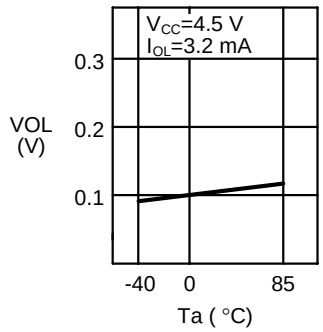
1.15 Output leakage current I_{LO} -- Ambient temperature Ta



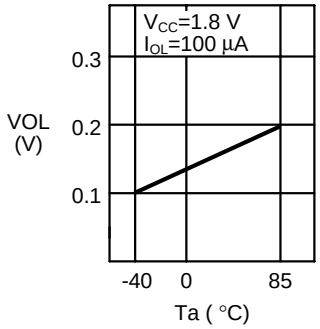
1.16 Low level output voltage V_{OL} -- Low level output current I_{OL}



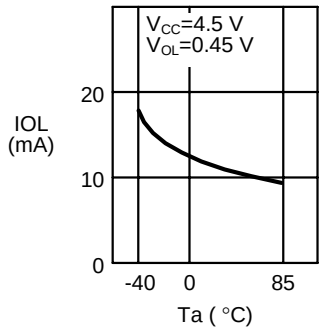
1.17 Low level output voltage V_{OL} -- Ambient temperature Ta



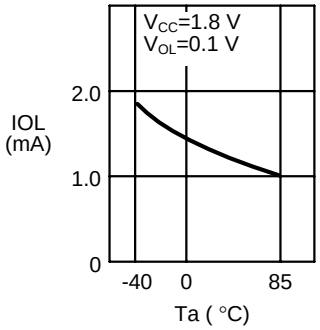
1.18 Low level output voltage V_{OL} -- Ambient temperature Ta



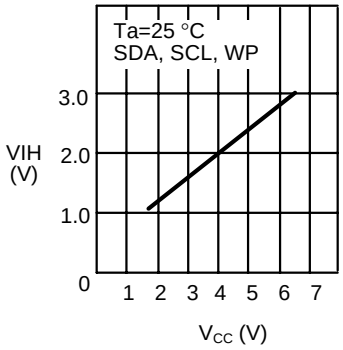
1.19 Low level output current I_{OL} -- Ambient temperature Ta



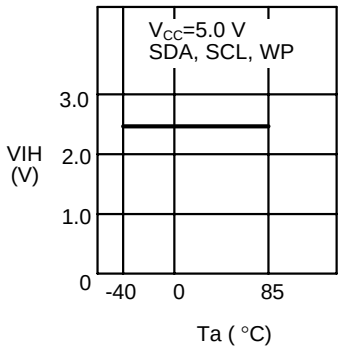
1.20 Low level output current I_{OL} -- Ambient temperature Ta



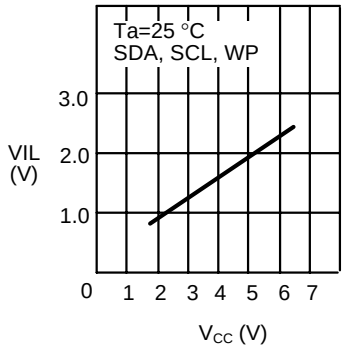
1.21 High input inversion voltage VIH -- Power supply voltageV_{CC}



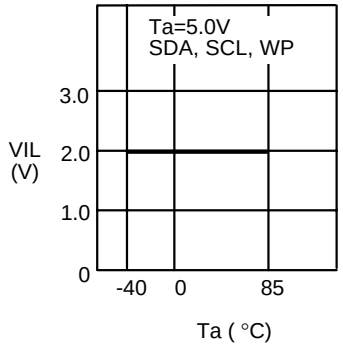
1.22 High input inversion voltage VIH -- Ambient temperature Ta



1.23 Low input inversion voltage VIL -- Power supply voltageV_{CC}

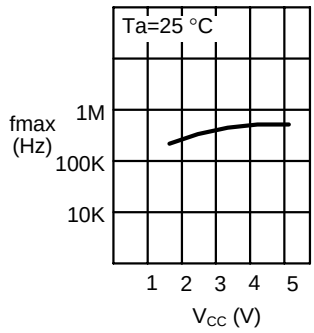


1.24 Low input inversion voltage VIL -- Ambient temperature Ta

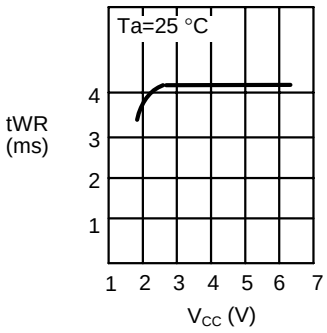


2. AC Characteristics

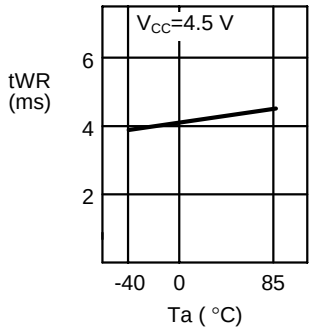
2.1 Maximum operating frequency fmax -- Power supply voltage V_{CC}



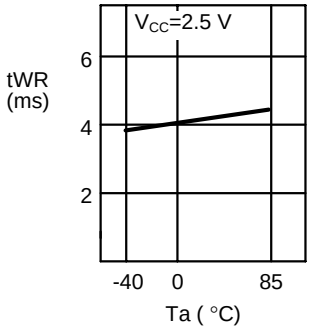
2.2 Write time t_{WR} -- Power supply voltage V_{CC}



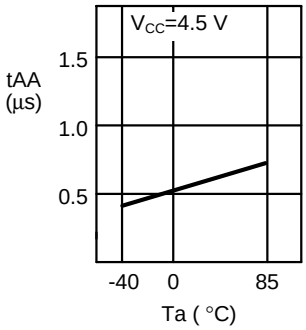
2.3 Write time t_{WR} -- Ambient temperature Ta



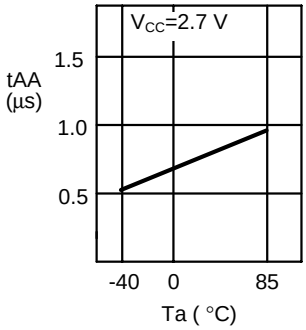
2.4 Write time t_{WR} -- Ambient temperature Ta



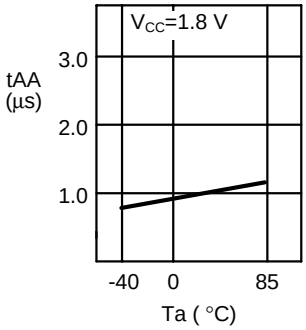
2.5 SDA output delay time t_{AA} -- Ambient temperature Ta



2.6 SDA output delay time t_{AA} -- Ambient temperature Ta



2.7 Data output delay time t_{AA} -- Ambient temperature Ta



Collection of Product FAQs

Author: Ebisawa Takashi Date: 99/01/13 (Wednesday), 17:27 (modified: 99/01/22 (Friday))

<Information level>

A: Public (Printing O.K.)

Index: B: Technical

<Product>

Division name: 01 IC

Category 1: 12 Memory

Category 2: 1.2 Wire Bus Serial EEPROM

Cal No.: Overall

Related documents:

Question:

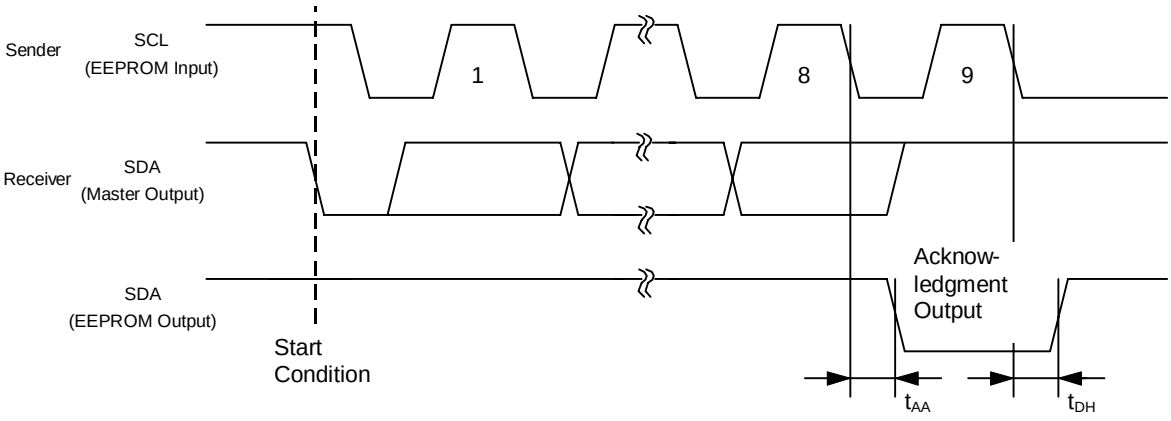
How important are acknowledgement (malfunction) checks?

Answer:

[Why acknowledgement is important]

The I2CBUS protocol includes an acknowledgement check function (for an outline of this function, see “FAQ Acknowledgement”) as a handshake function to prevent communication errors. This function can detect improper data communication between a microcomputer and EEPROM.

Due to the specifications of the software, some users may ignore this function and continue to execute a command. This, however, may result in a malfunction, miswriting, or hang-up. We recommend that acknowledgement checks be executed from the microcomputer.



<Remarks>

FAQ No.: 12020

Collection of Product FAQs

Author: Kano Tomoo Date: 98/11/12 (Thursday) 10:17 (modified: 99/01/22)

<Information level>

A: Public (Printing O.K.)

Index: B: Technical

<Product>

Division name: 01 IC

Category 1: 12 Memory

Category 2: 1.2 Wire Bus Serial EEPROM

Cal No.: Overall

Related documents:

Question:

What about the basic terms (acknowledgement.ack)?

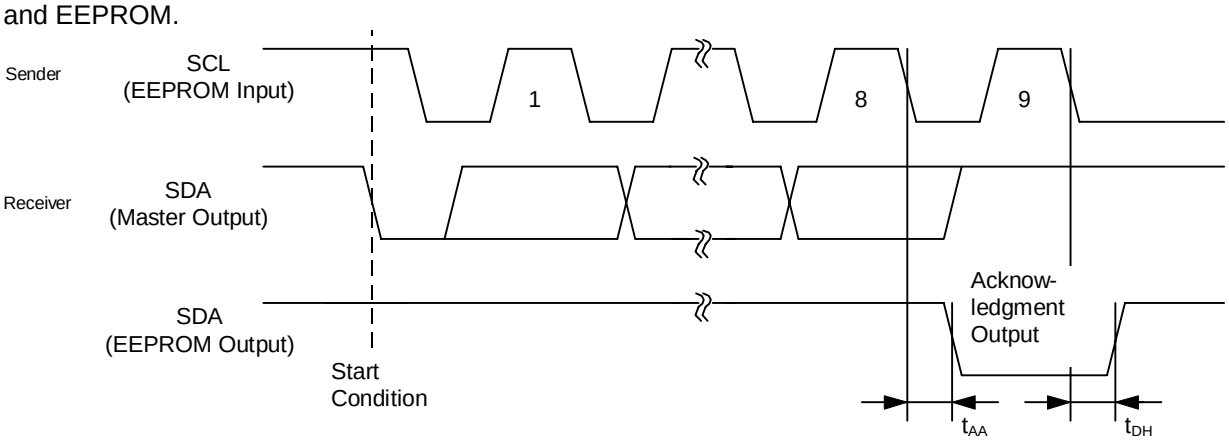
Answer:

Acknowledgement →S-24C series

If data from the sender is successfully transmitted, the receiver issues an output signal (L).

[Reason this signal is required]

The I2CBUS protocol includes an acknowledgement check function as a handshake function to prevent communication errors. This function can detect improper data communication between a microcomputer and EEPROM.



<Remarks>

FAQ No.: 12019

Collection of Product FAQs

Author: Ebisawa Takashi Date: 99/01/13 (Wednesday) 14:40 (modified: 99/01/13)

<Information level>

A: Public (Printing O.K.)

Index: B: Technical

<Product>

Division name: 01 IC

Category 1: 12 Memory

Category 2: 1.2 Wire Bus Serial EEPROM

Cal No.: Overall

Related documents:

Question:

Method for resetting the S-24 series, phase matching during access: malfunction

Answer:

Due to the lack of a reset terminal (for the internal circuit), the 24C-series EEPROM cannot be reset externally. Thus, if communication with the EEPROM is interrupted, action must be taken with the software. For example, even if a reset signal is input to the microcomputer, the internal circuit of the EEPROM is not reset unless a stop condition is input to the EEPROM. Therefore, the EEPROM holds its state, and cannot enter the next operation. This is particularly common in cases in which only the microcomputer is reset while the power voltage is decreasing. If the power voltage is recovered under these conditions, reset the EEPROM (match the phase between the EEPROM and microcomputer) and then input a command. This reset method is shown in.

<Remarks>

FAQ No.: 12010

Collection of Product FAQs

Author: Kano Tomoo Date: 98/11/12 (Thursday) 10:17 (modified: 99/01/22)

<Information level>

A: Public (Printing O.K.)

Index: B: Technical

<Product>

Division name: 01 IC

Category 1: 12 Memory

Category 2: 1.2 Wire Bus Serial EEPROM

Cal No.: Overall

Related documents:

Question:

Method for resetting the S-24 series, phase matching during access: malfunction

Answer:

Method for resetting the EEPROM

The EEPROM can be normally reset using start and stop commands. However, while the EEPROM is reading data '0' or outputting an acknowledgement signal, '0' is being output to the SDA line so the microcomputer cannot output a command to the SDA line. In such a case, end the acknowledgement-signal output operation or read operation of the EEPROM, and enter a start command.

Fig. 1 shows this procedure. First, enter a start condition. Then, send SCL for nine clocks (dummy clocks). During this operation, the microcomputer keeps the SDA line at a high level. The EEPROM then aborts the acknowledgement-signal output operation or data output, so enter a start condition. (*2) This resets the EEPROM. Then, input a stop condition to the EEPROM to ensure safety. Normal operations will then be enabled.

We recommend that this reset method using dummy clocks be executed following activation of the power voltage and during system initialization.

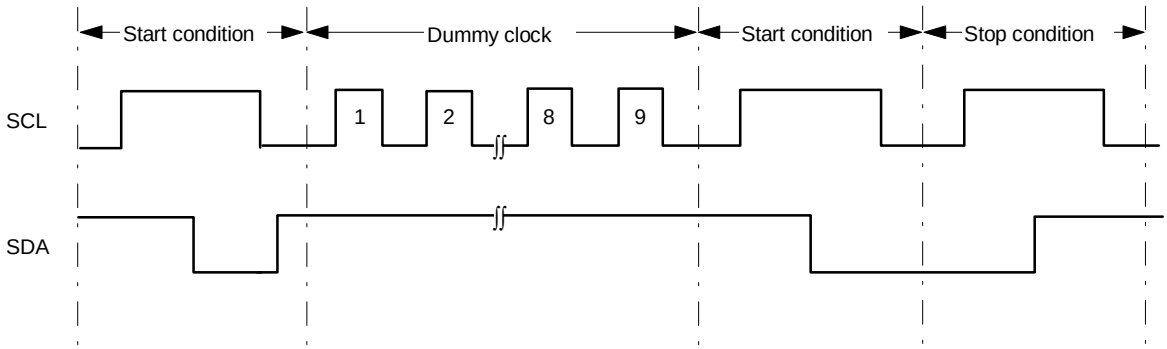


Fig. 7 EEPROM Resetting Method

(*2) If SCL clocks are continuously provided after the nine clocks (dummy clocks) without input of a start condition, a write operation may be started when a stop condition is received. To prevent this, input a start condition after the nine clocks (dummy clocks).

<Remarks>

FAQ No.: 12009

Collection of Product FAQs

Author: Ebisawa Takashi Date: 99/01/13 (Wednesday) 18:19 (modified: 99/01/14)

<Information level>

A: Public (Printing O.K.)

Index: C: quality, reliability

<Product>

Division name: 01 IC

Category 1: 12 Memory

Category 2: 2. Serial EEPROM

Cal No.: Overall

Related documents:

Question:

What about the reliability and quality of the EEPROM?

Answer:

1. The EEPROM must have a quality that is “special in a sense” and that differs from that of the other ICs.

   <What is this special quality?>

(1) Number of possible rewrites: 105 or 106

   A specified minimum number of data rewrites must be assured.

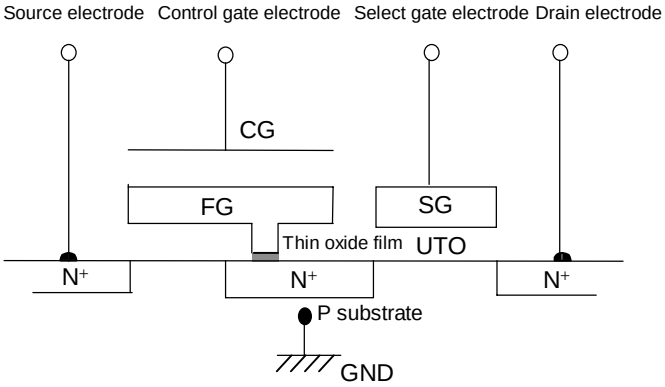
(2) Data retention: 10 years

   It must be ensured that written data (‘1’ and ‘0’) will be stored for at least 10 years.

Ensuring (1) and (2) is very difficult in a technical sense, as well as in the sense that high quality must be maintained despite the need for mass production.

2. Why this guarantee is technically difficult

   As shown in the figure below, the EEPROM functions as a non-volatile memory by holding charges in FG.



[Data rewrite]

Data rewrite refers to the injection or removal of electrons into or from the FG. In this process, electrons pass through a thin oxide film (UTO). The oxide film inherently acts as an insulator, but in this case the film conducts electricity (electrons are transferred).

[Data retention]

Data retention refers to the prevention of leakage of electrons stored in the FG. This must be assured for at least 10 years.

To meet the above stated contradictory properties, high-quality thin oxide films (UTO) must be manufactured. Such UTOs are very thin (on the order of 10 nm), and stably manufacturing them requires a very difficult technique.

<Remarks>

FAQ No.: 12022

Collection of Product FAQs

Author: Ebisawa Takashi Date: 99/01/13 (Wednesday) 18:57 (modified: 99/01/13)

<Information level>

X: Working

Index: A: General

<Product>

Division name: 01 IC

Category 1: 12 Memory

Category 2: 2. Serial EEPROM

Cal. No.: Overall

Related documents:

Question:

What about the distribution of application notes, usage notes, and malfunctions?

Answer:

Distribution of application notes

All EEPROMS, including ours, may malfunction (false-writes may occur) due to an “operation in a low-voltage region upon power-on/off” or “improper recognition of a command due to a noise signal.” This defect is particularly common in the voltage region of the microcomputer transmitting commands to the EEPROM, where the voltage is lower than the lowest operating voltage of the microcomputer.

To prevent this defect, usage notes have been prepared for the EEPROM.

- S-93C series, S29 series
- S-24CxxA series
- S-24CxxB series

<Remarks>

FAQ No.: 12022

Collection of Product FAQs

Author: Ebisawa Takashi Date: 99/01/13 (Wednesday) 17:43 (modified: 99/01/13)

<Information level>

A: Public (Printing O.K.)

Index: A: General

<Product>

Division name: 01 IC

Category 1: 12 Memory

Category 2: 2. Serial EEPROM

Cal. No.: Overall

Related documents:

Question:

What are some applications of the serial EEPROM?

Answer:

1. Applications of the EEPROM

   The applications of the EEPROM can be roughly divided into the following types:

- Tuning memory, mode setting, ID codes: Arbitrary data can easily be rewritten and data can be retained during power-off.
- Replacement of a DIP switch (from a mechanical to an electronic switch): User costs are substantially reduced.
- Adjustment data for IC elements and other electronics: The accuracy of final products is increased. Adjustments, which had been performed manually, can be automated.

2. Specific examples of applications

   Based on the above applications, general examples are shown below. Basically, the EEPROM (a non-volatile memory) is useful for electronic applications.

   [Television] TV channel memory, screen setting data, data backup during power-off
   S-24C series

   [Video] VTR channel memory, program reservation data, image-quality adjustment data, data backup during power-off
   S-93Cx6A, S-29xx0A, S-24C series

   [White goods] Maintenance data, adjustment data
   S-93Cx6A, S-29xx0A, S-24C series

   [Vehicle-mounted] Troubleshooting data, maintenance data, adjustment data: Air bags, ABS, distance meters
   S-93Cx6A, S-29xx0A, S-24C series

   [Printers] Printer maintenance data
   S-93Cx6A, S-29xx0A, S-24C series

[Modems] Replacement of DIP switches, software (firmware) data
S-93Cx6A, S-29xx0A, S-24C series

[Mobile telephones] Personal ID, telephone-number data, address data, adjustment data
S-24C series

[Pagers] Personal ID, telephone-number data, address data
S-93Cx6A, S-29Z series, S-24C series

[PC cards] LAN cards and modem cards, replacement of dip switches, software data
S-93C46A, S-29, S-24C series

<Remarks>

FAQ No.: 12021

Collection of Product FAQs

Author: Kano Tomoo Date: 98/11/12 (Thursday) 10:17 (modified: 99/01/13)

<Information level>

A: Public (Printing O.K.)

Index: D: Technical terms

<Product>

Division name: 01 IC

Category 1: 12 Memory

Category 2: 2. Serial EEPROM

Cal. No.: Overall

Related documents:

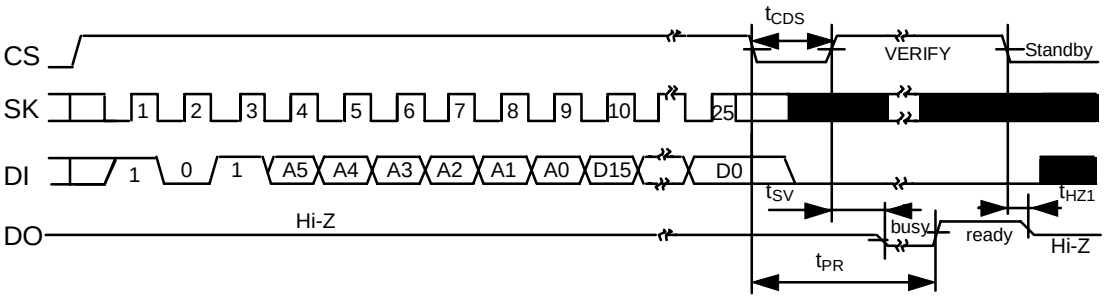
Question:

What about the basic terms (verify, ready/busy function)?

Answer:

Verify, ready/busy (R/B) function

This is a function to find out about an actual write operation (time). There are two methods, a “monitoring method based on the output condition of the DO pin” and a “method for monitoring the output condition of the Ready/Busy pin.” This function eliminates the need to wait 10 ms for writing to be completed, thereby minimizing the write time according to the performance of the IC (performance value: 4 ms to 5 ms; 1 ms is ensured for the S-24C series).



(Note) Note that this differs from a normal verify function, which checks written data for errors.

<Remarks>

FAQ No.: 12018

Collection of Product FAQs

Author: Kano Tomoo Date: 98/11/12 (Thursday) 10:17 (modified: 99/01/13)

<Information level>

A: Public (Printing O.K.)

Index: D: Technical terms

<Product>

Division name: 01 IC

Category 1: 12 Memory

Category 2: 2. Serial EEPROM

Cal. No.: Overall

Related documents:

Question:

What about the basic term (page write)?

Answer:

Page write S-24C series

Writing to memory is normally executed in addresses. With the page write function, however, writing can be executed in pages (multiple addresses). This function can improve the efficiency of write commands and reduce writing time.

Ex.:S-24C04B (4 K = 512 addresses x 8 bits) 16-byte page write function

Writing in addresses: A write time of 10 msec. x 512 = 5.1 sec. is required.

Page write: 10 msec. x 512 / 16 = 320 msec.

However, compatibility with products from other companies must be confirmed.

<Remarks>

FAQ No.: 12017

Collection of Product FAQs

Author: Kano Tomoo Date: 98/11/12 (Thursday) 10:17 (modified: 99/01/13)

<Information level>

A: Public (Printing)

Index: D: Technical terms

<Product>

Division name: 01 IC

Category 1: 12 Memory

Category 2: 2. Serial EEPROM

Cal. No.: Overall

Related documents:

Question:

What about the basic terms (Test pin, ORG pin)

Answer:

TEST pin

This is an input pin used to enter a test mode when tests are conducted during an SII inspection process. This information is not provided to users. It can be used with a GND or Vcc connection, or in an open state (see note). This is important in maintaining compatibility with the pin layouts of other companies. Some users fear that the test mode may be inadvertently entered during operation, but such fears are unnecessary, as a potential of at least 10 V must be constantly supplied to enter the test mode.

(Note) Since the TEST pin has a C-MOS input structure, the GND or Vcc connection is most suited for this pin.

ORG (Organization) pin

Input pin used to specify a memory configuration. A normal memory has a “16 bit/1 address” data configuration and includes no ORG pin. Competing manufacturers, however, have released products that enable data to be switched between “x16” and “x8” using “H” or “L” of the ORG pin. Since this function is provided for the 93C series of the NS code, there is a compatibility problem. SII has not yet released products featuring this function.

<Remarks>

FAQ No.: 12014

Collection of Product FAQs

Author: Kano Tomoo Date: 98/11/12 (Thursday) 10:17 (modified: 99/01/13)

<Information level>

A: Public (Printing O.K.)

Index: B: Technical

<Product>

Division name: 01 IC

Category 1: 12 Memory

Category 2: 2. Serial EEPROM

Cal. No.: Overall

Related documents:

Question:

Malfunction (false-write, illegal data)

Answer:

[Malfunction of the EEPROM] (key words: false-store(illegal data)

The EEPROM may malfunction (false-store) due to power-on/off or noise from the microcomputer. The defect rate, however, is on the order of ppm. Even though, this could be a serious problem for the users and to the applications.

- This problem essentially results from users' design techniques, but the manufacturer should make efforts to prevent this defect. As the unit price continuously decreases, this is particularly important in discriminating us from our competitors.
- Improving the business techniques of the manufacturer
  Malfunction basically results from a user's inappropriate operation, so the user is the responsible party. We, however, must bear responsibility for defects in the IC. Thus, the best action to take depends on whether the user or SII is responsible for the defect. In practice, however, it is difficult to determine from a user's claim or inquiry, or through an agent, who is responsible for a defect.

In such a case, inform the Business Techniques section of the situation as soon as possible. In addition, see FAQ on other "malfunctions" for technical information.

<Remarks>

FAQ No.: 12012

Collection of Product FAQs

Author: Kano Tomoo Date: 98/11/12 (Thursday) 10:17 (modified: 99/01/13)

<Information level>

A: Public (Printing O.K.)

Index: B: Technical

<Product>

Division name: 01 IC

Category 1: 12 Memory

Category 2: 2. Serial EEPROM

Cal. No.: Overall

Related documents:

Question:

Power-on clear in S-93CxxA, S-29xxxA, notes for power-on (malfunction)

Answer:

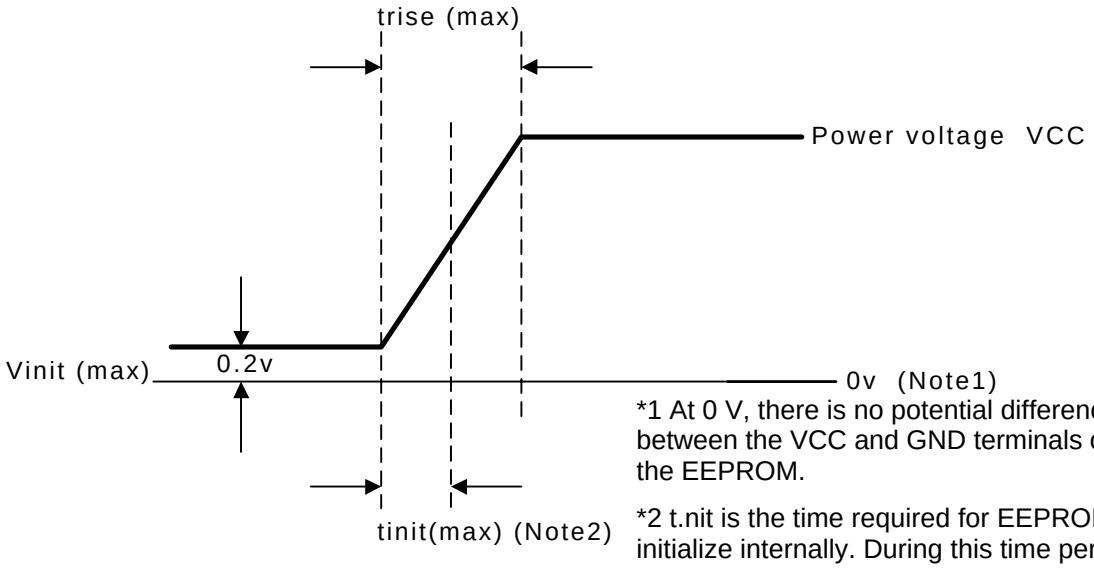
1. This IC series has a built-in power-on clear circuit.

   This circuit instantly initializes the EEPROM when the power voltage is activated. Since malfunction may occur if initialization has not been completed normally, the conditions specified below are required to activate the power voltage in order to operate the power-on clear circuit normally.

2. Notes on power-on

① Method for activating the power voltage

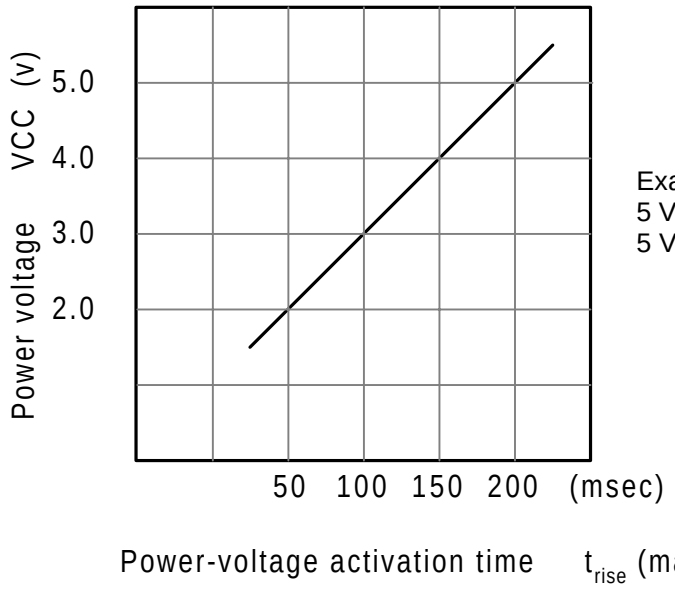
As shown in Fig. 1, activate the power voltage starting from a maximum of 0.2 V so that the power voltage reaches the operating value within the time specified as tRISE. If the operating power voltage is, for example, 5.0 V, tRISE = 200 ms, as shown in Fig. 2. Thus, the power voltage must be activated within 200 ms.



*1 At 0 V, there is no potential difference between the VCC and GND terminals of the EEPROM.

*2 t.nit is the time required for EEPROM to initialize internally. During this time period, the EEPROM will not accept commands.

Fig. 1 Activation of the Power Voltage



Example) If the operating power voltage is 5 V, ensure that the power voltage reaches 5 V within 20.0 ms.

Fig. 2 Maximum power-voltage activation time

② Initialize time tinit

The EEPROM is instantly initialized when the power voltage is activated.

Since the EEPROM does not accept commands during initialization, the transmission of commands to the EEPROM must be started after this initialization time period.

Fig. 3 shows the time required to initialize the EEPROM.

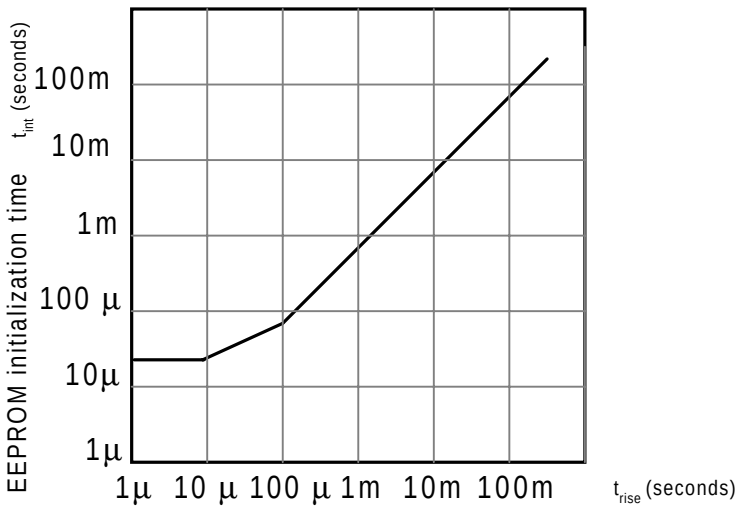


Fig. 3 EEPROM initialization time

When the power-on clear circuit has finished initialization normally, the EEPROM enters a program-disabled state. If the power-on clear circuit does not operate, the following situation is likely:

- In some cases, a previously entered command has been enabled. If, for example, a program-enabled command has been enabled and the input terminal mistakenly recognizes a write command due to extraneous noise while the next command is being entered, writing may be executed.

The following may prevent the power-on clear circuit from operating:

- If the power lines of the microcomputer and EEPROM are separated from each other, and the output terminals of the microcomputer and EEPROM are wired or connected to each other, there may be a potential difference between the power lines of the EEPROM and microcomputer. If the voltage of the microcomputer is higher, a current may flow from the output terminal of the microcomputer to the power line of the EEPROM via a parasitic diode in the DO pin of the EEPROM. Therefore, the power voltage of the EEPROM has an intermediate potential to prevent power-on from being cleared.
- During an access to the EEPROM, the voltage may decrease due to power-off. Even if the microcomputer has been reset due to a decrease in voltage, the EEPROM may malfunction if EEPROM power-on clear operation conditions are not met. For the EEPROM power-on clear operation conditions, see “Method for Activating the Power Voltage.”

<Remarks>

FAQ No.: 12011

Collection of Product FAQs

Author: Kano Tomoo Date: 98/11/12 (Thursday) 10:17 (modified: 99/01/13)

<Information level>

B: For Distri & Rep (Printing N.G.)

Index: B: Technical

<Product>

Division name: 01 IC

Category 1: 12 Memory

Category 2: 2. Serial EEPROM

Cal. No.: Overall

Related documents:

Question:

False-writes in S-93C, S-29 series: inadvertent activation of CS (malfunction)

Answer:

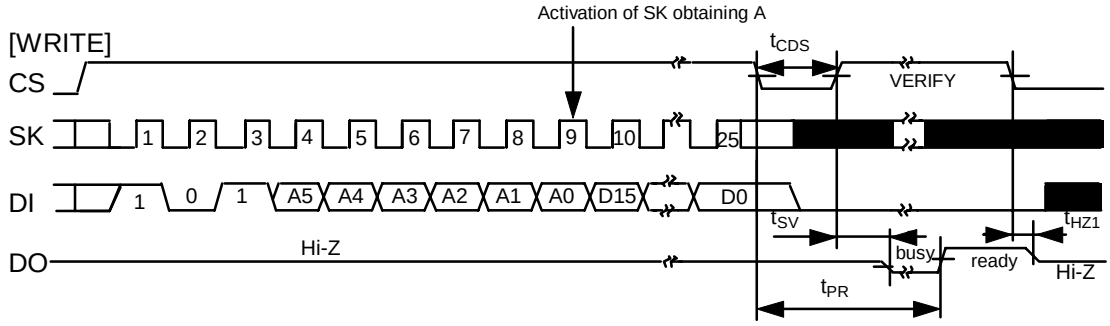
Inadvertent writing in the S-29 series

In the S-29 series, when a CS input is inadvertently activated during a write command, undefined data may be written. Relevant timings are shown below.

A command is composed of the following: “start bit + two command bits + address + (data).”

The figure below shows the timings in which commands are set (In the figure, the portion denotes the rising edge of SK.)

In the case of a write command, after a final address has been input and while 16-bit data is being input, undefined data is written when the CS input is changed from H to L.



Case in which, during a command entry, CS is changed from H to L with a timing that differs by a predetermined minimum number of clocks.

In the case of a write command, if the number of clocks is smaller than the predetermined value, data is loaded so as to be changed from D15 to D0. When, for example, CS is shifted from H to L after three clocks, data, which would otherwise have been stored in D15 to D13, is stored in D2 to D0, while undefined data is stored on the upper side a storage state in which the internal logic has been changed to either H or L). In addition, if the number of clocks is greater than the predetermined value, the last 16 pieces of data are stored correctly.

<Remarks>

FAQ No.: 12008

Collection of Product FAQs

Author: Kano Tomoo Date: 98/11/12 (Thursday) 10:17 (modified: 99/01/13)

<Information level>

A: Public (Printing O.K.)

Index: A: General

<Product>

Division name: 01 IC

Category 1: 12 Memory

Category 2: 2. Serial EEPROM

Cal. No.: Overall

Related documents:

Question:

EEPROM compatibility table, cross reference

Answer:

EEPROM compatibility table

Product name	Key word	NATIONAL SEMICONDUCTOR	ATMEL	ST Micro electronic
S-29130ADPA	EE,1KB,DIP,3W	NM93C(S)46ZEN	AT93C46-10PI-2.5	ST93C46(7)AB6
S-93C46ADP	↑	↑	↑	↑
S-29130AFJA-TB	EE,1KB,SOP1,3W	NM93C(S)46ZEM8	AT93C46R-10SI-2.5	ST93C46(7)TM6013TR
S-93C46AFJ-TB	↑		↑	↑
S-29130ADFJA-TB	EE,1KB,SOP2,3W		AT93C46W-10SI-2.5	ST93C46(7)AM6013TR
S-93C46ADFJ-TB	↑		↑	↑
S-29131ADPA	EE,1KB,DIP,3W,PROT	NM93C46ZEN	AT93C46-10PI-2.5	ST93C46(7)B6
S-29131AFJA-TB	EE,1KB,SOP1,3W,PROT	NM93C46ZEM8	AT93C46R-10SI-2.5	ST93C46(7)TM6013TR
S-29220ADPA	EE,2KB,DIP,3W	NM93C(S)56ZEN	AT93C56-10PI-2.5	ST93C56(7)AB6
S-29220AFJA-TB	EE,2KB,SOP1,3W	NM93C(S)56ZEM8	AT93C56R-10SI-2.5	ST93C56(7)TM6013TR
S-29220ADFJA-TB	EE,2KB,SOP2,3W		AT93C56W-10SI-2.5	ST93C56(7)AM6013TR
S-29221ADPA	EE,2KB,DIP,3W,PROT	NM93C56ZEN	AT93C56-10PI-2.5	ST93C56(7)B6
S-29221AFJA-TB	EE,2KB,SOP1,3W,PROT	NM93C56ZEM8	AT93C56R-10SI-2.5	ST93C56(7)TM6013TR
S-29330ADPA	EE,4KB,DIP,3W	NM93C(S)66ZEN	AT93C66-10PI-2.5	ST93C66(7)AB6
S-29330AFJA-TB	EE,4KB,SOP1,3W	NM93C(S)66ZEM8	AT93C66R-10SI-2.5	ST93C66(7)TM6013TR
S-29330ADFJA-TB	EE,4KB,SOP2,3W		AT93C66W-10SI-2.5	ST93C66(7)AM6013TR
S-29331ADPA	EE,4KB,DIP,3W,PROT	NM93C66ZEN	AT93C66-10PI-2.5	ST93C66(7)B6
S-29331AFJA-TB	EE,4KB,SOP1,3W,PROT	NM93C66ZEM8	AT93C66R-10SI-2.5	ST93C66(7)TM6013TR
S-29430ADP	EE,8KB,DIP,3W			
S-29430AFE-TF	EE,8KB,SOP1,3W			
S-24C01ADPA-01	EE,1KB,DIP,2W		AT24C01A-10PI-2.5	ST24(25)C(W)01B6
S-24C01AFJA-TB-01	EE,1KB,SOP,2W		AT24C01A-10SI-2.5	ST24(25)C(W)01M6TR
S-24C02ADPA-01	EE,2KB,DIP,2W	NM24C02(03)LEN	AT24C02-10PI-2.5	ST24(25)C(W)02B6
S-24C02AFJA-TB-01	EE,2KB,SOP,2W	NM24C02(03)LEM8	AT24C02N-10SI-2.5	ST24(25)C(W)02M6TR
S-24C04ADPA-01	EE,4KB,DIP,2W	NM24C04(05)LEN	AT24C04-10PI-2.5	ST24(25)C(W)04B6

S-24C04AFJA-TB-01	EE,4KB,SOP,2W	NM24C04(05)LEM8	AT24C04N-10SI-2.5	ST24(25)C(W)04M6TR
S-24C08ADPA-01	EE,8KB,DIP,2W	NM24C08(09)LEN	AT24C08-10PI-2.5	ST24(25)C(W)08B6
S-24C08AFJA-TB-01	EE,8KB,SOP,2W	NM24C08(09)LEM8	AT24C08N-10SI-2.5	ST24(25)C(W)08M6TR
S-24C16ADPA-01	EE,16KB,DIP,2W	NM24C16(17)LEN	AT24C16-10PI-2.5	ST24(25)C(W)16B6
S-24C16AFJA-TB-01	EE,16KB,SOP,2W	NM24C16(17)LEM8	AT24C16N-10SI-2.5	ST24(25)C(W)16M6TR
S-29L130AFE-TB	EE,1KB,SOP1,3W,L/V	NM93C(S)46XLZEM8	AT93C46R-10SI-1.8	ST93C46(7)TM6013TR
S-29L130ADFE-TB	EE,1KB,SOP2,3W,L/V		AT93C46W-10SI-1.8	ST93C46(7)AM6013TR
S-29L131ADFE-TB	EE,1KB,SOP2,3W,L/V,PROT	NM93C(S)46XLZEM8	AT93C46W-10SI-1.8	ST93C46(7)AM6013TR
S-29L220AFE-TB	EE,2KB,SOP1,3W,L/V	NM93C(S)56XLZEM8	AT93C56R-10SI-1.8	ST93C56(7)TM6013TR
S-29L220ADFE-TB	EE,2KB,SOP2,3W,L/V		AT93C56W-10SI-1.8	ST93C56(7)AM6013TR
S-29L221ADFE-TB	EE,2KB,SOP2,3W,L/V,PROT	NM93C(S)56XLZEM8	AT93C56W-10SI-1.8	ST93C56(7)AM6013TR
S-29L330AFE-TB	EE,4KB,SOP1,3W,L/V	NM93C(S)66XLZEM8	AT93C66R-10SI-1.8	ST93C66(7)TM6013TR
S-29L330ADFE-TB	EE,4KB,SOP2,3W,L/V		AT93C66W-10SI-1.8	ST93C66(7)AM6013TR
S-29L331ADFE-TB	EE,4KB,SOP2,3W,L/V,PROT	NM93C(S)66XLZEM8	AT93C66W-10SI-1.8	ST93C66(7)AM6013TR

<Remarks>

FAQ No.: 12007

Collection of Product FAQs

Author: Kano Tomoo Date: 98/11/12 (Thursday) 10:17 (modified: 99/01/13)

<Information level>

A: Public (Printing O.K.)

Index: D (Technical terms)

<Product>

Division name: 01 IC

Category 1: 12 Memory

Category 2: 2. Serial EEPROM

Cal. No.: Overall

Related documents:

Question:

What about the basic terms (memory protect, reset, CS)?

Answer:

Memory protect, reset →S-29xx1A, S-29x94A, S-29x55A

Function for prohibiting a write command from being executed in a certain region of the memory space. This function is enabled by controlling the protect or reset input pin (select/deselect protect). This reset prevents the microcomputer from running uncontrollably and also prevents false-writes caused by noise in order to protect data.

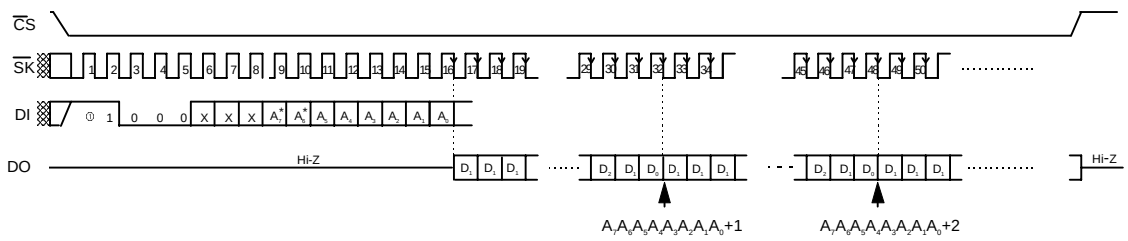
Ex.: Storage of ID codes and product shipment adjustment data

(Note) S-29xx1A and S-29x94A protect 50% of memory, starting with the leading address.

CS, /CS (/CS: S-29x55A, S-29x94A)

CS is an input pin used to select the execution of a command. It is selected using “H” and deselected using “L” (the reverse is true for /CS)

→ /CS is useful on the interface of the microcomputer (L active is mainly used for the microcomputer). Malfunction, however, is likely to be caused by noise upon power-on if a command is executed at the GND level.



<Remarks>

FAQ No.: 12006

Collection of Product FAQs

Author: Kano Tomoo Date: 98/11/12 (Thursday) 10:17 (modified: 99/01/13(Wednesday))

<Information level>

A: Public (Printing O.K.)

Index: A: General

<Product>

Division name: 01 IC

Category 1: 12 Memory

Category 2: 2. Serial EEPROM

Cal No.: Overall

Related documents:

Question:

Concept of the compatibility, features, and markets of the S-29 series

Answer:

[Compatibility of the EEPROM]

In terms of memory, most SII EEPROMs are compatible with our competitors' standard products in their operation codes. If another company's product is to be replaced by a corresponding SII product, the DC/AC specifications desired by the user must be carefully determined.

The key words for the products are given below.

Our competitor's 93C-series products are compatible with SII's S-29xx0A-series products, and our competitor's 24C-series products are compatible with SII's S-24C-series products.

The key word for each company is given below.

NM93C : National Semiconductor

AT93C : ATMEL

93C : Microchip

M93C : ST Micro electronic (formerly SGS Tomson ST93C)

CAT93C : Catalyst

AK93C : Asahi Kasei

BR93C : ROHM

<Remarks>

FAQ No.: 12005

Collection of Product FAQs

Author: Kano Tomoo Date: 98/11/12 (Thursday) 10:17 (modified: 99/01/13(Wednesday))

<Information level>

A: Public (Printing O.K.)

Index: A: General

<Product>

Division name: 01 IC

Category 1: 12 Memory

Category 2: 2. Serial EEPROM

Cal No.: Overall

Related documents:

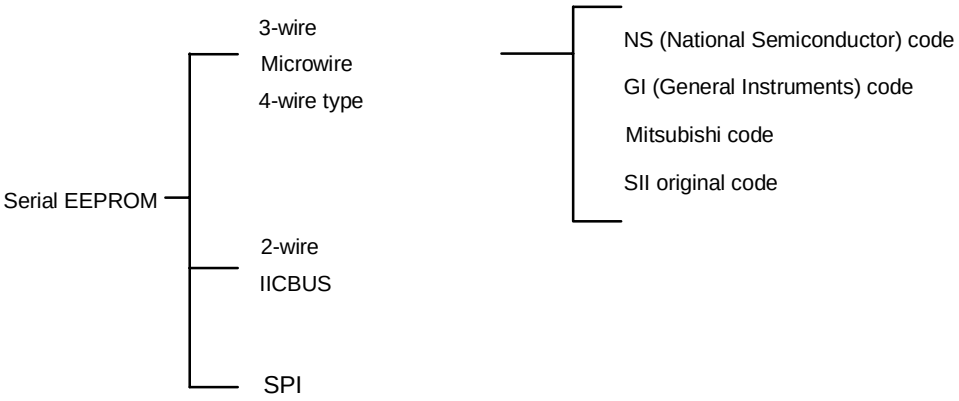
Question:

How are operation codes classified?

A:

[EEPROM operation codes]

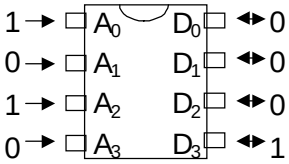
In the serial EEPROM, the operation codes can be classified into several types. Our competitors have released products compatible with each type of operation code. The key words of the operation codes are given below.



1. Serial and parallel

   Data reading and writing are divided into serial and parallel types.

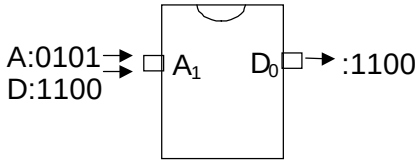
ex.: Parallel



Addresses and data are processed in parallel.

[Advantage] Fast processing

ex.: Serial



Addresses and data are processed in serial.

[Advantages] The size can be reduced due to the reduced number of I/O terminals, and fewer wires are required for the substrate.

The package can be downsized and manufactured inexpensively.

2. 3-wire type, microwire, 4-wire type

   Composed of four pins, including three input pins CS, SK, and DI, and an output pin DO. Since DI and DO can be directly coupled together, the EEPROM can be virtually composed of three pins (the 4-wire type includes an additional Ready/Busy pin, but is still referred to as a "3-wire type").

① NS code: The key word is "93Cx." Compatible with SII S-29xxOA.

   General code used by many competing companies. Mass produced and low in cost.

② GI code

   General Instrument Inc.'s original code. Its markets continue to dwindle.

③ Mitsubishi code: The key word is "M6M8."Compatible with SII S-29x55A. Serial-port direct-coupling type in which commands and data are composed of x8 units. Intended for the TV and VTR markets and primarily sold as a set with Mitsubishi microcomputers.

④ SII original code: S-29x9xA

   Serial-port direct-coupling type in which commands and data are composed of x8 units. Intended for technology-oriented users.

3. 2-wire type, IICBUS: The key word is "24C." Compatible with SII S-24CxxA. Composed of two pins: an input pin (SCL) and an I/O pin (SDA). Phillips Inc. owns a relevant patent.

   [Advantages] Fewer wires are required, and the microcomputer port can be shared with another IICBUS. TV set maker will be main market.

4. SPI: The key word is "25C." Not compatible with SII. Under development. Composed of four pins: three input pins CS, SCK, and SI, and an input pin SO. In the case of the EEPROM, the advantages are high speed (5 MHz at 5v) and a high capacity (128 Kbytes).

<Remarks>

FAQ No.: 12004

Collection of Product FAQs

Author: Kano Tomoo Date: 98/11/12 (Thursday) 10:17 (modified: 99/01/13(Wednesday))

<Information level>

A: Public (Printing O.K.)

Index: D: Technical Terms

<Product>

Division name: 01 IC

Category 1: 12 Memory

Category 2: 2. Serial EEPROM

Cal No.: Overall

Related documents:

Question:

What are the basic operation codes?

Answer:

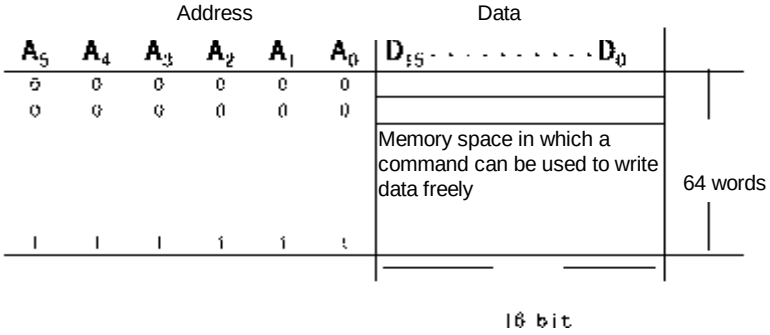
[Terms required to understand EEPROM data sheets (1)] Basic commands

- Data read, READ
  Reads data from a specified address
- Data write, WRITE or PROGRAM
  Writes data to a specified address
- Data erase, ERASE
  Erases data at a specified address (all “1”’s)
- Chip write, WRAL
  Writes the same (word) data in all address spaces
- Chip erase, ERAL
  Erases data in all address spaces (all “1”’s)
- Program disable, EWDS or PDS
  Prohibits write operations (WRITE), and prevents false-writes caused by noise or uncontrollable running of the CPU
- Program enable, EWES or PEN
  Enables write operations (WRITE)

[Note]

When the power to the EEPROM is turned on, the internal circuit of the IC is reset and the program disable mode is entered. Thus, following power-on, the program enable command must be entered in order to write data.

Memory space: In the case of the S-29130A (64 words X 16 bits)



<Remarks>

FAQ No.: 12003

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Author: Kano Tomoo Date: 98/11/12 (Thursday) 10:17 (modified: 99/01/13(Wednesday))

<Information level>

A: Public (Printing O.K.)

Index: D: Technical terms

<Product>

Division name: 01 IC

Category 1: 12 Memory

Category 2: 2. Serial EEPROM

Cal No.: Overall

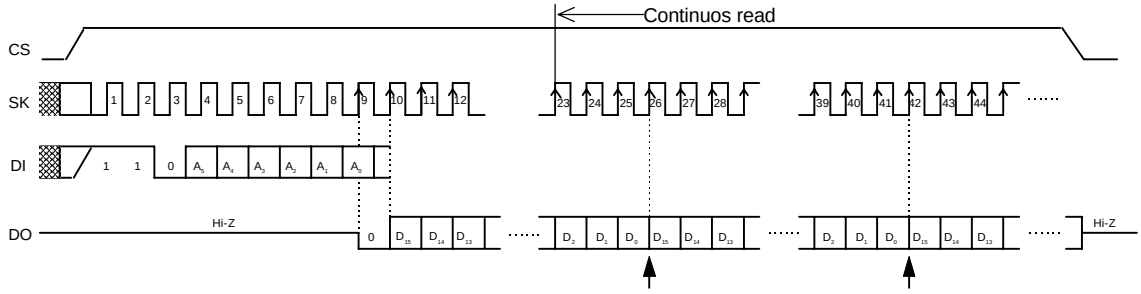
Related documents:

Question:

What about the basic terms. (continuous read, sequential read)?

Answer:

- Continuous read, sequential read →S-93C series, S-29 series, S-24C series
  Function by which data is read from a specified address using a read command, followed by the output of the next address. This is useful when there is a large amount of user data (ex.: ID codes).



- Serial-port direct coupling, microcomputer interface, 8-bit command
  →S-29x9xA, S-29x55A, S-2900A

  The serial port is a serial I/O port provided for a microcomputer. A device that can be easily and directly coupled to this port is referred to as a “serial-port direct-coupling type” or a “microcomputer interface.”

1. The EEPROM is configured as follows for simple direct coupling:

① Data is input at the rising edge of the SK input clock, and output at its falling edge.

② Commands and data are input and output in 8 bits.

2. A microcomputer with a serial port communicates in 8 bits (8 clocks).

   This configuration can substantially reduce the number of programs required for the microcomputer. The advantages are easy programming and a reduced ROM capacity.

<Remarks>

FAQ No.: 12002

Collection of Product FAQs

Creator: Takashi Ebisawa Date: 98/01/13 (Wednesday) 10:51 (modified: 99/01/13(Wednesday))

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A: Public (Printing O.K.)

Index: D: Technical terms

<Product>

Division name: 01 IC

Category 1: 12 Memory

Category 2: 2. Serial EEPROM

Cal No.: Overall

Related documents:

Question:

What is the EEPROM?

Answer:

1. Electrically Erasable Programmable Read Only Memory

- Why this memory is referred to as “read only” despite the fact that it enables data to be rewritten?
  The EEPROM requires a longer time for writing than a RAM, so it is used exclusively for reading.
- What is the “memory”?
  Elements storing data. Data is generally represented by the digits “0” and “1.”
- What is the “ROM”?
  Read Only Memory
  Reference: RAM is Random Access read write Memory.

<Remarks>

FAQ No.: 12001