

# RC4200

## Analog Multiplier

### Features

- High accuracy
- Nonlinearity – 0.1%  
Temperature coefficient – 0.005%/°C
- Multiple functions
- Multiply, divide, square, square root, RMS-to-DC conversion, AGC and modulate/demodulate
- Wide bandwidth – 4 MHz
- Signal-to-noise ratio – 94 dB

### Applications

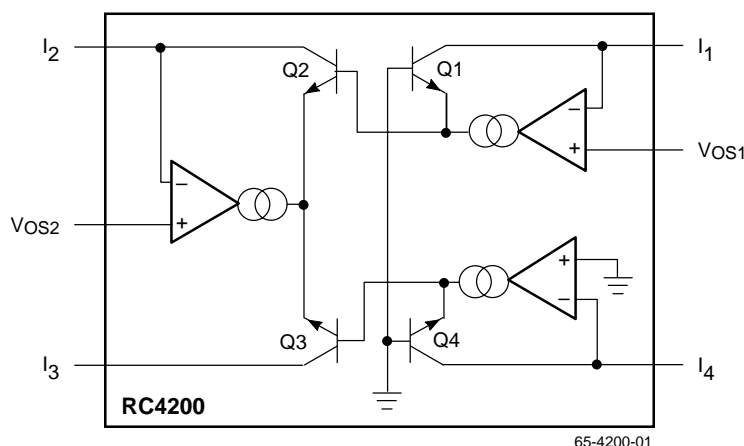
- Low distortion audio modulation circuits
- Voltage-controlled active filters
- Precision oscillators

### Description

The RC4200 analog multiplier has complete compensation for nonlinearity, the primary source of error and distortion. This multiplier also has three onboard operational amplifiers designed specifically for use in multiplier logging circuits. These amplifiers are frequency compensated for optimum AC response in a logging circuit, the heart of a multiplier, and can therefore provide superior AC response.

The RC4200 can be used in a wide variety of applications without sacrificing accuracy. Four-quadrant multiplication, two-quadrant division, square rooting, squaring and RMS conversion can all be easily implemented with predictable accuracy. The nonlinearity compensation is not just trimmed at a single temperature, it is designed to provide compensation over the full temperature range. This nonlinearity compensation combined with the low gain and offset drift inherent in a well-designed monolithic chip provides a very high accuracy and a low temperature coefficient.

### Block Diagram



## Functional Description

The RC4200 multiplier is designed to multiply two input currents ( $I_1$  and  $I_2$ ) and to divide by a third input current ( $I_4$ ). The output is also in the form of a current ( $I_3$ ). A simplified circuit diagram is shown in the Block Diagram. The nominal relationship between the three inputs and the output is:

$$I_3 = \frac{I_1 I_2}{I_4} \quad (1)$$

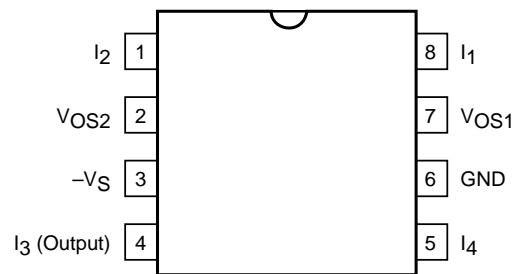
The three input currents must be positive and restricted to a range of 1  $\mu$ A to 1 mA. These currents go into the multiplier chip at op amp summing junctions which are nominally at zero volts. Therefore, an input voltage can be easily converted to an input current by a series resistor. Any number of currents may be summed at the inputs. Depending on the application, the output current can be converted to a voltage by an external op amp or used directly. This capability of combining input currents and voltages in various combinations provides great versatility in application.

Inside the multiplier chip, the three op amps make the collector currents of transistors Q1, Q2 and Q4 equal to their respective input currents ( $I_1$ ,  $I_2$ , and  $I_4$ ). These op amps are designed with current source outputs and are phase-compensated for optimum frequency response as a multiplier. Power drain of the op amps was minimized to prevent the introduction of undesired thermal gradients on the chip. The three op amps operate on a single supply voltage (nominally -15V) and total quiescent current drain is less than 4 mA. These special op amps provide significantly improved performance in comparison to 741-type op amps.

The actual multiplication is done within the log-antilog configuration of the Q1-Q4 transistor array. These four transistors, with associated proprietary circuitry, were specially designed to precisely implement the relationship.

$$V_{BEN} = \frac{kT}{Q} \ln \frac{I_{CN}}{I_{SN}} \quad (2)$$

## Pin Assignments



Previous multiplier designs have suffered from an additional undesired linear term in the above equation; the collector current times the emitter resistance. The  $I_{CrE}$  term introduces a parabolic nonlinearity even with matched transistors. Fairchild Semiconductor has developed a unique and proprietary means of inherently compensating for this undesired  $I_{CrE}$  term. Furthermore, this Fairchild Semiconductor developed circuit technique compensates linearity error over temperature changes. The nonlinearity versus temperature is significantly improved over earlier designs.

From equation (2) and by assuming equal transistor junction temperatures, summing base-to-emitter voltage drops around the transistor array yields:

$$\frac{KT}{q} \left[ \ln \frac{I_1}{I_{S1}} = \ln \frac{I_2}{I_{S2}} - \ln \frac{I_3}{I_{S3}} - \ln \frac{I_4}{I_{S4}} \right] = 0 \quad (3)$$

This equation reduces to:

$$\frac{I_1 I_2}{I_3 I_4} = \frac{I_{S1} I_{S2}}{I_{S3} I_{S4}} \quad (4)$$

The rate of reverse saturation current  $I_{S1} I_{S2} / I_{S3} I_{S4}$ , depends on the transistor matching. In a monolithic multiplier this matching is easily achieved and the rate is very close to unity, typically  $1.0 \pm 1\%$ . The final result is the desired relationship:

$$I_3 = \frac{I_1 I_2}{I_4} \quad (5)$$

The inherent linearity and gain stability combined with low cost and versatility makes this new circuit ideal for a wide range of nonlinear functions.

## Absolute Maximum Ratings

Parameter		Min.	Max.	Unit
Supply Voltage <sup>1</sup>			-22	V
Input Current			-5	mA
Storage Temperature Range	RM4200/4200A	-65	+150	°C
	RC4200/4200A	-55	+125	°C
Operating Temperature Range	RM4200/4200A	-55	+125	°C
	RC4200/4200A	0	+70	°C

**Notes:**

1. For a supply voltage greater than -22V, the absolute maximum input voltage is equal to the supply voltage.
2. Observe package thermal characteristics.

## Thermal Characteristics

(Still air, soldered into PC board)

	8-Lead Plastic DIP	8-Lead SOIC	8-Lead Ceramic DIP
Maximum Junction Temperature	+125°C	+125°C	+175°C
Maximum PD TA < 50°C	468mW	300mW	833mW
Thermal Resistance $\theta_{JC}$	—	—	45°C/W
Thermal Resistance $\theta_{JA}$	160°C/W	240°C/W	150°C/W
For TA > 50°C Derate at	6.25mW/°C	4.17mW/°C	8.33mW/°C

## Electrical Characteristics

(Over operating temperature range, VS = -15V unless otherwise noted)

Parameters	Test Conditions	4200A			4200			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Total Error as Multiplier	TA = +25°C							
	Untrimmed <sup>1</sup>			±2.0			±3.0	%
	With External Trim		±0.2			±0.2		%
	Versus Temperature		±0.005			±0.005		%/°C
	Versus Supply (-9 to -18V)		±0.1			±0.1		%/V
Nonlinearity <sup>2</sup>	50µA ≤ I1,2,4 ≤ 250 µA, TA = +25°C			±0.1			±0.3	%
Input Current Range (I1, I2 and I4)		1.0		1000	1.0		1000	µA
Input Offset Voltage	I1 = I2 = I4 = 150 µA TA = +25°C			±5.0			±10	mV
Input Bias Current	I1 = I2 = I4 = 150 µA TA = +25°C			300			500	nA
Average Input Offset Voltage Drift	I1 = I2 = I4 = 150 µA			±50			±100	µV/°C
Output Current Range (I3) <sup>3</sup>		1.0		1000	1.0		1000	µA

### Electrical Characteristics (continued)

(Over operating temperature range,  $V_S = -15V$  unless otherwise noted)

Parameters	Test Conditions	4200A			4200			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Frequency Response, -3dB point			4.0			4.0		MHz
Supply Voltage		-18	-15	-9.0	-18	-15	-9.0	V
Supply Current	$I_1 = I_2 = I_4 = 150 \mu A$ $T_A = +25^\circ C$			4.0			4.0	mA

**Notes:**

1. Refer to Figure 6 for example.
2. The input circuits tend to become unstable at  $I_1, I_2, I_4 < 50 \mu A$  and linearity decreases when  $I_1, I_2, I_4 > 250 \mu A$  (eq. @  $I_1 = I_2 = 500 \mu A$ , nonlinearity error  $\approx 0.5\%$ ).
3. These specifications apply with output ( $I_3$ ) connected to an op amp summing junction. If desired, the output ( $I_3$ ) at pin (4) can be used to drive a resistive load directly. The resistive load should be less than  $700\Omega$  and must be pulled up to a positive supply such that the voltage on pin (4) stays within a range of 0 to +5V.

## Applications Discussion

### Current Multiplier/ Divider

The basic design criteria for all circuit configurations using the RC4200 multiplier is contained in equation (1), that is,

$$I_3 = \frac{I_1 I_2}{I_4}$$

The current-product-balance equation restates this as:

$$I_1 I_2 = I_3 I_4 \quad (6)$$

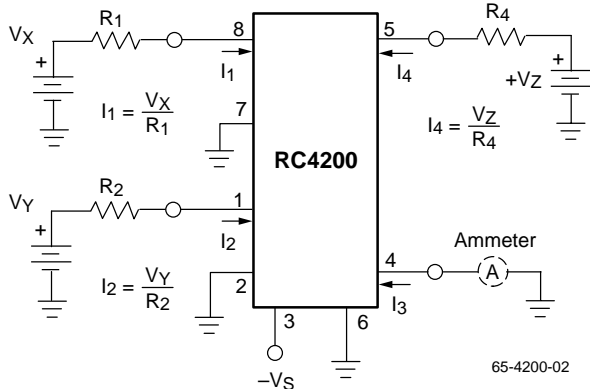


Figure 1. Current Multiplier/Divider

### Dynamic Range and Stability

The precision dynamic range for the RC4200 is from +50  $\mu A$  to +250  $\mu A$  inputs for  $I_1, I_2$  and  $I_4$ . Stability and accuracy degrade if this range is exceeded.

To improve the stability for input currents less than 50  $\mu A$ , filter circuits (RSCS) are added to each input (see Figure 2).

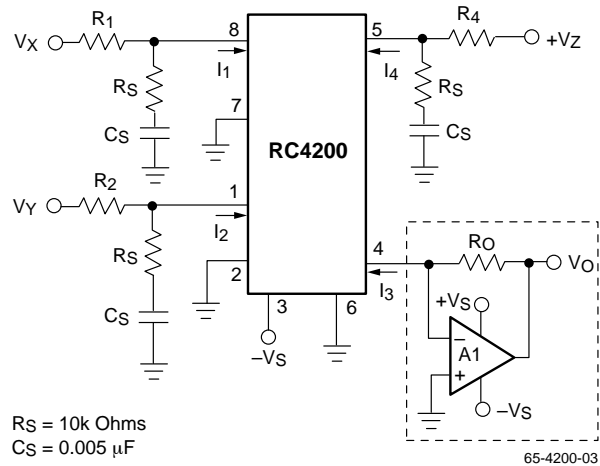
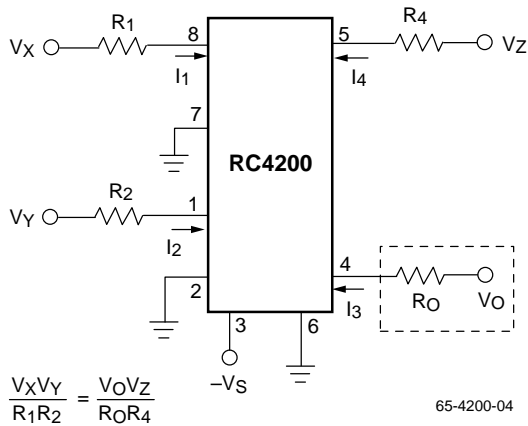


Figure 2. Current Multiplier/Divider with Filters

Amplifier A1 is used to convert the  $I_3$  current to an output voltage.

- Multiplier:  $V_Z = \text{constant} \neq 0$
- Divider:  $V_Y = \text{constant} \neq 0$

**Voltage Multiplier/Divider**



**Figure 3. Voltage Multiplier/Divider**

Solving for  $V_0 = \frac{V_X V_Y}{V_Z} \frac{R_0 R_4}{R_1 R_2}$

For a multiplier circuit  $V_Z = V_R = \text{constant}$

Therefore:  $V_0 = V_X V_Y K$  where  $K = \frac{R_0 R_4}{V_R R_1 R_2}$

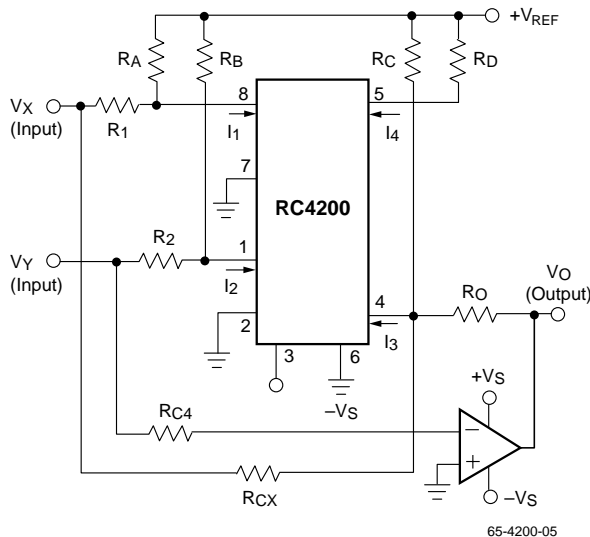
For a divider circuit  $V_Y = V_R = \text{constant}$

Therefore:  $V_0 = \frac{V_X}{V_Z} K$  where  $K = \frac{V_R R_0 R_4}{R_1 R_2}$

**Extended Range**

The input and output voltage ranges can be extended to include 0 and negative voltage signals by adding bias currents. The RSCS filter circuits are eliminated when the input and biasing resistors are selected to limit the respective currents to 50  $\mu\text{A}$  min. and 250  $\mu\text{A}$  max.

**Extended Range Multiplier**



**Figure 4. Extended Range Multiplier**

Resistors  $R_a$  and  $R_b$  extend the range of the  $V_X$  and  $V_Y$  inputs by picking values such that:

$$I_1(\text{min.}) = \frac{V_X(\text{min.})}{R_1} + \frac{V_{REF}}{R_a} = 50 \mu\text{A},$$

and  $I_1(\text{max.}) = \frac{V_X(\text{max.})}{R_1} + \frac{V_{REF}}{R_a} = 250 \mu\text{A},$

also  $I_2(\text{min.}) = \frac{V_Y(\text{min.})}{R_2} + \frac{V_{REF}}{R_b} = 50 \mu\text{A},$

and  $I_2(\text{max.}) = \frac{V_Y(\text{max.})}{R_2} + \frac{V_{REF}}{R_b} = 250 \mu\text{A}.$

Resistor  $R_C$  supplies bias current for  $I_3$  which allows the output to go negative.

Resistors  $R_{CX}$  and  $R_{CY}$  permit equation (6) to balance, i.e.:

$$\left(\frac{V_X}{R_1} + \frac{V_{REF}}{R_a}\right)\left(\frac{V_Y}{R_2} + \frac{V_{REF}}{R_b}\right) = \left(\frac{V_0}{R_0} + \frac{V_{REF}}{R_C} + \frac{V_X}{R_{CX}} + \frac{V_Y}{R_{CY}}\right)\left(\frac{V_{REF}}{R_D}\right)$$

$$\frac{V_Y V_X}{R_1 R_2} + \frac{V_X V_{REF}}{R_1 R_b} + \frac{V_Y V_{REF}}{R_2 R_a} + \frac{V_{REF}}{R_a R_b} =$$

$$\frac{V_0 V_{REF}}{R_0 R_D} + \frac{V_X V_{REF}}{R_{CX} R_D} + \frac{V_Y V_{REF}}{R_{CY} R_D} + \frac{V_{REF}^2}{R_C R_D}$$

**Cross-Product Cancellation**

Cross-products are a result of the  $V_X V_R$  and  $V_Y V_R$  terms. To the extent that  $R_1 R_b = R_{CX} R_D$ , and  $R_2 R_a = R_{CY} R_D$  cross-product cancellation will occur.

**Arithmetic Offset Cancellation**

The offset caused by the  $V_{REF}^2$  term will cancel to the extent that  $R_a R_b = R_0 R_D$ , and the result is:

$$\frac{V_Y V_X}{R_1 R_2} = \frac{V_0 V_{REF}}{R_0 R_D} \text{ or } V_0 = V_X V_Y K$$

where  $K = \frac{R_0 R_D}{V_{REF} R_1 R_2}$

**Resistor Values**

Inputs:

$$V_X(\text{min.}) \leq V_X \leq V_X(\text{max.})$$

$$\Delta V_X = V_X(\text{max.}) - V_X(\text{min.})$$

$$V_Y(\text{min.}) \leq V_Y \leq V_Y(\text{max.})$$

$$\Delta V_Y = V_Y(\text{max.}) - V_Y(\text{min.})$$

$$V_{REF} = \text{Constant (+7V to +18V)}$$

$$K = \frac{V_0}{V_X V_Y} \text{ (Design Requirements)}$$

$$R_1 = \frac{\Delta V_X}{200\mu A}, R_2 = \frac{\Delta V_Y}{200\mu A}, R_d = \frac{V_{REF}}{250\mu A}$$

$$R_a = \frac{\Delta V_X V_{REF}}{250\mu A \Delta V_X - 200\mu A V_X(\max.)}$$

$$R_b = \frac{\Delta V_X V_{REF}}{250\mu A \Delta V_Y - 200\mu A V_Y(\max.)}$$

$$R_c = \frac{R_a R_b}{R_d}, R_{CX} = \frac{R_1 R_b}{R_d}, R_{CY} = \frac{R_2 R_a}{R_d}$$

$$R_0 = \frac{\Delta V_X \Delta V_Y K}{160\mu A}$$

**Multiplying Circuit Offset Adjust**

$$10K \leq R_5 = R_9 = R_{16} \leq 50K$$

$$R_7 = R_{11} = R_{14}, = 100\Omega$$

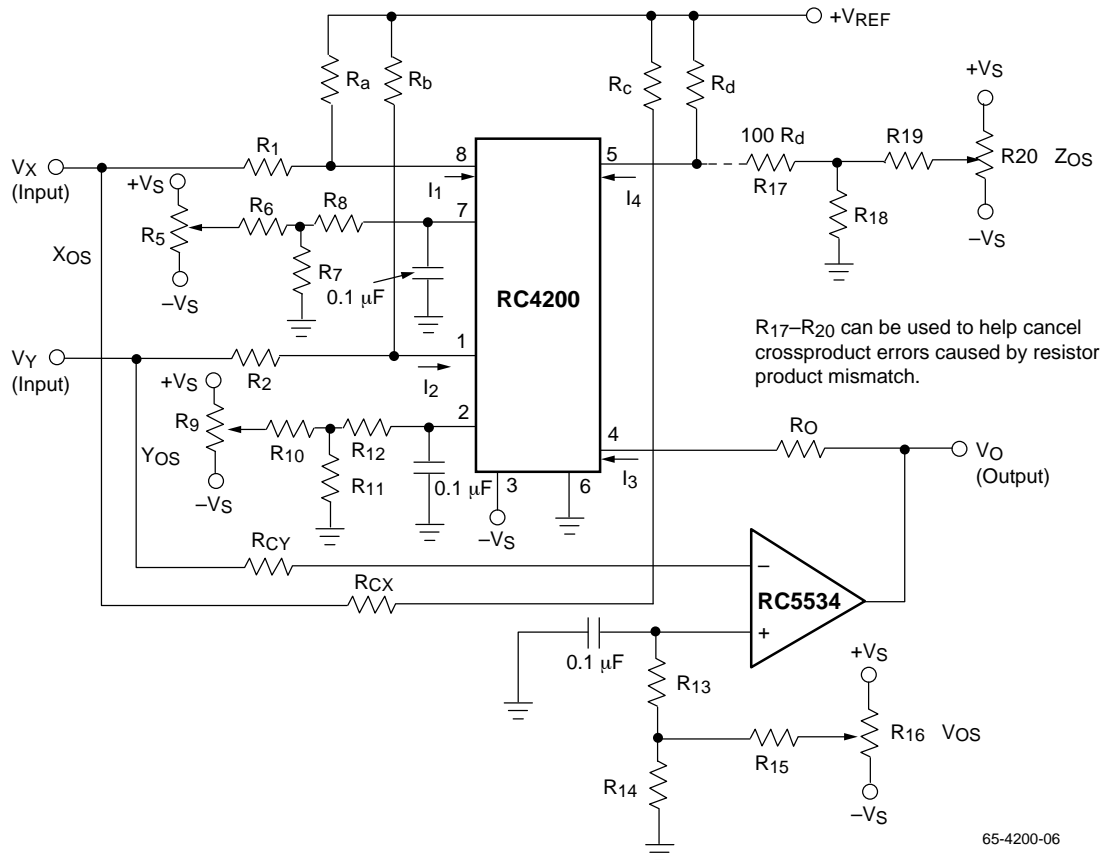
$$R_6 = R_{10} = 100\Omega (V_S/0.05)$$

$$R_{15} = 100\Omega (V_S/0.10)$$

$$R_8 = R_1 \parallel R_a$$

$$R_{12} = R_2 \parallel R_b$$

$$R_{13} = R_0 \parallel R_C \parallel R_{CX} \parallel R_{CY}$$



**Figure 5. Multiplying Circuit Offset Adjust**

**Procedure**

1. 1.Set all trimmer pots to 0V on the wiper.
2. 2.Connect V<sub>X</sub> input to ground. Put in a full scale square wave on V<sub>Y</sub> input. Adjust X<sub>OS</sub>(R<sub>5</sub>) for no square wave on V<sub>0</sub> output (adjust for 0 feedthrough).
3. 3.Connect V<sub>Y</sub> input to ground. Put in a full scale square wave on V<sub>X</sub> input. Adjust Y<sub>OS</sub>(R<sub>9</sub>) for no square wave on V<sub>0</sub> output (adjust for 0 feedthrough).
4. 4.Connect V<sub>X</sub> and V<sub>Y</sub> to ground. Adjust V<sub>OS</sub>(R<sub>16</sub>) for 0V on V<sub>0</sub> output.

## Extended Range Divider

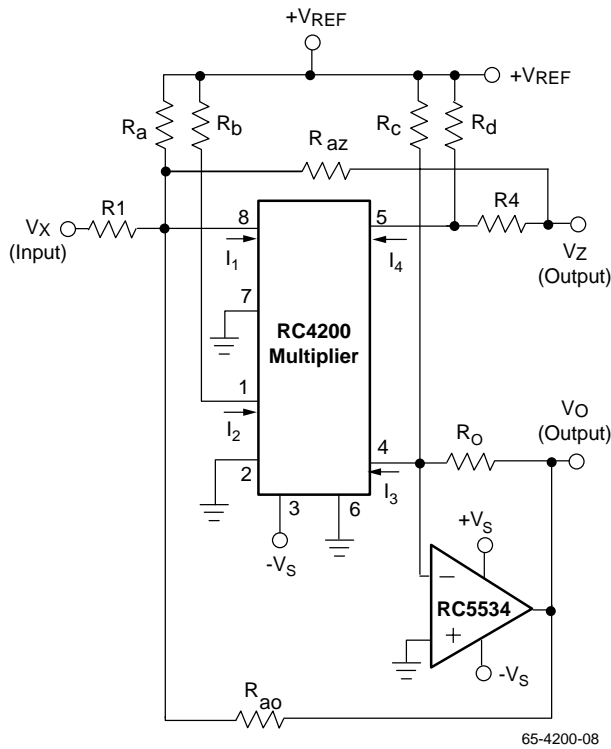


Figure 6. Extended Range Divider

As with the extended range multiplier, resistors  $R_{az}$  and  $R_{ao}$  are added to cancel the cross-product error caused by the biasing resistors, i.e.

$$\left(\frac{V_X}{R_1} + \frac{V_0}{R_{ao}} + \frac{V_Z}{R_{az}} + \frac{V_{REF}}{R_a}\right)\left(\frac{V_{REF}}{R_b}\right) = \left(\frac{V_0}{R_0} + \frac{V_{REF}}{R_c}\right)\left(\frac{V_Z}{R_4} + \frac{V_{REF}}{R_d}\right)$$

$$\frac{V_X V_{REF}}{R_1 R_b} + \frac{V_0 V_{REF}}{R_{ao} R_b} + \frac{V_Z V_{REF}}{R_{az} R_b} + \frac{V_{REF}^2}{R_a R_b} =$$

$$\frac{V_0 V_Z}{R_0 R_4} + \frac{V_0 V_{REF}}{R_0 R_d} + \frac{V_Z V_{REF}}{R_4 R_c} + \frac{V_{REF}^2}{R_c R_d}$$

To cancel cross-product and arithmetic offset:

$$R_{ao} R_b = R_0 R_d, R_{az} R_b = R_4 R_c \text{ and } R_a R_b = R_c R_d$$

and the result is:

$$\frac{V_X V_{REF}}{R_1 R_b} = \frac{V_0 V_Z}{R_0 R_4} \text{ or } V_0 = \frac{V_X}{V_Z K}$$

$$\text{where } K = \frac{V_{REF} R_0 R_4}{R_1 R_b}$$

Notice that it is necessary to match the above resistor cross-products to within the amount of error tolerable in the output offset, i.e., with a 10V F.S. output, 0.1% resistor cross-product match will give 0.1% x 10V. untrimmable output offset voltage.

### Resistor Values

#### Inputs:

$$V_X(\text{min.}) \leq V_X \leq V_X(\text{max.})$$

$$\Delta V_X = V_X(\text{max.}) - V_X(\text{min.})$$

$$V_Z(\text{min.}) \leq V_Z \leq V_Z(\text{max.})$$

$$\Delta V_Z = V_Z(\text{max.}) - V_Z(\text{min.})$$

$$V_{REF} = \text{Constant (+7V to +18V)}$$

#### Outputs:

$$V_0(\text{min.}) \leq V_0 \leq V_0(\text{max.})$$

$$\Delta V_0 = V_0(\text{max.}) - V_0(\text{min.})$$

$$K = \frac{V_0 V_Z}{V_X} \text{ (Design Requirement)}$$

$$R_0 = \frac{\Delta V_0}{750\mu\text{A}}, R_b = \frac{\Delta V_{REF}}{250\mu\text{A}}, R_4 = \frac{\Delta V_Z}{200\mu\text{A}}$$

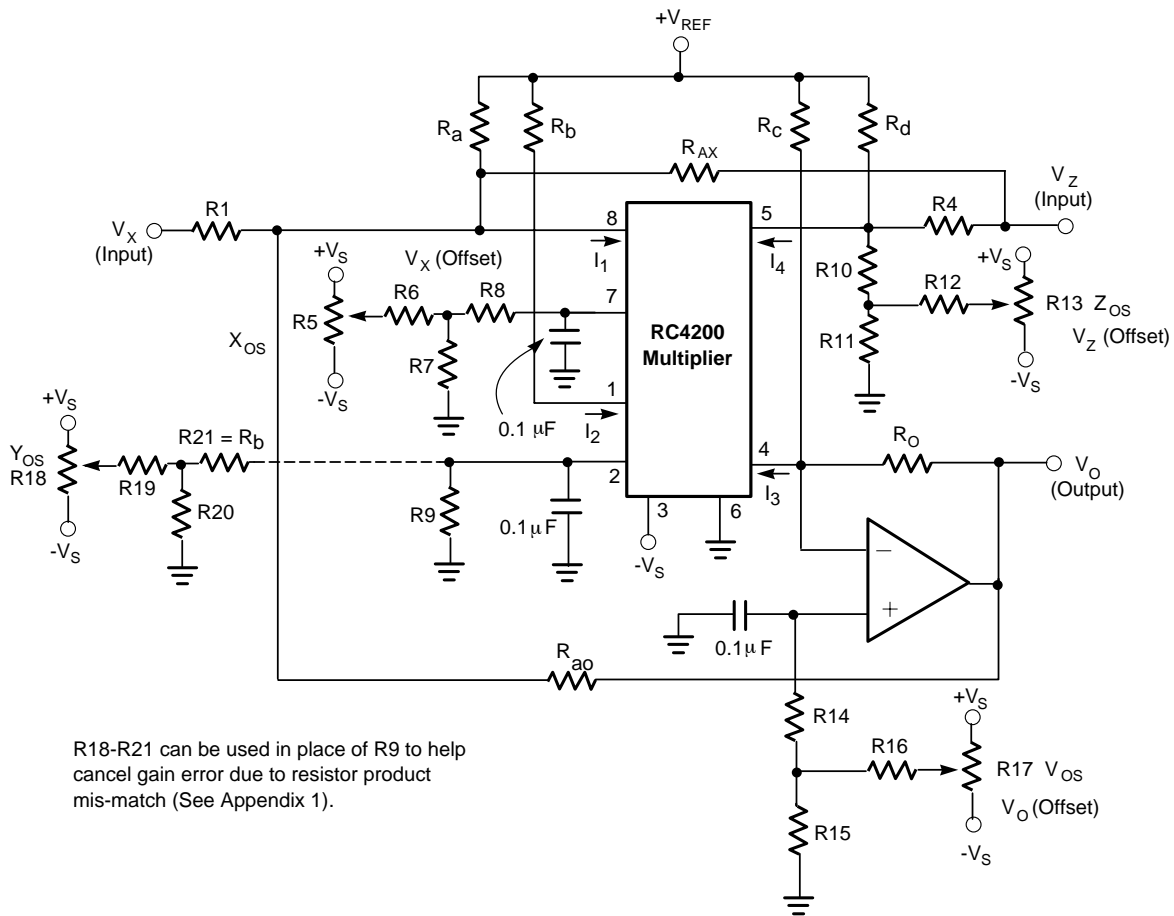
$$R_c = \frac{\Delta V_0 V_{REF}}{750\mu\text{A} \Delta V_0 - 700\mu\text{A} V_0(\text{max.})}$$

$$R_d = \frac{\Delta V_X V_{REF}}{250\mu\text{A} \Delta V_Z - 200\mu\text{A} V_Z(\text{max.})}$$

$$R_a = \frac{R_c R_d}{R_b}, R_{az} = \frac{R_c R_4}{R_b}, R_{ao} = \frac{R_0 R_d}{R_b}$$

$$R_1 = \frac{\Delta V_0 \Delta V_Z}{600\mu\text{A} K}$$

Divider Circuit with Offset Adjustment



R18-R21 can be used in place of R9 to help cancel gain error due to resistor product mis-match (See Appendix 1).

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General

- $10K \leq R5 = R13 = R17 \leq 50K$
- $R7 + R8 \approx R1 \parallel Ra \parallel Raz \parallel Rao$
- $R6 \approx R7 (Vs/0.05)$
- $R9 = Rb$
- $R10 \approx 100 \times R4$
- $R11 = 20K$
- $R12 = 100K$
- $R14 + R15 \approx R0 \parallel Rc$
- $R16 \approx R15 (Vs/0.10)$

Example: Two-Quad Divider

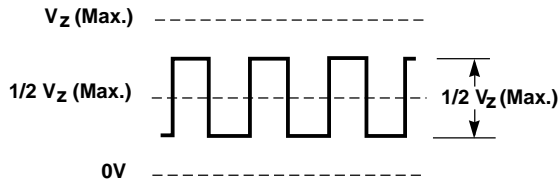
- $V0 = K(Vx/Vz), K = k, VREF = +Vs = +15V$
- $-10 \leq Vx \leq +10, \text{ therefore } \Delta Vx = 20$
- $0 \leq Vz \leq +10, \text{ therefore } \Delta Vz = 20$
- $-10 \leq V0 \leq +10, \text{ therefore } \Delta V0 = 20$
- $R0 = 26.7K$
- $R1 = 333K$
- $Rb = 60K$
- $R5, R13, R17 = 10K$
- $R4 = 50K$
- $R7, R15 = 1K$
- $Rc = 37.5K$
- $R8, R11 = 20K$
- $Rd = 300K$
- $R6, R9, R16 = 300K$
- $Ra = 187.5K$
- $R10 = 4.7M$
- $Raz = 31.25$
- $R12 = 100K$
- $Rao = 133K$

Figure 7. Divider Circuit with Offset Adjustment



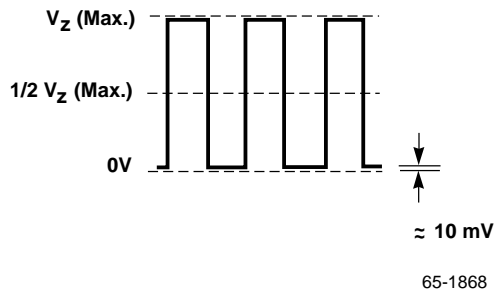
**Divider Circuit Offset Adjustment Procedure**

1. Set each trimmer pot to 0V on the wiper.
2. Connect  $V_X$  (input) to ground. Put a DC voltage of approximately  $1/2 V_Z$  (max.) DC on the  $V_Z$  (input) with an AC (squarewave is easiest) voltage of  $1/2 V_Z$  (max.) peak-to-peak superimposed on it. Adjust  $XOS$  ( $R_5$ ) for zero feedthrough. (No AC at  $V_0$ )



3. Connect  $V_X$  (input) to  $V_Z$  (input) and put in the  $1/2 V_Z$ (max.) DC with an AC of approximately 20 mV less than  $V_Z$ (max.).

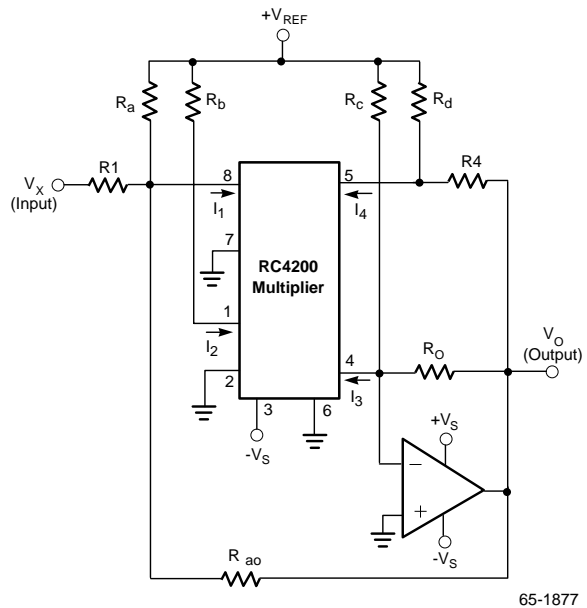
Adjust  $ZOS$  ( $R_{13}$ ) for zero feedthrough.



4. Return  $V_X$  (Input) to ground and connect  $V_Z$ (max.) DC on  $V_Z$ (input). Adjust output  $V_{OS}$ ( $R_{17}$ ) for  $V_0 = 0V_0$
5. Connect  $V_X$  (input) to  $V_Z$  (input) and and in  $V_Z$  (max.) DC. (The output will equal  $K$ .) Decrease the input slowly until the output ( $V_0 - K$ ) deviates beyond the desired accuracy. Adjust  $ZOS$  to bring it back into tolerance and return to Step 4. Continue steps 4 and 5 until  $V_Z$  reduces to the lowest value desired.

Notice that as the input to  $V_X$  and  $V_Z$  gets closer to zero (an illegal state) the system noise will predominate so much that an integrating voltmeter will be very helpful.

**Square Root Circuit  $V_0 = N\sqrt{V_X}$**



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**Figure 8.**

$$\frac{V_X V_{REF}}{R_1 R_b} + \frac{V_{REF}^2}{R_a R_b} + \frac{V_0 V_{REF}}{R_{ao} R_b} = \frac{V_0^2}{R_0 R_4} + \frac{V_0 V_{REF}}{R_c R_4} + \frac{V_0 V_{REF}}{R_0 R_d} + \frac{V_{REF}}{R_c R_d}$$

If  $R_a R_b = R_c R_d$  and  $R_{ao} R_b R_0 R_d + R_{ao} R_b R_c R_4 = R_c R_d R_0 R_4$

Then  $\frac{V_0^2}{R_0 R_4} = \frac{V_X V_{REF}}{R_1 R_b}$  or  $V_0^2 = V_X K$  where  $K = \frac{V_{REF} R_0 R_4}{R_1 R_b}$

and  $V_0 = N\sqrt{V_X}$  where  $N = \sqrt{K}$

$0 \leq V_X \leq V_X(\text{max.})$  and  $V_0(\text{max.}) = N\sqrt{V_X(\text{max.})}$

$N = \frac{V_0}{\sqrt{V_X}}$  (Design Requirements)

$R_1 = \frac{V_0(\text{max.})^2}{74\mu A N^2}$

$R_a = R_d = \frac{V_{REF}}{50\mu A}$

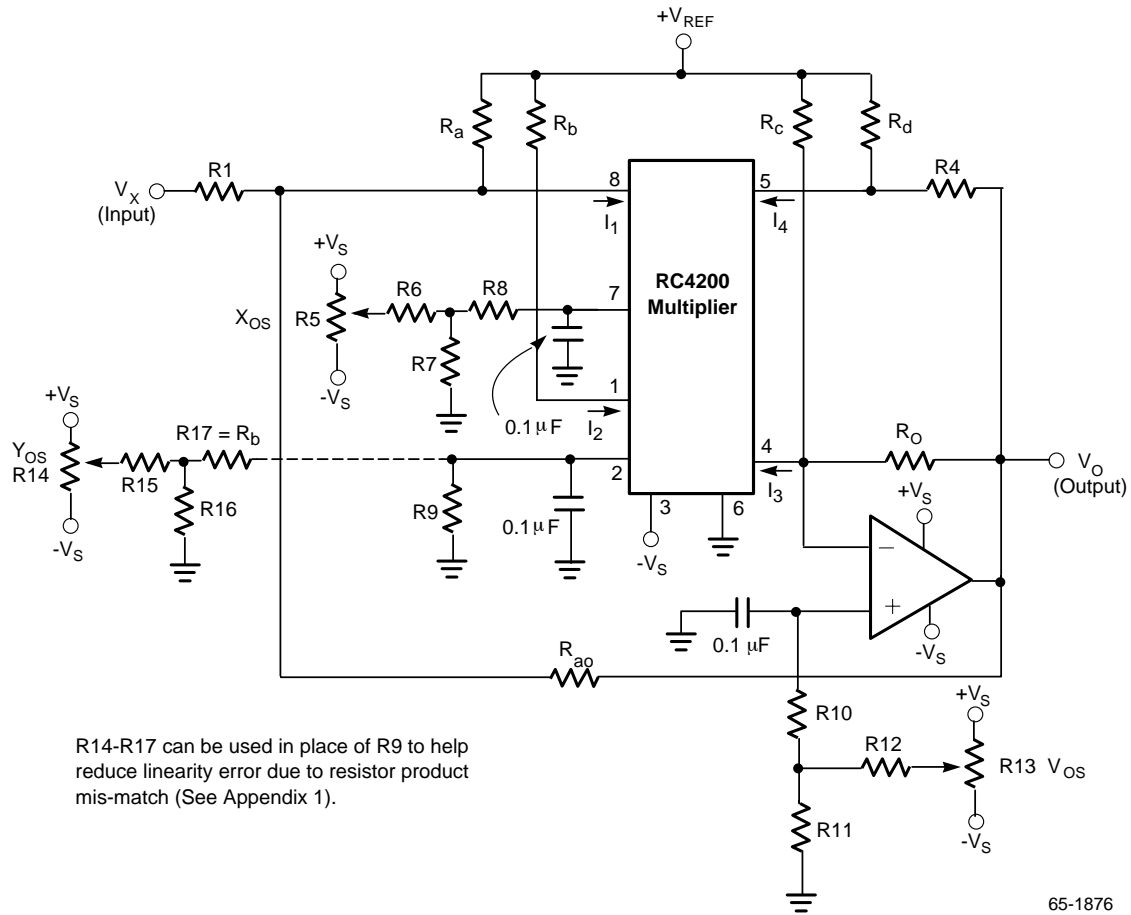
$R_b = R_c = \frac{V_{REF}}{150\mu A}$

$R_4 = \frac{V_0(\text{max.})}{50\mu A}$

$R_{ao} = \frac{V_0(\text{max.})}{125\mu A}$

$R_0 = \frac{V_0(\text{max.})}{225\mu A}$

**Square Root Circuit Offset Adjust**



**Figure 9. Square Root Circuit Offset Adjust**

$$10K \leq R_5 = R_{13} \leq 50K$$

$$R_7 = 100\Omega$$

$$R_6 = R_7 \frac{V_S}{0.05}$$

$$R_8 = R_1 \parallel R_a \parallel R_{a0}$$

$$R_9 = R_b$$

$$R_{10} = R_0 \parallel R_c$$

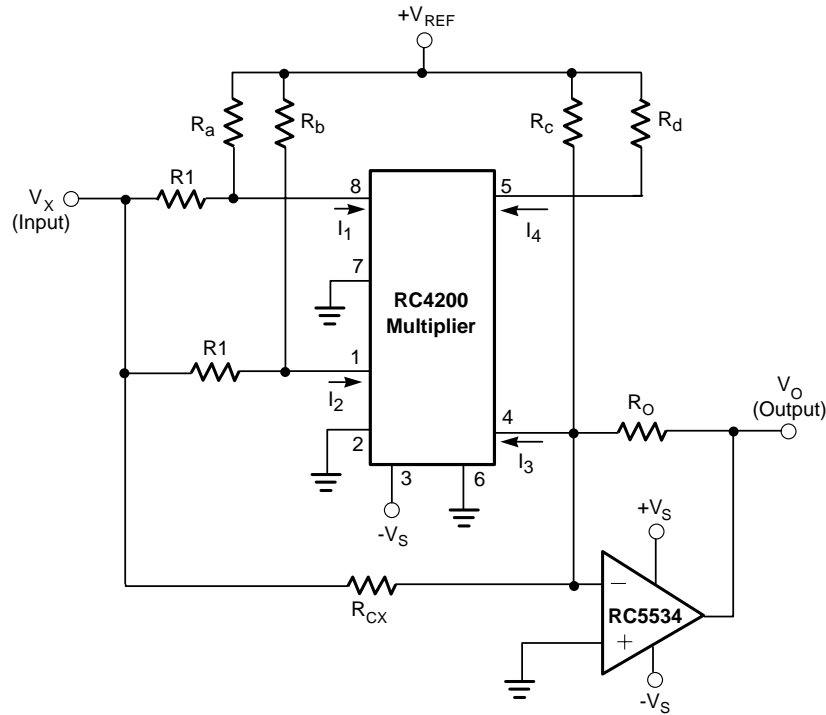
$$R_{11} = 100\Omega$$

$$R_{12} = R_{11} \frac{V_S}{0.1}$$

**Procedure**

1. Set both trimmer pots to 0V on the wiper.
2. Put in a full scale (0 to  $V_X(\text{max.})$ ) squarewave on  $V_X$  input. Adjust  $X_{OS}(R_5)$  for proper peak-to-peak amplitude on  $V_0$  output. (Scaling adjust)
3. Connect  $V_X$  input to ground. Adjust  $V_{OS}(R_{13})$  for 0V on  $V_0$  output.

**Squaring Circuits  $V_0 = K V_X^2$**



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**Figure 10. Squaring Circuit**

$$\frac{V_X^2}{R_1^2} + \frac{2V_X V_{REF}}{R_1 R_a} + \frac{V_{REF}^2}{R_a^2} = \frac{V_0 V_{REF}}{R_0 R_d} + \frac{V_{REF}^2}{R_c R_d} + \frac{V_X V_{REF}}{R_c R_d}$$

if  $R_a^2 = R_c R_d$  and  $R_1 R_a = 2R_{CX} R_D$

then  $\frac{V_0 V_{REF}}{R_0 R_d} = \frac{V_X^2}{R_1^2}$  or  $V_0 = K V_X^2$  where  $K = \frac{R_0 R_d}{V_{REF} R_1^2}$

$V_X(\text{min.}) \leq V_X \leq V_X(\text{max.}) \quad \Delta V_X = V_X(\text{max.}) - V_X(\text{min.})$

$K = \frac{V_0}{V_X^2}$  (Design Requirement)

$$R_1 = \frac{\Delta V_X}{200\mu A}$$

$$R_a = \frac{\Delta V_X V_{REF}}{250\mu A \Delta V_X - 200\mu A V_X(\text{max.})}$$

$$R_d = \frac{V_{REF}}{250\mu A}$$

$$R_c = \frac{R_a^2}{R_d}$$

$$R_{CX} = \frac{R_1 R_a}{2R_d}$$

$$R_0 = \frac{\Delta V_X^2 K}{160\mu A}$$

Squaring Circuits Offset Adjust

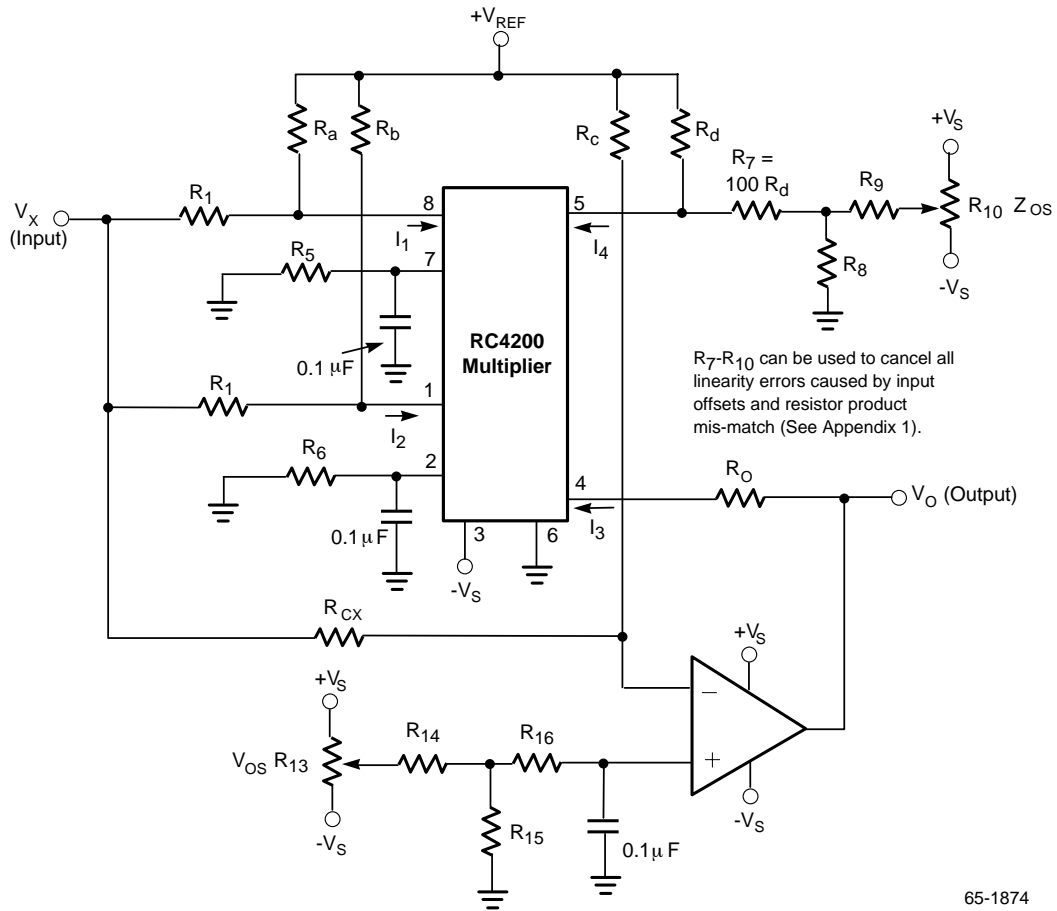


Figure 11. Squaring Circuit Offset Adjust

$$10K \leq R_{10} = R_{11} \leq 50K$$

$$R_8, R_{15} = 100\Omega$$

$$R_9, R_{14} = 100\Omega \frac{V_S}{0.1}$$

$$R_5, R_6 = R_1 \parallel R_a$$

$$R_{16} = R_0 \parallel R_c \parallel R_a$$

**Procedure**

1. 1.Set both trimmer pots to 0V on the wiper.
2. 2.Put in a full scale ( $\pm V_X$ ) squarewave on  $V_X$  input. Adjust ZOS( $R_{10}$ ) for uniform output.
3. 3.Connect  $V_X$  input to ground. Adjust  $V_{OS}$ ( $R_{11}$ ) for 0V on  $V_0$  outputs.

## Appendix 1—System Errors

There are four types of accuracy errors which affect overall system performance. They are:

- Nonlinearity—Incremental deviation from absolute accuracy. See Note 1.
- Scaling Error—Linear deviation from absolute accuracy.
- Output Offset—Constant deviation from absolute accuracy.
- Feedthrough.—Cross-product errors caused by input offsets and external circuit limitations. See Note 2.

This nonlinearity error in the transfer function of the RC4200 is  $\pm 0.1\%$  maximum ( $\pm 0.03$  maximum for the RC4200A). That is,

$$I_3 = \frac{I_1 I_2}{I_4} \pm 0.1\% \text{ F.S.}^{(4)}$$

The other system errors are caused by voltage offsets on the inputs of the RC4200 and can be as high as  $\pm 3.0\%$  ( $\pm 2.0\%$  for RC4200A).

$$V_0 = \frac{V_X V_Y}{V_Z} \frac{R_0 R_4}{R_1 R_2} \pm 3.0\% \text{ F.S.}^{(3)(4)}$$

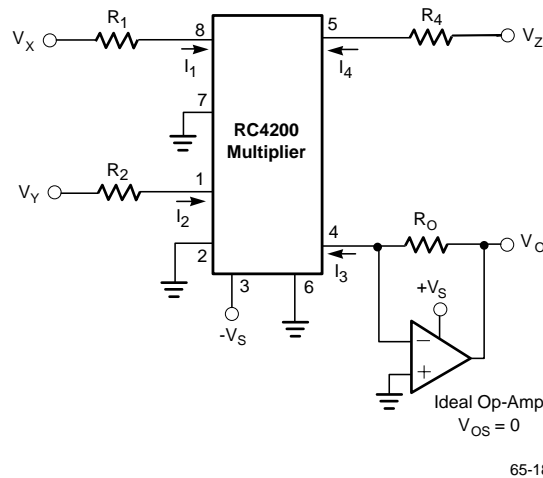


Figure 12.

**Notes:**

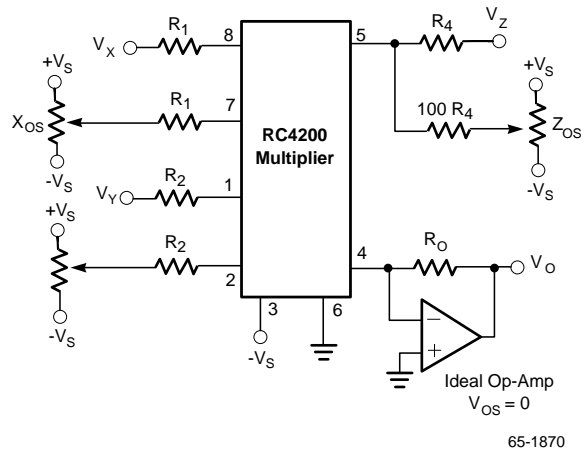
1. The input circuits tend to become unstable at  $I_1, I_2, I_4 < 50 \mu\text{A}$  and linearity decreases when  $I_1, I_2, I_4 > 250 \mu\text{A}$  (e.g., @  $I_1 = I_2 = 500 \mu\text{A}$  nonlinearity error  $\approx 0.5\%$ ).
2. This section will not deal with feedthrough which is proportional to frequency of operation and caused by stray capacitance and/or bandwidth limitations. (refer to Figure 12.)
3. Not including resistor tolerance or output offset on the operational amplifier.
4. For  $50 \mu\text{A} \leq I_1, I_2, I_4 \leq 250 \mu\text{A}$ .

## Errors Caused by Input Offsets

$$V_0 = \frac{R_0 R_4}{R_0 R_4} \left[ \frac{V_X V_Y}{V_Z} \pm \frac{1}{V_Z} \left( V_Y V_{OSX} \pm V_X V_{OSY} \pm V_0 V_{OSZ} \pm V_{OSX} V_{OSY} \right) \right]$$

$V_Y$  Feedthrough  $\rightarrow$   $V_Y V_{OSX}$   
 $V_X$  Feedthrough  $\rightarrow$   $V_X V_{OSY}$   
 Scaling Error  $\rightarrow$   $V_0 V_{OSZ}$   
 Output Offset Error  $\rightarrow$   $V_{OSX} V_{OSY}$

System errors can be greatly reduced by externally trimming the input offset voltages of the RC4200. ( $\pm 3.0\%$  F.S. for RC4200 and  $\pm 0.1\%$  for RC4200A.)



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If  $X_{OS} = X_{OSX}, Y_{OS} = Y_{OSY}, Z_{OS} = -V_{OSZ}$ ,

$$\text{then } V_0 \frac{V_X V_Y}{V_Z} \frac{R_0 R_4}{R_1 R_2} \pm 0.3\% \text{ F.S.}^{(3)}$$

Figure 13. RC4200 with Input Offset Adjustment

## Extended Range Circuit Errors

The extended range configurations have a disadvantage in that additional accuracy errors may be introduced by resistor product mismatching.

## Multiplier

An error in resistor product matching will cause an equivalent feedthrough or output offset error. See Figure 6.

$$R_1 R_b = R_C X R_d \pm \alpha, V_X \text{ feedthrough } (V_Y = 0) = I \alpha V_X$$

$$R_2 R_a = R_C Y R_d \pm \beta, V_Y \text{ feedthrough } (V_X = 0) = \pm \beta V_Y$$

$$R_a R_b = R_C R_d \pm \gamma, V_0 \text{ offset } (V_X = V_Y = 0) = \pm \gamma V_{REF}^*$$

**Note:**

\* Output offset errors can always be trimmed out with the output op amp offset adjust,  $V_{OS}$  (R16).

## Reducing Mismatch Errors

You need not use 0.01% resistors to reduce resistor product mismatch errors. Here are a couple of ways to obtain maximum accuracy out of the extended range multiplier (see Figure 4) using 1% resistors.

### Method 1

$V_X$  feedthrough, for example, occurs when  $V_Y = 0$  and  $V_{OSY} \neq 0$ . This  $V_X$  feedthrough will equal  $\pm V_X V_{OSY}$ . Also, if  $V_{OSZ} \neq 0$ , there is a  $V_X$  feedthrough equal to  $V_X V_{OSZ}$ . A resistor-product error of  $\alpha$  will cause a  $V_X$  feedthrough of  $\pm \alpha V_X$ . Likewise,  $V_Y$  feedthrough errors are:  $\pm V_Y V_{OSX}$ ,  $\pm V_Y V_{OSZ}$  and  $\pm \beta V_Y$

Total feedthrough:

$$\pm V_X V_{OSY} \pm V_Y V_{OSX} \pm \alpha V_X \pm \beta V_Y \pm (V_X + V_Y) V_{OSZ}$$

By carefully abusing  $X_{OS}(R5)$ ,  $Y_{OS}(R9)$  and  $Z_{OS}(R20)$  this equation can be made to very nearly equal zero and the feedthrough error will practically disappear.

A residual of set will probably remain which can be trimmed out with  $V_{OS}(R16)$  at the output of amp.

### Method 2

Notice that the ratios of  $R_1 R_b : R_C X R_d$  and  $R_2 R_a : R_C Y R_d$  are both dependent of  $R_d$  also that  $R_1$ ,  $R_2$ ,  $R_a$  and  $R_b$  are all functions of the maximum input requirements. By designing a multiplier for the same input ranges on both  $V_X$  and  $V_Y$  then  $R_1 = R_2$ ,  $R_C X = R_C Y$  and  $R_a = R_b$ . (Note: it is acceptable to design a four quadrant multiplier and use only two quadrants of it.)

Select  $R_d$  to be 1% or 2% below (or above) the calculated value. This will cause  $\alpha$  and  $\beta$  to both be positive (or negative) by nearly the same amount. Now the effective value of  $R_d$  can be trimmed with an offset adjustment  $Z_{OS}(R20)$  on pin 5.

This technique causes: a slight gain error which can be compensated with the  $R_0$  value, and an output of offset error that can be trimmed with  $V_{OS}(R16)$  on the output op amp.

## Extended Range Divider

The only cross-product error of interest is the  $V_Z$  feedthrough ( $V_X = 0$  and  $V_{OSX} \neq 0$ ) which is easily adjusted with  $X_{OS}(R5)$ . See Figure 6.

Resistor product mismatch will cause scaling errors (gain) that could be a problem for very low values of  $V_Z$ . Adjustments to  $Y_{OS}(R18)$  can be made to improve the high gain accuracy.

## Square Root and Squaring

These circuits are functions of single variables so feedthrough, as such, is not a consideration. Cross product errors will effect incremental accuracy that can be corrected  $Y_{OS}(R14)$  or  $Z_{OS}(R10)$ . See Figure 9 and Figure 11.

## Appendix 2—Applications

### Design Considerations for RMS-to-DC Circuits

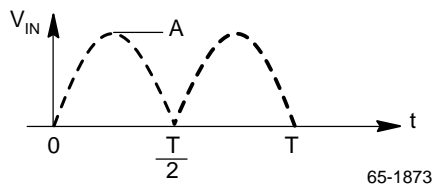
#### Average Value

Consider  $V_{in} = A \sin \omega t$ . By definition,

$$V_{AG} = \int_0^T V_{IN} dt$$

Where T = Period

$$\begin{aligned} \omega &= 2\pi f \\ &= \frac{2\pi}{T} \end{aligned}$$



$$V_{AG} = \frac{2}{T} \int_0^T A \sin \omega t dt$$

$$\begin{aligned} &= \frac{2A}{T} \left[ -\frac{1}{\omega} \cos \omega t \right]_0^T \\ &= \frac{2A}{2\pi} [-\cos(\pi) + \cos(0)] \end{aligned}$$

Average Value of  $A \sin \omega t$  is  $\frac{2}{\pi} A$

#### RMS Value

Again, consider  $V_{IN} = A \sin \omega t$

$$V_{rms} = \sqrt{V_{AVG}} = \sqrt{\frac{1}{T} \int_0^T [V_{IN}]^2 dt}$$

$V_{rms}$  for  $A \sin \omega t$ :

$$V_{rms} = \sqrt{\frac{1}{T} \int_0^T A^2 \sin^2 \omega t dt}$$

$$V_{rms} = \sqrt{\frac{A^2}{T} \int_0^T \left[ \frac{1}{2} - \frac{1}{2} \cos 2 \omega t \right] dt}$$

$$V_{rms} = \sqrt{\frac{A^2}{2} \left[ \frac{T}{2} - \frac{1}{4\omega} \sin 2 \omega t \right]_0^T}$$

$$V_{rms} = \sqrt{\frac{A^2}{2} \left[ \frac{T}{2} \right]}$$

$$V_{rms} = \sqrt{\frac{A^2}{2}}$$

Therefore, the rms value of  $A \sin \omega t$  becomes:

$$V_{rms} = \frac{A}{\sqrt{2}}$$

#### RMS Value for Rectified Sine Waves

Consider  $V_{in} = |A \sin \omega t|$ , a rectified wave. To solve, integrate of each half cycle.

i.e.  $\frac{1}{T} \int_0^T V_{in}^2 dt =$

$$\frac{1}{T} \left[ \int_0^{\frac{T}{2}} A^2 \sin^2 \omega t dt + \int_{\frac{T}{2}}^T (-A \sin \omega t)^2 dt \right]$$

This is the same as  $\frac{1}{T} \int_0^T A^2 \sin^2 \omega t dt$

so,  $|A \sin \omega t|_{rms} = A \sin \omega t_{rms}$

Practical Consideration:  $|A \sin \omega t|$  has high-order harmonics;  $A \sin \omega t$  does not. Therefore, non-ideal integrators may cause different errors for two approaches.

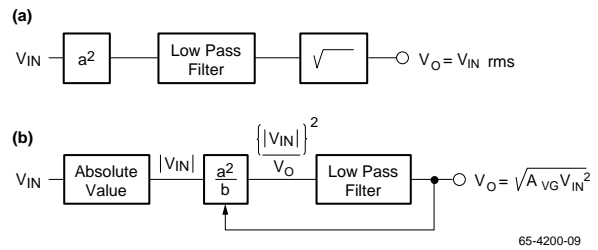
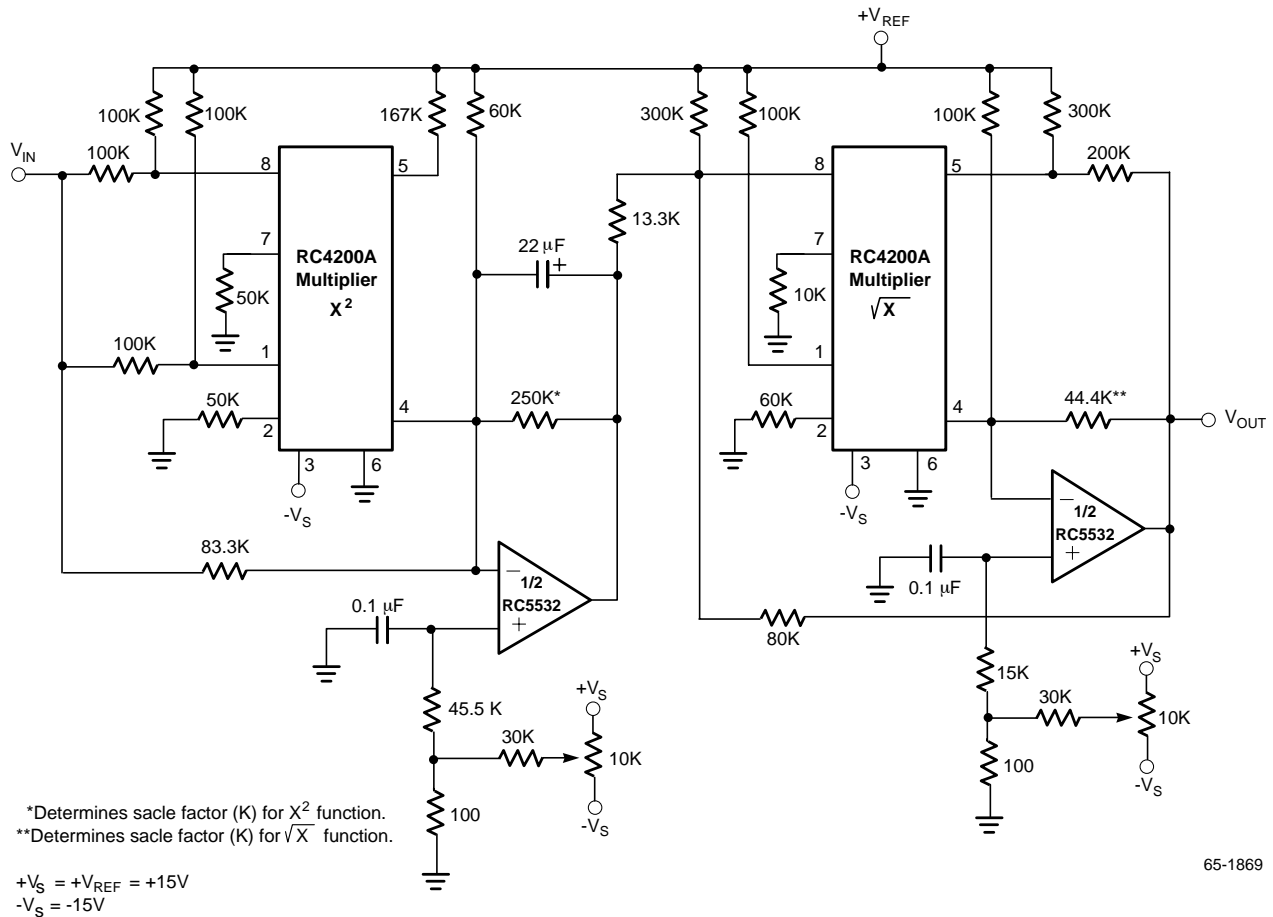


Figure 14.

$$Avg \left[ \frac{V_{IN}^2}{V_0} \right] = V_0$$

implies  $V_0 = \sqrt{Avg(|V_{IN}^2|)}$

$$V_0 = \sqrt{Avg V_{IN}^2}$$



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Figure 15. RMS to DC Converter V<sub>OUT</sub>=√V<sub>IN</sub><sup>2</sup>

**Amplitude Modulator with A.G.C.**

In many AC modulator applications, unwanted output modulation is caused by variations in carrier input amplitude. The versatility of the RC4200 multiplier can be utilized to eliminate this undesired fluctuation. The extended range multiplier circuit (Figure 4) shows an output amplitude inversely proportional to the reference voltage V<sub>REF</sub>.

$$\text{i.e., } V_0 = \frac{V_X V_Y}{V_{REF}} \frac{R_0 R_d}{R_1 R_2}$$

By making V<sub>REF</sub> proportional to V<sub>Y</sub> (where V<sub>Y</sub> is the carrier input) such that:

$$V_{REF} = V_H = \int(|V_Y|)$$

Then the denominator becomes a variable value that automatically provides constant gain, such that the modulating input (V<sub>X</sub>) modulates the carrier (V<sub>Y</sub>) with a fixed scale factor even though the carrier varies in amplitude.

If V<sub>H</sub> is made proportional to the average value of A sin ωt (i.e., 2A/π) and scaled by a value of π/2 then:

$$V_H = A$$

and if: V<sub>X</sub> = Modulating input (V<sub>M</sub>)

and: V<sub>Y</sub> Carrier input (A sin ωt)

$$\text{Then: } V_0 = K V_M \sin \omega t \text{ where } K = \frac{R_0 R_d}{R_1 R_2}$$

The resistor scaling is determined by the dynamic range of the carrier variation and modulating input.

The resistor values are solved, as with the other extended range circuits, in terms of the input voltages.

Input voltages:

Modulation voltage (V<sub>M</sub>): 0 ≤ V<sub>M</sub> ≤ V<sub>X</sub>(max.)

Carrier (V<sub>Y</sub>): V<sub>Y</sub> = A sin ωt

Carrier amplitude fluctuation (ΔA):

$$A(\text{min.}) \sin t \leq V_Y \leq A(\text{max.}) \sin \Omega \omega t$$

Dynamic Range (N): A(max.)/A(min.),

$$A(\text{max.}) = V_H(\text{max.}) \text{ and } A(\text{min.}) = V_H(\text{min.})$$



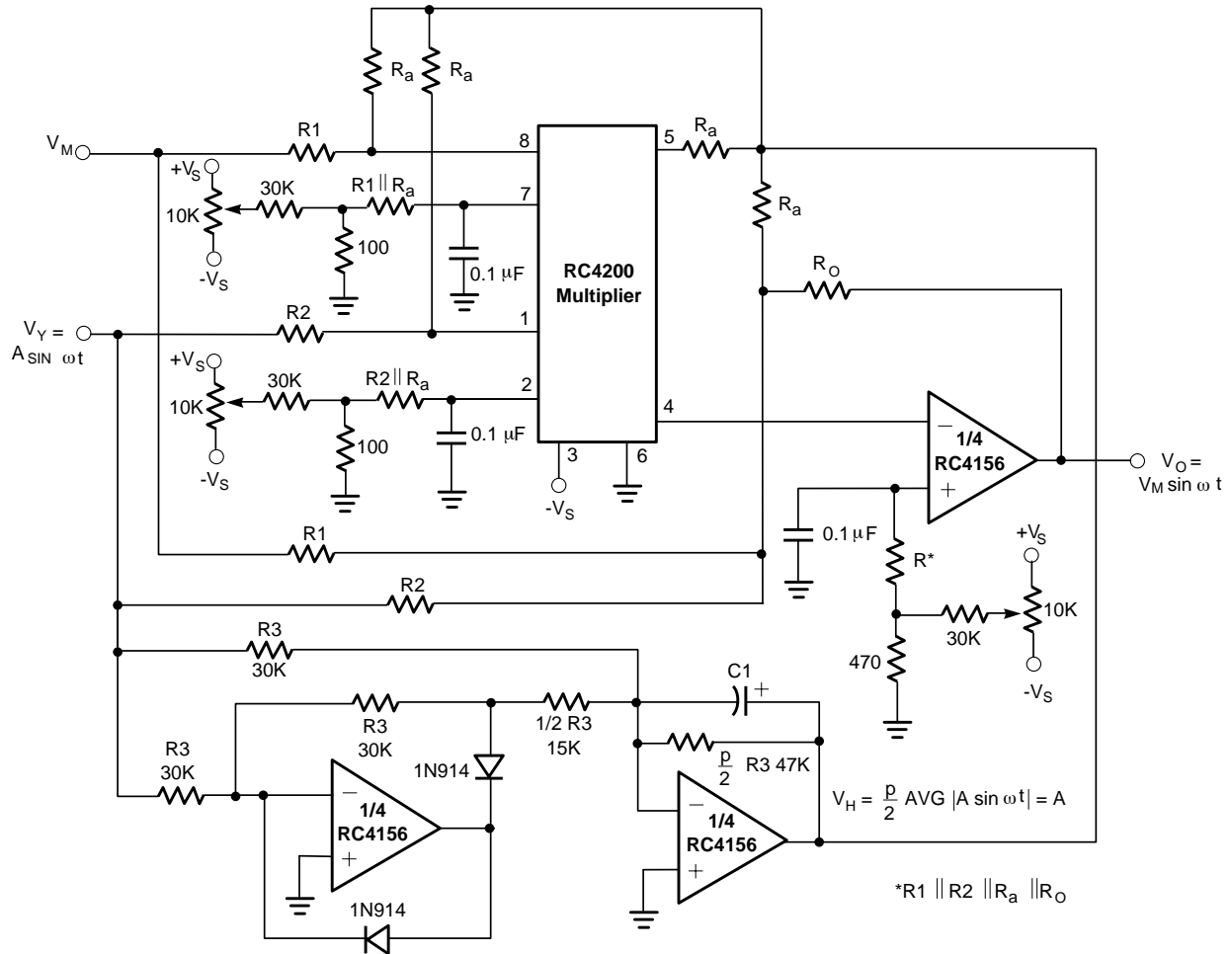


Figure 16. Amplitude Modulator with A.G.C.

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The maximum and minimum values for I<sub>1</sub> and I<sub>2</sub> lead to:

$$I_1(\text{max.}) = \frac{V_X(\text{max.})}{R_1} + \frac{V_H(\text{max.})}{R_a} = 250\mu\text{A}$$

$$I_1(\text{min.}) = \frac{V_H(\text{min.})}{R_a} = 50\mu\text{A} \quad V_M(\text{min.}) = 0$$

$$I_2(\text{max.}) = \frac{A(\text{max.})}{R_2} + \frac{V_H(\text{max.})}{R_a} = 250\mu\text{A}$$

$$I_2(\text{min.}) = \frac{V_H(\text{min.})}{R_a} = 50\mu\text{A}$$

For a dynamic range of N, where

$$N = \frac{A(\text{max.})}{A(\text{min.})} < 5,$$

These equations combine to yield:

$$R_1 = \frac{V_X(\text{max.})}{(5-N)50\mu\text{A}}, \quad R_2 = \frac{A(\text{max.})}{(5-N)50\mu\text{A}},$$

$$R_a = \frac{A(\text{min.})}{50\mu\text{A}} \quad \text{and} \quad R_O = K \frac{R_1 R_2}{R_a}$$

**Example 1**

$V_Y = A \sin \omega t$   $2.5\text{V} \leq A \leq 10\text{V}$ , therefore  $N = 4$   
 $0\text{V} \leq V_M \leq 10\text{V}$ , therefore  $V_X(\text{max.}) = 10\text{V}$   
 $K = 1$ , therefore  $V_O = V_M \sin \omega t$

$$R_1 = \frac{V_X(\text{max.})}{50\mu\text{A}} = \frac{10\text{V}}{50\mu\text{A}} = 200\text{K}$$

$$R_1 = \frac{A(\text{max.})}{50\mu\text{A}} = \frac{10\text{V}}{50\mu\text{A}} = 200\text{K}$$

$$R_a = \frac{A(\text{min.})}{50\mu\text{A}} = \frac{2.5\text{V}}{50\mu\text{A}} = 50\text{K}$$

$$R_O = K \frac{R_1 R_2}{R_a} = 1 \frac{200\text{K} \times 200\text{K}}{50\text{K}} = 800\text{K}$$

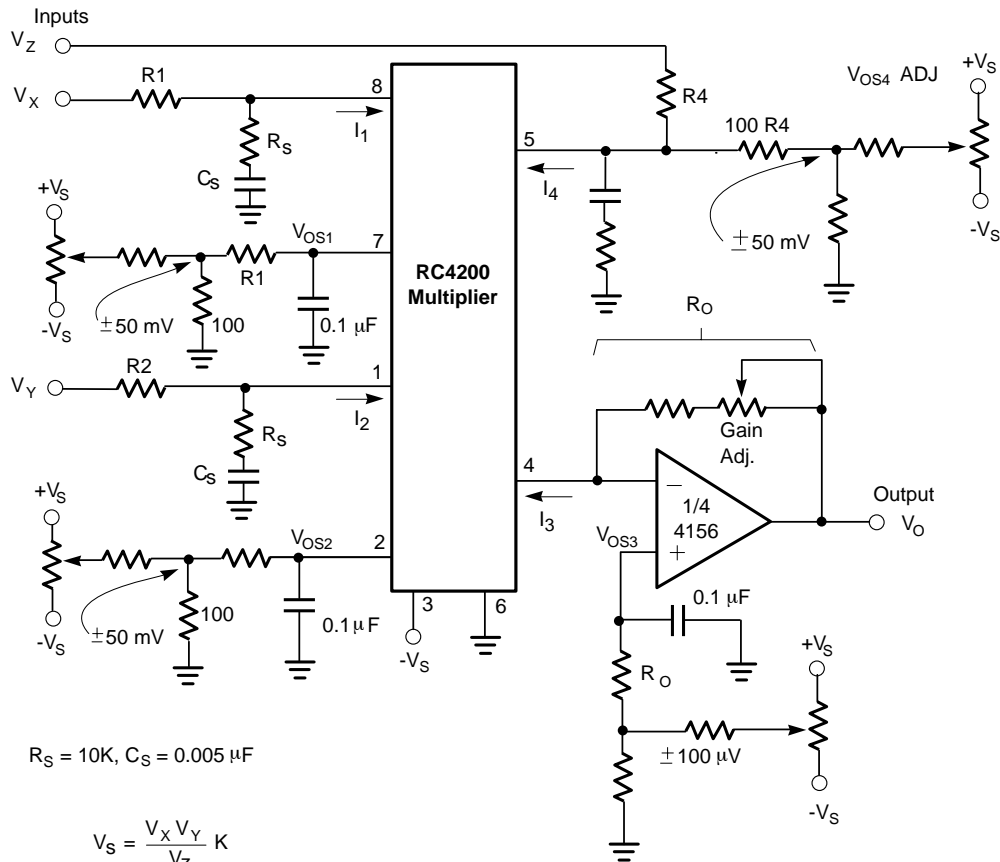
**Example 2**

$V_Y = A \sin \omega t$   $3 \leq A \leq 6$ , therefore  $N = 2$   
 $0\text{V} \leq V_M \leq 8\text{V}$ , therefore  $V_X(\text{max.}) = 8\text{V}$   
 $K = 0.2$ , therefore  $V_O = 0.2 V_M \sin \omega t$

so:

$$R_1 = 53.3\text{K}, \quad R_2 = 40\text{K}$$

$$R_a = 60\text{K} \quad \text{and} \quad R_O = 7.11\text{K}$$



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### Limited Range, First Quadrant Applications

The following circuit has the advantage that cross-product errors are due only to input offsets and nonlinearity error is slightly less for lower input currents.

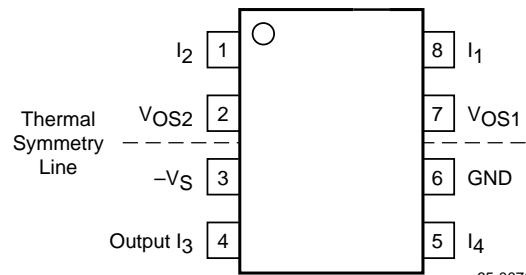
The circuit also has no standby current to add to the noise content, although the signal-to-noise ratio worsens at very low input currents (1-5  $\mu A$ ) due to the noise current of the input stages.

The RSCS filter circuits are added to each input to improve the stability for input currents below 50  $\mu A$ .

### Caution!

The bandpass drops off significantly for lower currents (<50  $\mu A$ ) and non-symmetrical rise and fall times can cause second harmonic distortion.

### Thermal Symmetry



The scale factor is sensitive to temperature gradients across the chip in the lateral direction. Where possible, the package should be oriented such that forces generating temperature gradients are located physically on the line of thermal symmetry. This will minimize scale-factor error due to thermal gradients.

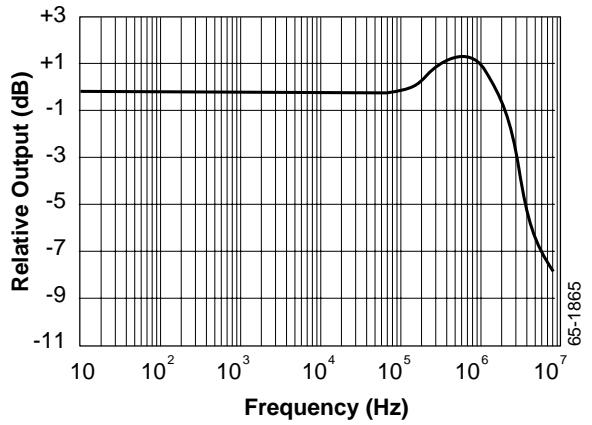
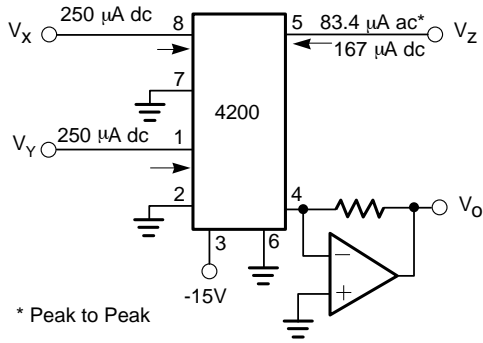
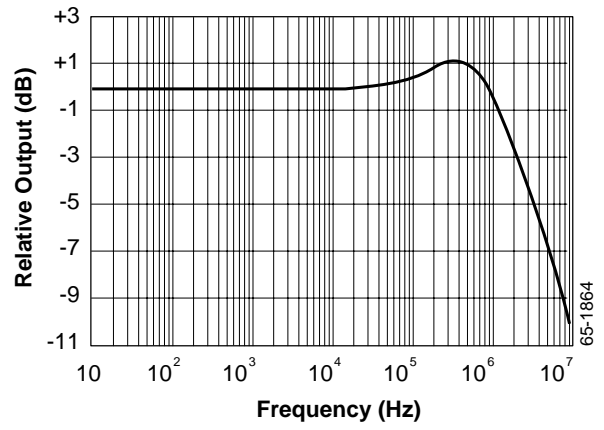
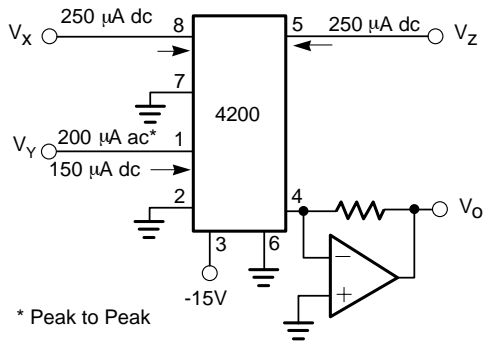
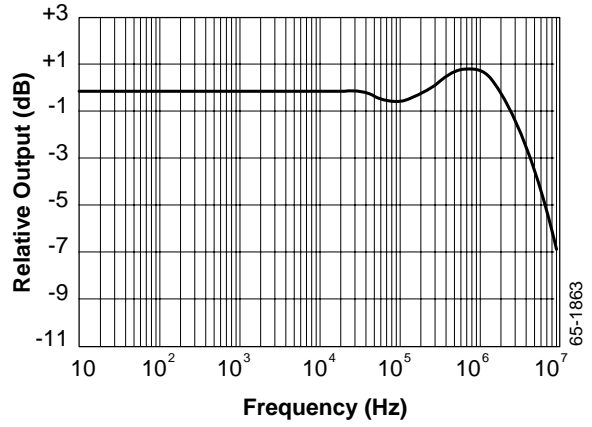
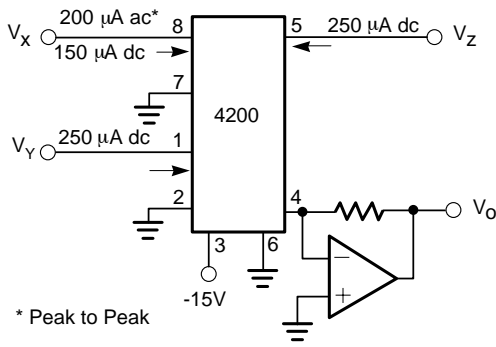


Figure 18. Outputs

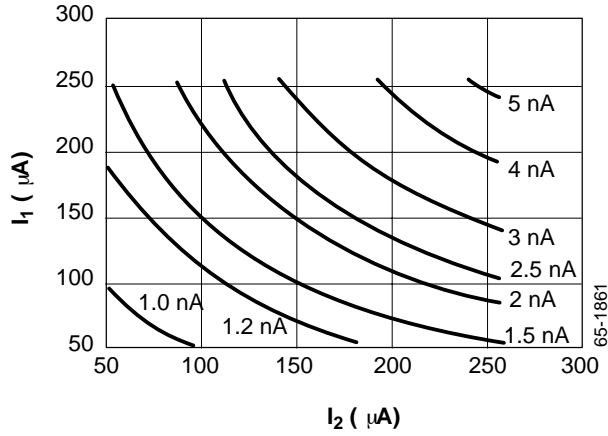


Figure 19a. Output Noise Current (I<sub>3</sub>) vs. Input Currents (I<sub>1</sub>, I<sub>2</sub>) for I<sub>4</sub> = 250µA

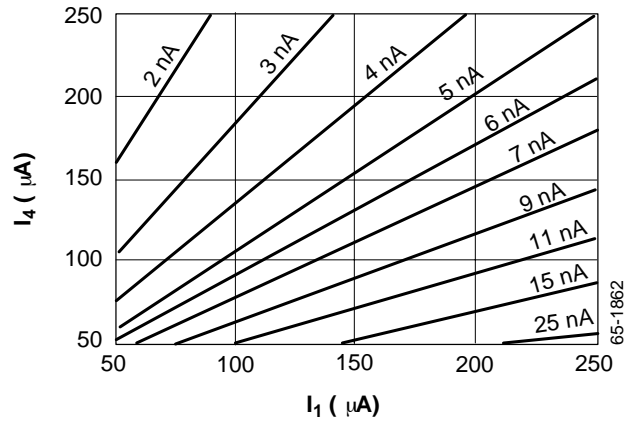


Figure 19b. Output Noise Current (I<sub>3</sub>) vs. Input Currents (I<sub>4</sub>, I<sub>1</sub>) for I<sub>2</sub> = 250µA

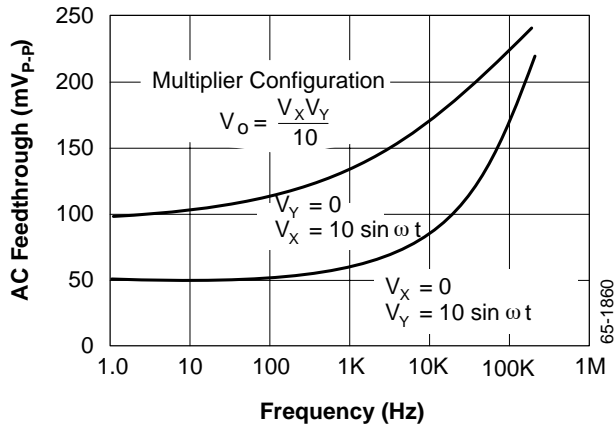


Figure 20. AC Feedthrough vs. Frequency

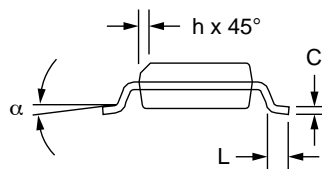
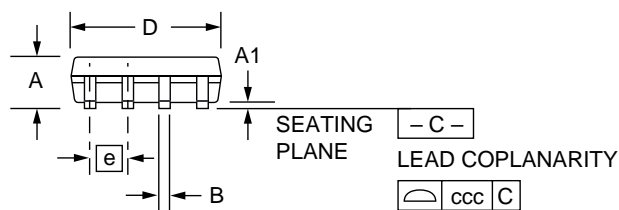
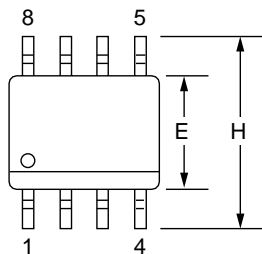
# Mechanical Dimensions

## 8-Lead SOIC Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.053	.069	1.35	1.75	
A1	.004	.010	0.10	0.25	
B	.013	.020	0.33	0.51	
C	.008	.010	0.20	0.25	5
D	.189	.197	4.80	5.00	2
E	.150	.158	3.81	4.01	2
e	.050 BSC		1.27 BSC		
H	.228	.244	5.79	6.20	
h	.010	.020	0.25	0.50	
L	.016	.050	0.40	1.27	3
N	8		8		6
$\alpha$	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

**Notes:**

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.



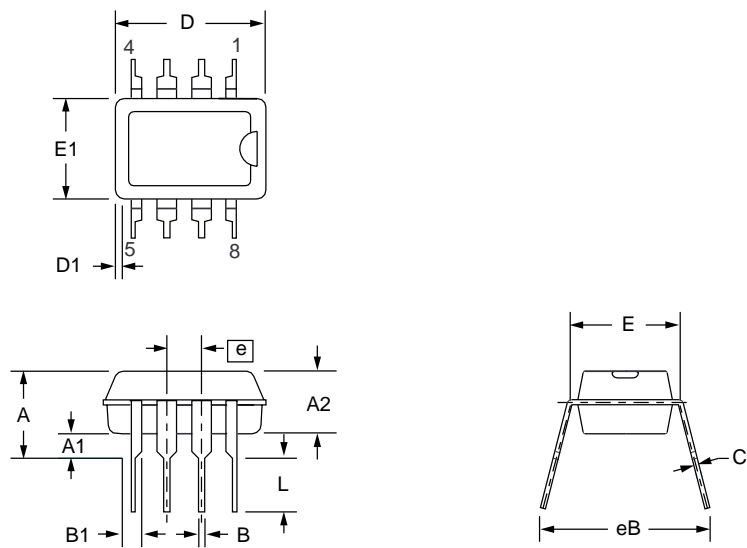
# Mechanical Dimensions (continued)

## 8-Lead Plastic DIP Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.210	—	5.33	
A1	.015	—	.38	—	
A2	.115	.195	2.93	4.95	
B	.014	.022	.36	.56	
B1	.045	.070	1.14	1.78	
C	.008	.015	.20	.38	4
D	.348	.430	8.84	10.92	2
D1	.005	—	.13	—	
E	.300	.325	7.62	8.26	
E1	.240	.280	6.10	7.11	2
e	.100 BSC		2.54 BSC		
eB	—	.430	—	10.92	
L	.115	.160	2.92	4.06	
N	8°		8°		5

**Notes:**

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E1" do not include mold flashing. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. Terminal numbers are for reference only.
4. "C" dimension does not include solder finish thickness.
5. Symbol "N" is the maximum number of terminals.



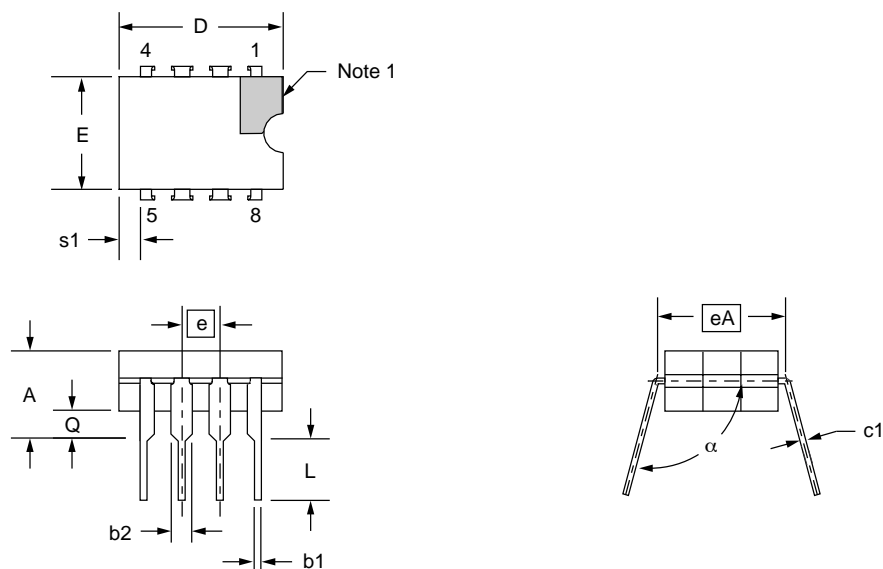
# Mechanical Dimensions (continued)

## 8-Lead Ceramic DIP Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.200	—	5.08	
b1	.014	.023	.36	.58	8
b2	.045	.065	1.14	1.65	2, 8
c1	.008	.015	.20	.38	8
D	—	.405	—	10.29	4
E	.220	.310	5.59	7.87	4
e	.100 BSC		2.54 BSC		5, 9
eA	.300 BSC		7.62 BSC		7
L	.125	.200	3.18	5.08	
Q	.015	.060	.38	1.52	3
s1	.005	—	.13	—	6
$\alpha$	90°	105°	90°	105°	

**Notes:**

1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
2. The minimum limit for dimension "b2" may be .023 (.58mm) for leads number 1, 4, 5 and 8 only.
3. Dimension "Q" shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within  $\pm .010$  (.25mm) of its exact longitudinal position relative to pins 1 and 8.
6. Applies to all four corners (leads number 1, 4, 5, and 8).
7. "eA" shall be measured at the center of the lead bends or at the centerline of the leads when " $\alpha$ " is 90°.
8. All leads – Increase maximum limit by .003 (.08mm) measured at the center of the flat, when lead finish applied.
9. Six spaces.



## Ordering Information

Part Number	Package	Operating Temperature Range
RC4200N	8-Lead Plastic DIP	0°C to +70°C
RC4200AN	8-Lead Plastic DIP	0°C to +70°C
RC4200M	8-Lead SOIC	0°C to +70°C
RC4200AM	8-Lead SOIC	0°C to +70°C
RM4200D	8-Lead Ceramic DIP	-55°C to +125°C
RM4200AD	8-Lead Ceramic DIP	-55°C to +125°C
RM4200AD/883B	8-Lead Ceramic DIP	-55°C to +125°C

**Note:**

/883B suffix denotes MIL-STD-883, Level B processing

### LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.