

$PIC12C50(X) \rightarrow PIC12C50(X)A$ Migration

DEVICE MIGRATIONS

This document is intended to describe the functional differences and the electrical specification differences that are present when migrating from one device to the next.

Note: This device has been designed to perform to the parameters of its data sheet. It has been tested to an electrical specification designed to determine its conformance with these parameters. Due to process differences in the manufacture of this device, this device may have different performance characteristics than its earlier version. These differences may cause this device to perform differently in your application than the earlier version of this device.

Table 1 shows the considerations that must be taken into account when migrating from the PIC12C50(X) to the PIC12C50(X)A.

TABLE 1: PIC12C50(X) → PIC12C50(X)A DIFFERENCES

Functional Differences								
No.	Difference	H/W	S/W	Prog.				
1	The OSCCAL register has changed.	✓		_				

Note: If you change from one device to another device, please verify oscillator characteristics in your application.

Parm. No.	Sym.	Characteristic	PIC12C50(X) Data Sheet			PIC12C50(X)A Data Sheet					
			Min	Тур	Max	Min	Тур	Max	Units	Conditions	
	VDD	Supply Voltage									
		'''	2.5	_	5.5	3.0	_	5.5	V	Com., Industrial	
			3.0	_	5.5	3.0	_	5.5	V	Extended	
	IDD	Supply Current									
		XT and EXTRC options	_	0.78	2.4	_	0.8	1.4	mA	(Note 1)	
		INTRC option	_	1.1	2.4	_	0.8	1.4	mA	(Note 2)	
		LP Option	_	10	27	_	19	27	μΑ	(Note 3)	
		LP Option	_	14	35	_	19	35	μA	(Note 4)	
		LP Option	_	14	35	_	30	55	μA	(Note 5)	
	IPD	Power-down Current								VDD = 3.0V	
		Extended	_	2.0	18	_	2.0	12	μΑ	WDT disabled	
	Δ lwdt										
		Commercial	_	3.75	8	_	2.2	5	μA	VDD = 3.0V	
		Industrial	_	3.75	9	_	2.2	6	μA	VDD = 3.0V	
		Extended	_	3.75	14	_	4	11	μΑ	VDD = 3.0V	
	VIL	Input Low Voltage									
		I/O Ports									
		with Schmitt Trigger	Vss	_	0.15 VDD	Vss	_	0.2 VDD	V		
		MCLR, GP2, T0CKI	Vss	_	0.15 VDD	Vss	_	0.2 VDD	V		
		OSC1 (EXTRC)	Vss	_	0.15 VDD	Vss	_	0.2 VDD	V		
	VIH	Input High Voltage									
		I/O Ports									
		with Schmitt Trigger	0.85 VDD	_	VDD	0.85 VDD		VDD	V	For all VDD	
		MCLR, GP2, T0CKI	0.85 VDD	_	VDD	0.85 VDD	_	VDD	V		
		OSC1 (EXTRC mode)	0.85 VDD	_	VDD	0.9 VDD	_	VDD	V		
	lı∟	Input Leakage Current									
		I/O Ports	-1	0.5	±1	-	_	±1	μΑ	$Vss \leq Vpin \leq Vdd$,	
										Pin at hi-impedan	
		MCLR, GP2, T0CKI	20	130	250	_	_	_	μΑ	VPIN = VSS + 0.25	
				0.5	+5	<u> </u>	_	±5	μΑ	VPIN = VDD	
		OSC1	-3	0.5	+3	_	_	±5	μΑ	$Vss \le Vpin \le Vdd$	

Note 1: Fosc = 4.0MHz, VDD = 5.5V

^{2:} Fosc = 20MHz, VDD = 5.5V

^{3:} FOSC = 32kHz, VDD = 3.0V, WDT disabled, Commercial Temperature

^{4:} FOSC = 32kHz, VDD = 3.0V, WDT disabled, Industrial Temperature

^{5:} FOSC = 32kHz, VDD = 3.0V, WDT disabled, Extended Temperature

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- The PICmicro family meets the specifications contained in the Microchip Data Sheet.
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