Signetics

PCF8583

256 × 8-Bit Static RAM with Alarm Clock/Calendar

Preliminary Specification

Linear Products

DESCRIPTION

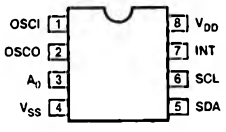
The PCF8583 is a low-power 2048-bit static CMOS RAM organized as 256 words by 8 bits. Addresses and data are transferred serially via a two-line bidirectional bus (I^2C). The built-in word address register is incremented automatically after each written or read data byte. One address pin, A_0, is used for programming the hardware address, allowing the connection of two devices to the bus without additional hardware. The built-in 32,768kHz oscillator circuit and the first 8 bytes of the RAM are used for the clock/calendar and counter functions. The next 8 bytes may be programmed as alarm registers or used as free RAM space.

FEATURES

- **I^2C bus interface operating supply voltage: 2.5V to 6V**
- **Clock operating supply voltage (0 to 70°C): 1.0V to 6V**
- **Data retention voltage: 1.0V to 6V**
- **Low standby current: max. 15μA**
- **Clock function with four-year calendar**
- **24 or 12 hour format**
- **32,768kHz or 50Hz time base**
- **Serial input/output bus (I^2C)**
- **Automatic word address incrementing.**
- **Programmable alarm, timer, and interrupt function**

PIN CONFIGURATION

N, D Packages



TOP VIEW

CD12820S

PIN NO.	SYMBOL	DESCRIPTION
1	OSCI	Oscillator input, 50Hz or event-pulse input
2	OSCO	Oscillator output
3	A_0	Address input
4	V_{SS}	Negative supply
5	SDA	Serial dataline (I^2C bus)
6	SCL	Serial clock line (I^2C bus)
7	INT	Open-drain interrupt output (Active-Low)
8	V_{DD}	Positive supply

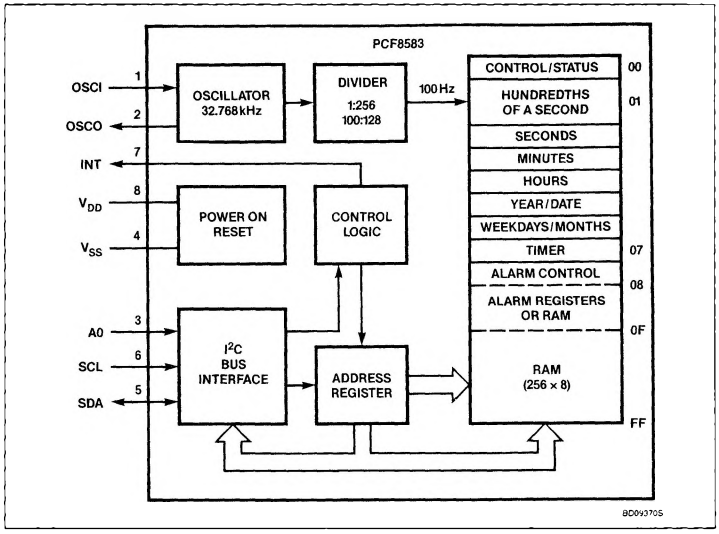
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP (SOT-97A)	−40°C to +85°C	PCF8583PN
8-Pin Plastic SO package (SO-8L, SOT-176)	−40°C to +85°C	PCF8583TD

APPLICATIONS

- **Instrumentation**
- **White goods**
- **Brown goods**
- **Products with time-dependent functions**

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Supply voltage range (Pin 8)[1]	−0.8 to 8.0	V
V_I	Voltage range on any input	−0.8 to V_{DD} + 0.8	V
I_I	DC input current (any input)	10	mA
I_O	DC output current (any output)[1]	10	mA
I_{DD}; I_{SS}	Supply current (Pin 4 or Pin 8)	50	mA
P_D	Power dissipation per package	300	mW
P_O	Power dissipation per output	50	mW
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	−40 to +85	°C

NOTE:
1. Inputs and outputs are protected against discharges in normal handling. However, to be totally safe, it is advised to take handling precautions appropriate to handling MOS devices.

DC ELECTRICAL CHARACTERISTICS V_{DD} = 2.0 to 6.0V; V_{SS} = 0V; T_A = −40°C to +85°C, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supply					
V_{DD}	Supply voltage (operating)	2.5		6	V
V_{DD}	Supply voltage (clock)	1.0		6	V
I_{DD}	Supply current T_A = 0 to +70°C operating at f_{SCL} = 100kHz			200	μA
I_{DDO}	Clock at V_{DD} = 5V		10	50	μA
I_{DDO}	Clock at V_{DD} = 1V		2	10	μA
V_{POR}	Power-on reset voltage level[1]	1.5	1.9	2.3	V
Inputs; input/output SDA					
V_{IL}	Input voltage Low[2]	−0.8		0.3 × V_{DD}	V
V_{IH}	Input voltage High[2]	0.7 × V_{DD}		V_{DD} + 0.8	V
I_{OL}	Output current Low at V_{OL} = 0.4V	3			V
I_{OH}	Output leakage current High at V_{OH} = V_{DD}			250	nA
± I_I	Input leakage current at V_I = V_{DD} or V_{SS}			250	nA
C_I	Input capacitance (SCL, SDA) at V_I = V_{SS}			7	pF
Low V_{DD} data retention					
V_{DDR}	Supply voltage for data retention	1		6	V
I_{DDR}	Supply current at V_{DDR} = 1V[3]			5	μA
I_{DDR}	Supply current at V_{DDR} = 1V; T_A = −25°C to +70°C[3]			2	μA
Oscillator					
C_{OSC}	Integrated oscillator capacitance		40		pF
f/f_{OSC}	Oscillator stability for: ΔV_{DD} = 100mV, V_{DD} = 1.5V, T_A = 25°C		2×10^6		
Quartz crystal parameters					
	Frequency = 32,768kHz				
R_S	Series resistance			40	kΩ
C_L	Parallel capacitance		9		pF
C_T	Trimmer capacitance	5		25	pF

NOTES:
1. The power-on reset circuit resets the I^2C bus logic when $V_{DD} < V_{POR}$.
2. When the voltages are a diode voltage above or below the supply voltage V_{DD} or V_{SS}, input current will flow; this current must not exceed ±0.5mA.
3. Event or 50Hz mode only (no quartz).

256 × 8-Bit Static RAM with Alarm Clock/Calendar PCF8583

FUNCTIONAL DESCRIPTION

The PCF8583 contains a 256-by-8-bit RAM with an 8-bit auto-increment address register, an on-chip 32,768kHz oscillator circuit, a frequency divider, a serial two-line bidirectional I^2C bus interface and a power-on reset circuit.

The first 8 bytes of the RAM (memory addresses 00 to 07) are designed as addressable 8-bit parallel registers. The first register (memory address 00) is used as a control/status register. The memory addresses 01 to 07 are used as counters for the clock function. The memory addresses 08 to 0F are free RAM locations or may be programmed as alarm registers.

Counter Function Modes

When the control/status register is set, a 32,768kHz clock mode, a 50Hz clock mode, or an event counter mode can be selected.

In the clock modes, the hundredths of a second, seconds, minutes, hours, date, month (four-year calendar), and weekdays are stored in a BCD format. The timer register stores up to 99 days. The event counter mode is used to count pulses applied to the oscillator input (OSCO left open). The event counter stores up to 6 digits of data.

When one of the counters is read (memory locations 01 to 07), the contents of all counters are strobed into capture latches at the beginning of a read cycle. Therefore, faulty reading of the count during a carry condition is prevented.

Alarm Function Modes

By setting the alarm enable bit of the control/status register, the alarm control register (address 08) is activated.

By setting the alarm control register, a dated alarm, a daily alarm, a weekday alarm, or a timer alarm may be programmed. In the clock modes, the timer register (address 07) may be programmed to count hundredths of a second, seconds, minutes, hours, or days. Days are counted when an alarm is not programmed.

Whenever an alarm event occurs, the alarm flag of the control/status register is set. A timer alarm event will set the alarm flag and an overflow condition of the timer will set the timer flag. The open-drain interrupt output is switched on (Active-Low) when the alarm or timer flag is set (enabled).

When a timer function without any alarm function is programmed, the remaining alarm registers (addresses 09 to 0F) may be used as free RAM space.

Table 1. Cycle Length of the Time Counters, Clock Modes

UNIT	COUNTING CYCLE	CARRY TO THE NEXT UNIT	CONTENTS OF THE MONTH COUNTER
Hundredths of a second	00 to 99	99 to 00	
Seconds	00 to 59	59 to 00	
Minutes	00 to 59	59 to 00	
Hours (24h)	00 to 23	23 to 00	
Hours (12h)	12 AM, 01 AM to 11 AM, 12 PM, 01 PM to 11 PM	11 PM to 12 AM	
Date	01 to 31 01 to 30 01 to 29 01 to 28	31 to 01 30 to 01 29 to 01 28 to 01	1, 3, 5, 7, 8, 10, 12 4, 6, 9, 11 2, year = 0 2, year = 1, 2, 3
Months	01 to 12	12 to 01	
Year	0 to 3		
Weekdays	0 to 6	6 to 0	
Timer/days	00 to 99	no carry	

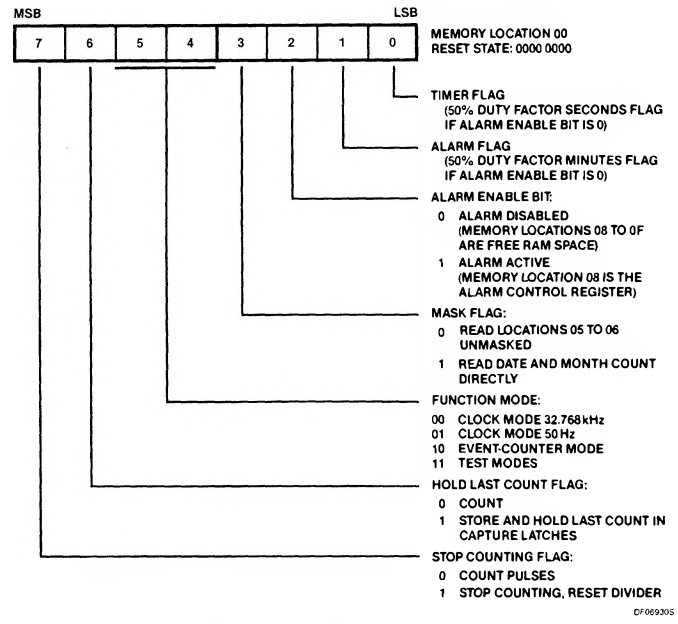


Figure 1. Control/Status Register

Control/Status Register

The control/status register is defined as the memory location 00 with free access for reading and writing via the I^2C bus. All functions and options are controlled by the contents of the control/status register (see Figure 1).

Counter Registers

In the different modes, the counter registers are programmed and arranged as shown in Figure 2. Counter cycles are listed in Table 1.

In the clock modes, 24h or 12h format can be selected by setting the most significant bit of the hours counter register. The format of the hours counter is shown in Figure 3.

The year and date are packed into memory location 05 (see Figure 4). The weekdays and months are packed into memory location 06 (see Figure 5). When reading these memory locations, the year and weekdays are masked out when the mask flag of the control/status register is set. This allows the user to read the date and month count directly.

In the event counter mode, events are stored in BCD format. D5 is the most significant and D0 the least significant digit. The divider is bypassed.

Alarm Control Register

When the alarm enable bit of the control/status register is set, the alarm control register (address 08) is activated. All alarm, timer, and interrupt output functions are controlled by the contents of the alarm control register (see Figures 6a and 6b).

Alarm Registers

All alarm registers are allocated with a constant address offset of hex 08 to the corresponding counter registers.

An alarm goes off when the contents of the alarm registers match bit-by-bit the contents of the involved counter registers. The year and weekday bits are ignored in a dated alarm. A daily alarm ignores the month and date bits. When a weekday alarm is selected, the contents of the alarm weekday/month register will select the weekdays on which an alarm is activated (see Figure 7).

Interrupt Output

The open-drain n-channel interrupt output is programmed by setting the alarm control register. It is switched on (Active-Low) when the alarm flag or the timer flag is set. In the clock mode without alarm, the output sequence is controlled by the timer flag. The OFF voltage of the interrupt output may exceed the supply voltage.

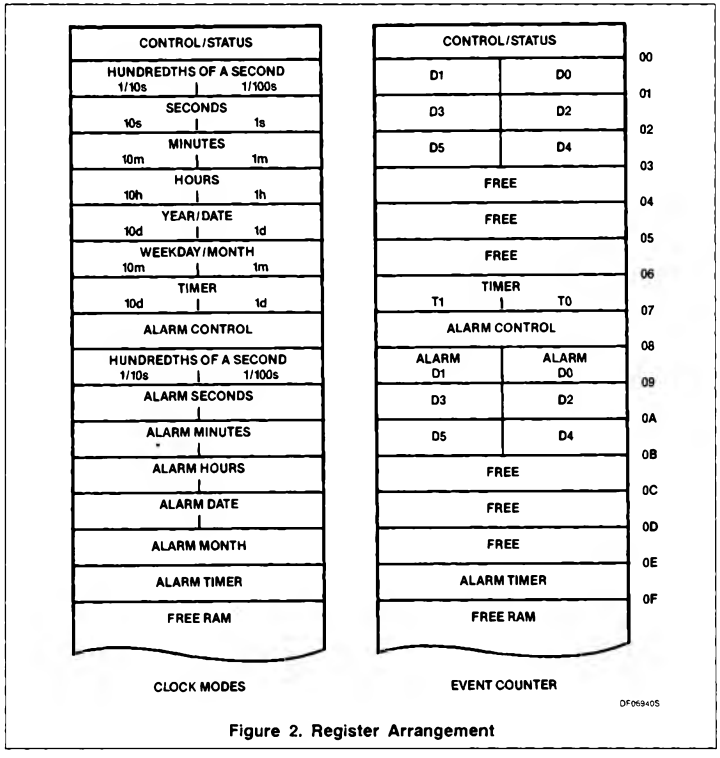


Figure 2. Register Arrangement

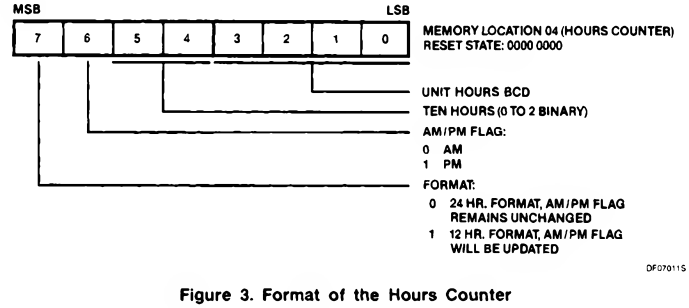


Figure 3. Format of the Hours Counter

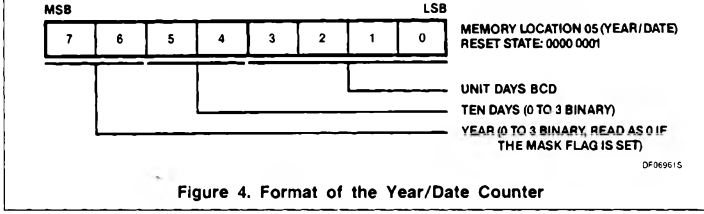


Figure 4. Format of the Year/Date Counter

Oscillator and Divider

A 32,768kHz quartz crystal has to be connected to OSCI (Pin 1) and OSCO (Pin 2). A trimmer capacitor between OSCI and V_{DD} is used for tuning the oscillator. The oscillator frequency is scaled down to 128Hz by the divider. A 100Hz clock signal is derived from this signal.

In the 50Hz clock mode or event counter mode, the oscillator is disabled and the oscillator input is switched to a high-impedance state. This allows the user to feed the 50Hz reference frequency or an external high-speed event signal into the input OSCI.

Initialization

When power-up occurs, the I²C bus interface, the control/status register, and all clock counters are reset. The device starts timekeeping in the 32,768kHz clock mode with the 24h format on the first of January at 0.00.00:00.

A second level-sensitive reset signal to the I²C bus interface is generated as soon as the supply voltage drops below the interface reset level. This reset signal does not affect the control/status or clock counter registers.

It is recommended to set the stop counting flag of the control/status register before loading the actual time into the counters. Loading of illegal states will lead to a clock malfunction, but will not latch-up the device.

CHARACTERICS OF THE I²C BUS

The I²C bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the High period of the clock pulse, as changes in the data line at this time will be interpreted as a control signal.

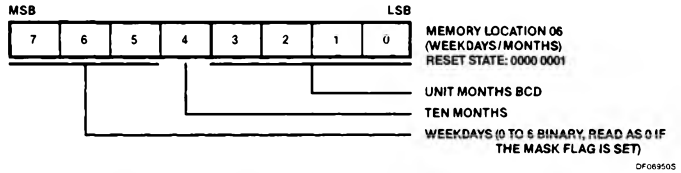
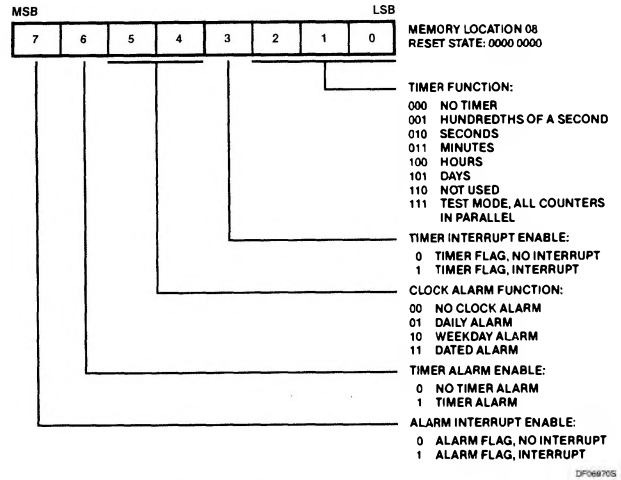
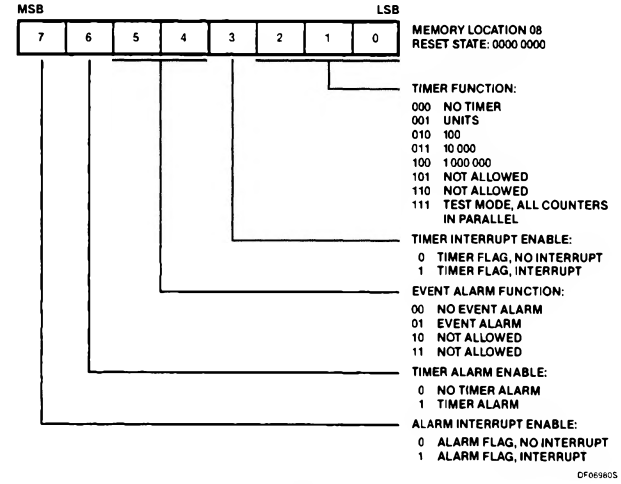


Figure 5. Format of the Weekdays/Months Counter



a. Alarm Control Register, Clock Modes



b. Alarm Control Register, Event Counter Mode

Figure 6

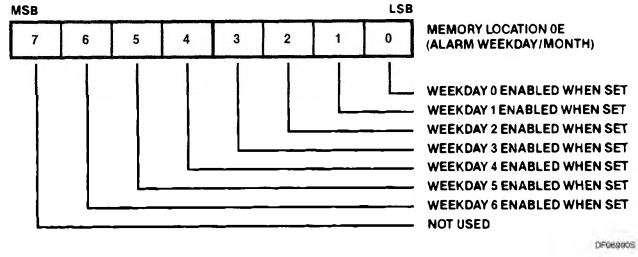


Figure 7. Selection of Alarm Weekdays

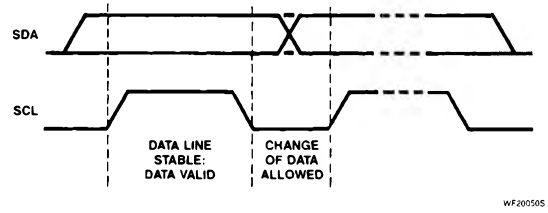


Figure 8. Bit Transfer

Start and Stop Conditions

Both data and clock lines remain High when the bus is not busy. A High-to-Low transition of the data line, while the clock is High, is defined as the start condition (S). A Low-to-High transition of the data line, while the clock is High, is defined as the stop condition (P).

System Configuration

A device generating a message is a "transmitter"; a device receiving a message is the "receiver". The device that controls the message is the "master", and the devices which are controlled by the master are the "slaves".

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each data byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a High level put on the bus by the transmitter, whereas the master also generates an extra acknowledge-related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also, a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The acknowledge device has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable Low during the High period of the clock pulse. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line High to enable the master to generate a stop condition.

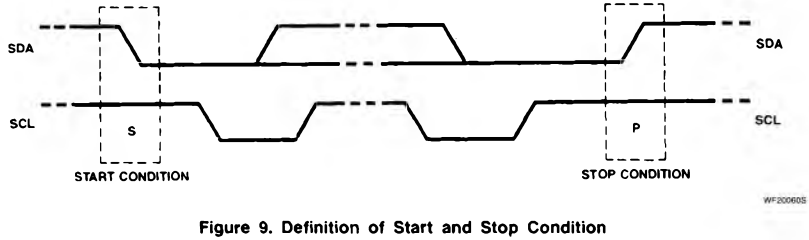


Figure 9. Definition of Start and Stop Condition

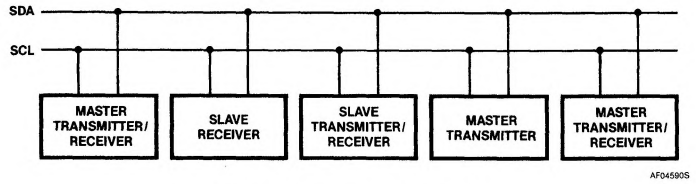


Figure 10. System Configuration

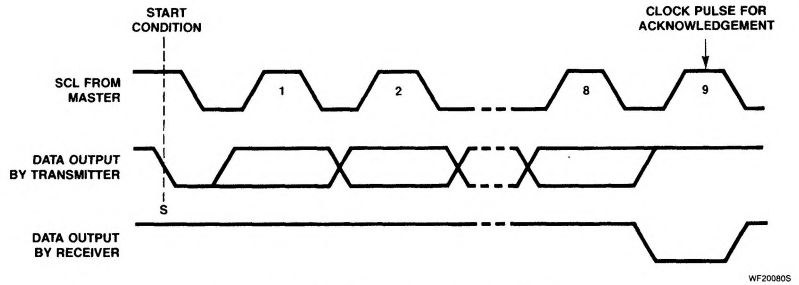


Figure 11. Acknowledgment on the I^2C Bus

Timing Specifications

All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
f_{SCL}	SCL clock frequency			100	kHz
t_{SW}	Tolerable spike width on bus			100	ns
t_{BUF}	Bus free time	4.0			μs
$t_{SU;\ STA}$	Start condition setup time	4.0			μs
$t_{HD;\ STA}$	Start condition hold time	4.7			μs
t_{LOW}	SCL Low time	4.7			μs
t_{HIGH}	SCL High time	4.0			μs
t_R	SCL and SDA rise time			1.0	μs
t_F	SCL and SDA fall time			0.3	μs
$t_{SU;\ DAT}$	Data setup time	250			ns
$t_{HD;\ DAT}$	Data hold time	0			ns
$t_{VD;\ DAT}$	SCL Low to data out valid			3.4	μs
$t_{SU;\ STO}$	Stop condition setup time	4.0			μs

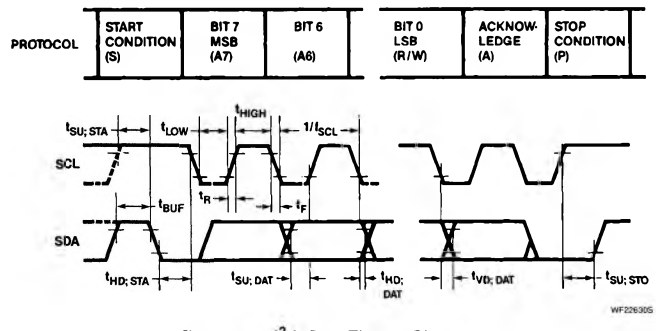


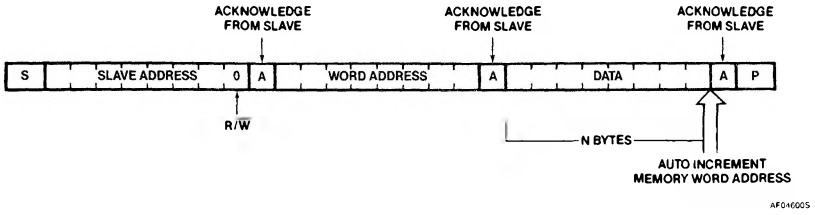
Figure 12. I^2C Bus Timing Diagram

I²C Bus Protocol

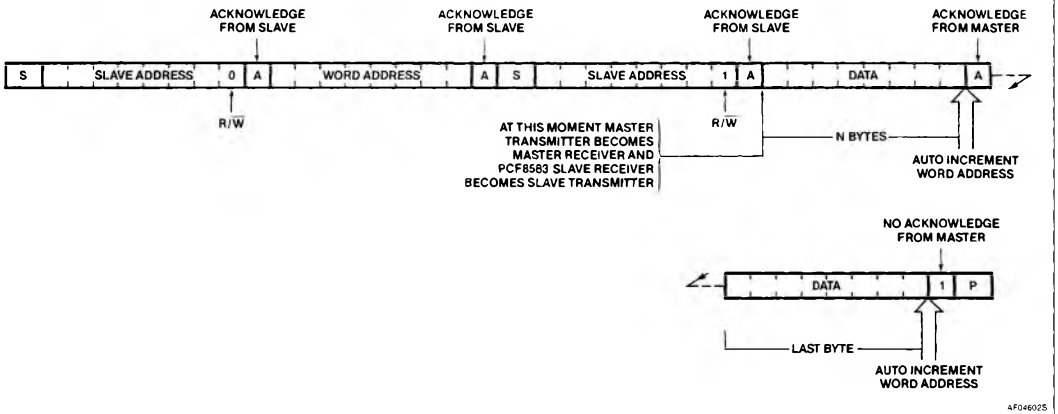
Before any data is transmitted on the I²C bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure. The I²C bus configuration for the different PCF8583 READ and WRITE cycles is shown in Figure 13.

APPLICATION INFORMATION

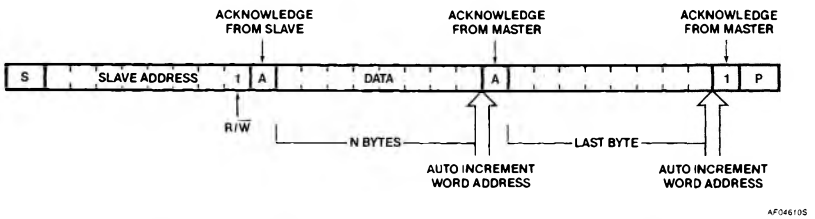
The PCF8583 slave address has a fixed combination 1010 as group 1.



a. Master Transmits to Slave Receiver (WRITE mode)



b. Master Reads After Setting Word Address (WRITE Word Address; READ Data)



c. Master Reads Slave Immediately After First Byte (READ Mode)

Figure 13

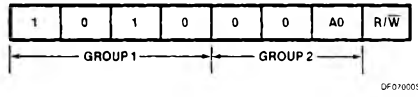


Figure 14. PCF8583 Address

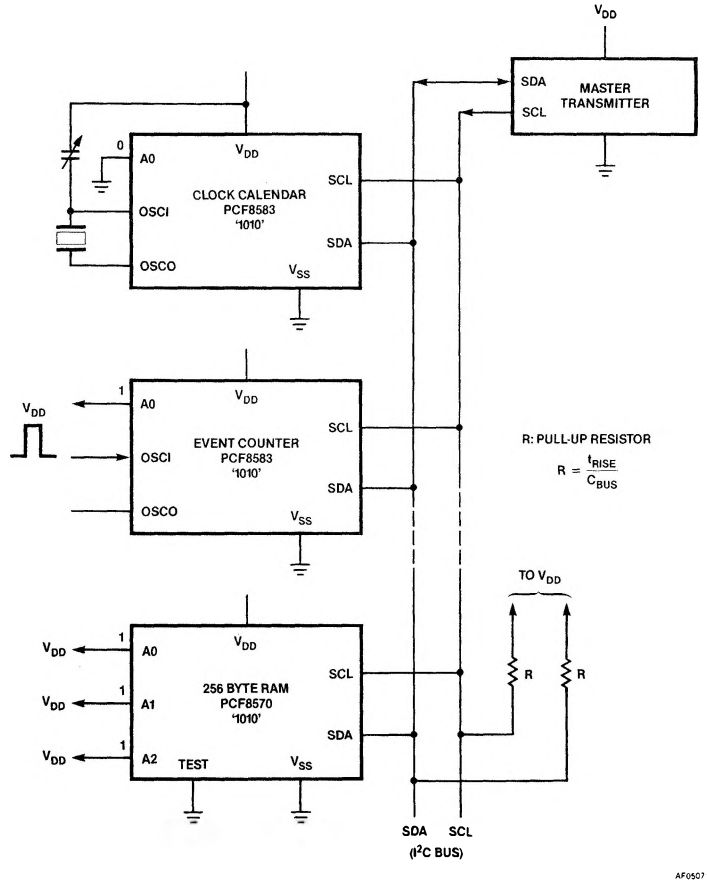


Figure 15. PCF8583 Application Diagram