Signetics

Linear Products

PCF8582A
Static CMOS EEPROM (256 × 8-bit)

Preliminary Specification

DESCRIPTION

The PCF8582A is 2K-bit 5V electrically erasable programmable read only memory (EEPROM) organized as 256 by 8 bits. It is designed in a floating-gate CMOS technology.

As data bytes are received and transmitted via the serial I^2C bus, an 8-pin DIP package is sufficient. Up to eight PCF8582A devices may be connected to the I^2C bus.

Chip select is accomplished by three address inputs.

FEATURES

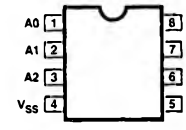
- **Non-volatile storage of 2K-bit organized as 256 × 8**
- **Only one power supply required (5V)**
- **On-chip voltage multiplier for erase/write**
- **Serial input/output bus (I^2C)**
- **Automatic word address incrementing**
- **Low power consumption**
- **One point erase/write timer**
- **Power-on reset**
- **10,000 erase/write cycles per byte**
- **10 years non-volatile data retention**
- **Infinite number of read cycles**
- **Pin-and address-compatible to PCF8570 and PCF8571**

APPLICATIONS

- **Telephony**
- **Radio and television**
- **General purpose**

PIN CONFIGURATION

N Package

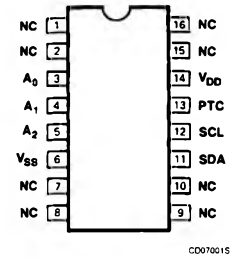


TOP VIEW

CD12090S

PIN NO.	SYMBOL	DESCRIPTION
1	A0	
2	A1	Address inputs/test
3	A2	Mode select
4	V_{SS}	Ground
5	SDA	I^2C bus lines
6	SCL	
7	PTC	Programming time control
8	V_{DD}	Positive supply

D Package



CD07001S

PIN NO.	SYMBOL	DESCRIPTION
1	NC	Not connected
2	NC	Not Connected
3	A_0	Address inputs/test mode select
4	A_1	
5	A_2	
6	V_{SS}	Logic ground
7	NC	Not connected
8	NC	Not connected
9	NC	Not connected
10	NC	Not connected
11	SDA	I^2C bus data input/output
12	SCL	I^2C bus clock input/output
13	PTC	Programming time control
14	V_{DD}	Positive supply voltage
15	NC	Not connected
16	NC	Not connected

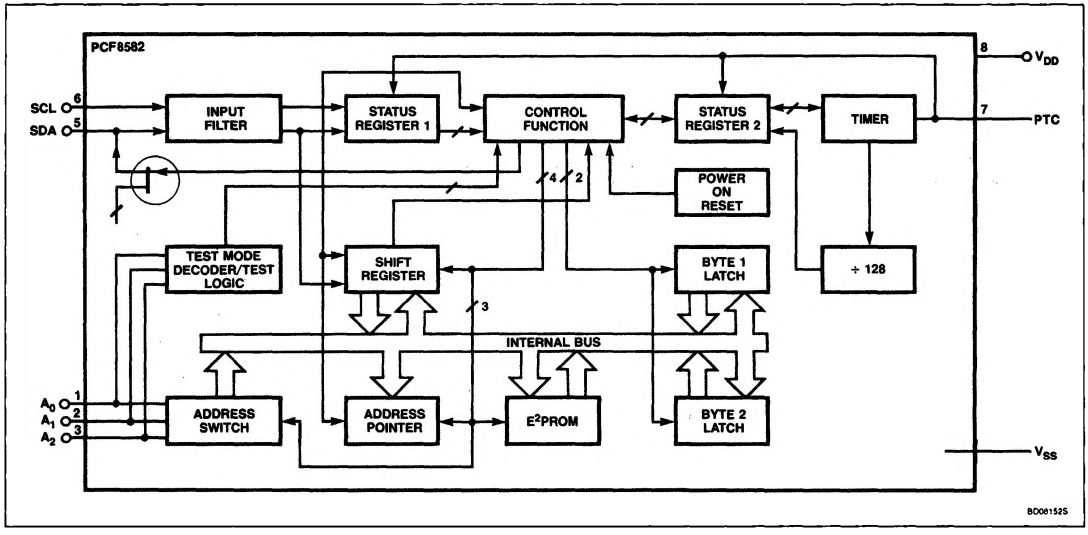
ORDERING INFORMATION

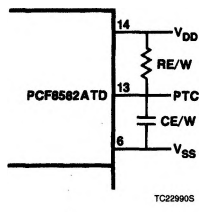
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP (SOT-97A)	−40°C to +85°C	PCF8582APN
16-Pin Plastic SO (SO16L; SOT-162A)	−40°C to +85°C	PCF8582ATD

ABSOLUTE MAXIMUM RATINGS

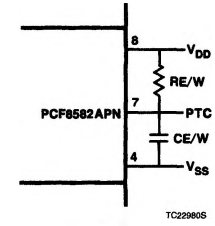
SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Supply voltage	−0.3 to 7	V
V_{IN}	Input voltage, at Pin 4, (input impedance 500Ω)	V_{SS} − 0.8 to V_{DD} + 0.8	V
T_A	Operating temperature range	−40 to +85	°C
T_{STG}	Storage temperature range	−65 to +150	°C
I_I	Current into any input pin	1	mA
I_O	Output current	10	mA

BLOCK DIAGRAM





a.



b.

Figure 1. RC Circuit Connections to PCF8582APN and PCF8582ATD When Using the Internal Oscillator

DC AND AC ELECTRICAL CHARACTERISTICS

V_{DD} = 5V; V_{SS} = 0V; T_A = −40°C to +85°C, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V_{DD}	Operating supply voltage	4.5	5	5.5	V
I_{DDR}	Operating supply current, READ ($V_{DD\ MAX}$, f_{SLC} = 100kHz)			0.4	mA
I_{DDW}	Operating supply current, WRITE/ERASE			2.0	mA
I_{DDO}	Standby supply current ($V_{DD\ MAX}$)			10	μA
Input PTC					
V_{IHP}	Input voltage High	V_{DD} − 0.3			V
V_{ILP}	Input voltage Low			V_{SS} + 0.3	V

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) V_{DD} = 5V; V_{SS} = 0V; T_A = −40°C to + 85°C, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Input SCL					
V_{IL} V_{IH} V	Input/output SDA: Input voltage LOW Input voltage HIGH Output voltage LOW	−0.3 3		1.5 V_{DD} + 0.8	V V
V_{OL}	(I_{OL} = 3mA, V_{DD} = 4.5V)			0.4	V
I_{OH}	Output leakage current HIGH (V_{OH} = V_{DD})			1	μA
$\pm I_{IN}$	Input leakage current (A0, A1, A2, SCL)[1]			1	μA
f_{SCL}	Clock frequency	0		100	kHz
C_I	Input capacitance (SCL, SDA)			7	pF
t_I	Noise suppression time constant at SCL and SDA input	0.25	0.5	1	μs
t_{BUF}	Time the bus must be free before a new transmission can start	4.7			μs
t_{HD}, t_{STA}	Hold time start condition. After this period the first clock pulse is generated	4			μs
t_{LOW}	The LOW period of the clock	4.7			μs
t_{HIGH}	The HIGH period of the clock	4			μs
t_{SU}, t_{STA}	Setup time for start condition (only relevent for a repeated start condition)	4.7			μs
t_{HD}, t_{DAT} t_{HD}, t_{DAT}	Hold time DATA for: CBUS compatible masters I^2C devices[2]	 5 0			 μs μs
t_{SU}, t_{DAT}	Setup time DATA	250			ns
t_R	Rise time for both SDA and SCL lines			1	μs
t_F	Fall time for both SDA and SCL lines			300	ns
t_{SU}, t_{STO}	Setup time for stop condition	4.7			μs
Erase/write timer constant					
$C_{E/W}$	Erase/write timing capacitor for erase/write cycle of 30ns[3]		3.3		nF
$R_{E/W}$	Erase/write cycle timing resistor[4]		56.0		kΩ
Programming frequency using external clock					
f_P	Frequency	2.57		12.85	kHz
t_{Low}	Period Low	10.0			μs
t_{High}	Period High	10.0			μs
t_R	Rise time			300	ns
t_F	Fall time			300	ns
t_D	Delay time	0			ns
t_S	Data retention time (T_A = 55°C)	10			years

NOTES:
1. Selection of the chip address is done by connecting the A0, A1, and A2 inputs either to V_{SS} or V_{DD}.
2. A transmitter must internally provide a hold time to bridge the undefined region (maximum 300ns) of the falling edge of SCL.
3. Maximum tolerance ±10% using internal oscillator.
4. Maximum tolerance ±5% using internal oscillator.

FUNCTIONAL DESCRIPTION

Characteristics of the I²C Bus

The I²C bus is intended for communication between different ICs. The serial bus consists of two bidirectional lines, one for data signals (SDA), and one for clock signals (SCL). Both the SDA and the SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:

Data transfer may be initiated only when the bus is not busy.

During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus Not Busy — both data and clock lines remain HIGH.

Start Data Transfer — a change in the state of the data line, from HIGH to LOW, while the clock is HIGH defines the start condition.

Stop Data Transfer — a change in the state of the data line, from LOW to HIGH, defines the stop condition.

Data Valid — the state of the data line represents valid data when, after a start condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line may be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition; the number of the data bytes transferred between the start and stop conditions is limited to two bytes in the ERASE/WRITE mode and unlimited in the READ mode. The information is transmitted in bytes and each receiver acknowledges with a ninth bit.

Within the I²C bus specifications a low-speed mode (2kHz clock rate) and a high-speed mode (100kHz clock rate) are defined. The PCF8582A works in both modes. By definition a device that gives out a signal is called a "transmitter," and the device which receives the signal is called a "receiver". The device which controls the signal is called the "master". The devices that are controlled by the master are called "slaves".

Each word of eight bits is followed by one acknowledge bit. This acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge-related clock pulse. A slave receiver which it addresses is obliged to generate an acknowledge after the reception of each byte.

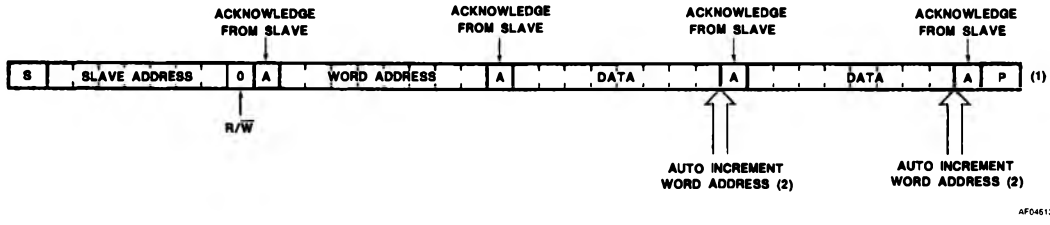
Also, a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the high period of the acknowledge related clock pulse.

Setup and hold times must be taken into account. A master receiver must signal an end-of-data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case the transmitter must leave the data line HIGH to enable the master generation of the stop condition.

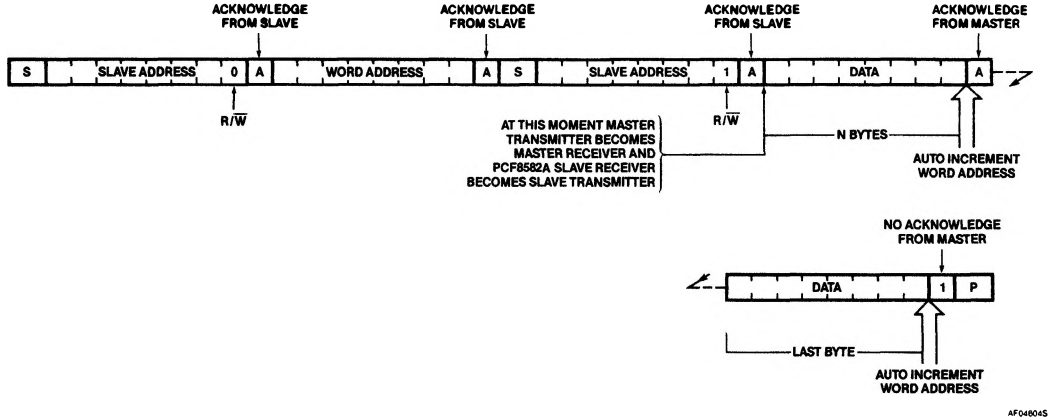
I²C Bus Protocol

The I²C bus configuration for different READ and WRITE cycles of the PCF8582A are shown in Figures 1a and 1b.

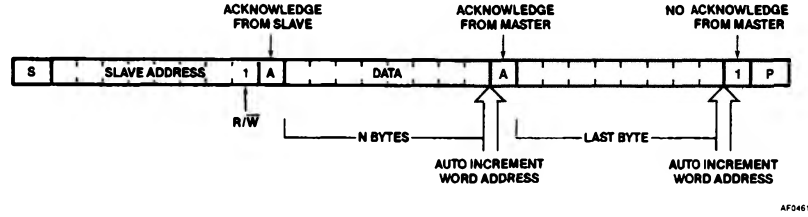


NOTES:
1. After this stop condition the erase/write cycle starts and the bus is free for another transmission; the duration of the erase/write cycle is approximately 30ms if only one byte is written, and 60ms if two bytes are written. During the erase/written cycle the slave receiver does not send an acknowledge bit if addressed via I^2C bus.
2. The second data byte is voluntary. Trying to erase/write more than two bytes is not allowed.

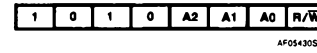
a. Master Transmitter Transmits to PCF8582A Slave Receiver (ERASE/WRITE Mode)



b. Master Reads PCF8582A Slave After Setting Word Address (Write Word Address; READ Data)



The slave address is defined in accordance with the I^2C bus specification as:



NOTE:
1. The device can be used as read only without the programming clock.

c. Master Reads PCF8582A Slave Immediately After First Byte (READ Mode)[1]

Figure 2

I²C BUS TIMING

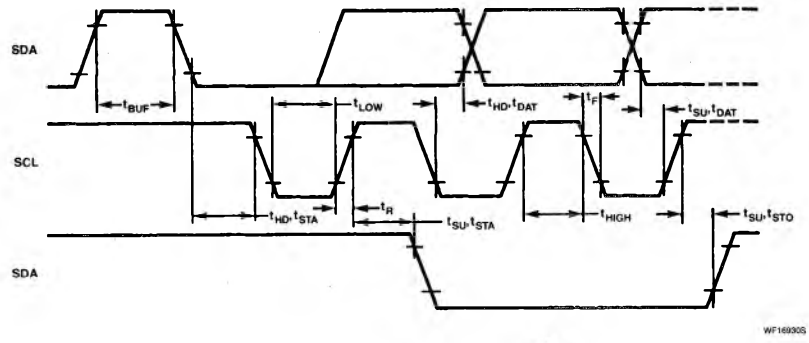


Figure 3. Timing Requirements for the I²C Bus