Signetics

PCF8577
32-/64-Segment LCD Driver for Automotive

Product Specification

Linear Products

DESCRIPTION

The PCF8577 is a single-chip, silicon-gate CMOS circuit. It is designed to drive liquid crystal displays with up to 32 segments directly, or 64 segments in a duplex manner.

The two-line I^2C bus interface substantially reduces wiring overheads in remote display applications. Bus traffic is minimized in multiple IC applications by automatic address incrementing, hardware sub-addressing, and display memory switching (direct drive mode).

FEATURES

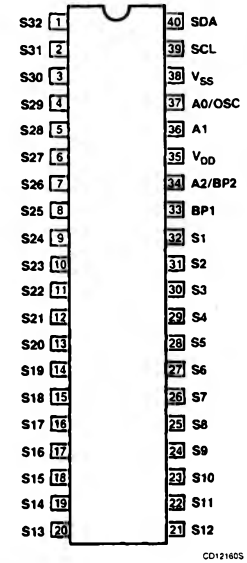
- **Direct-/duplex-drive modes with up to 32-/64-segment LCD drive capability per device**
- **Operating supply voltage: 2.5 to 9V**
- **Low power consumption**
- **I^2C bus interface**
- **Optimized pinning for single plane wiring**
- **Single-pin built-in oscillator**
- **Auto-incremented loading across device sub-address boundaries**
- **Display memory switching in direct-drive mode**
- **May be used for I^2C bus output expander**
- **System expansion up to 256 segments**
- **Power-on reset sets all segments off (to blank)**

APPLICATIONS

- **Telephony**
- **Car dashboards**
- **General instrumentation**

PIN CONFIGURATION

N, D Packages



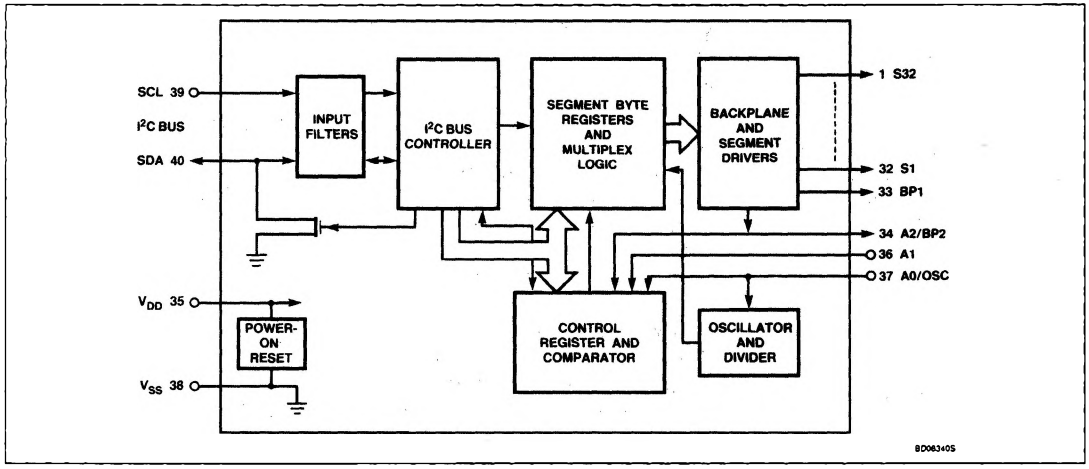
CD12160S

PIN NO.	SYMBOL	DESCRIPTION
Supply		
35	V_{DD}	Positive supply
38	V_{SS}	Negative supply
I^2C bus		
40	SDA	I^2C bus data line
39	SCL	I^2C bus clock line
Inputs		
36	A1	Hardware address line
37	A0/OSC	Hardware address line/oscillator pin
Outputs		
1 - 32	S1 - S32	Segment outputs
Input - Output		
34	A2/BP2	Hardware address line/cascade sync input/backplane output
33	BP1	Cascade sync input/backplane output

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
40-Pin Plastic DIP (SOT-129)	-40°C to +85°C	PCF8577PN
40-Pin Plastic SO (VSO-40; SOT-158A)	-40°C to +85°C	PCF8577TD

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Supply voltage range	−0.5 to 11	V
V_I	Voltage on any pin	V_{SS} − 0.8 to V_{DD} + 0.8	V
± I_I	DC input current	20	mA
± I_O	DC output current	25	mA
± I_{DD}, I_{SS}	V_{DD} or V_{SS} current	50	mA
P_{TOT}	Power dissipation per package	500[1]	mW
P_D	Power dissipation per output	100	mW
T_A	Operating ambient temperature range	−40 to +85	°C
T_{STG}	Storage temperature range	−65 to +150	°C

NOTE:
1. Derate 7.7mW/°C when $T_A > 60°C$.

DC AND AC ELECTRICAL CHARACTERISTICS V_{DD} = 2.5 to 9V; V_{SS} = 0V; T_A = −40°C to +85°C, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V_{DD}	Supply voltage	2.5		9.0	V
I_{DD}	Supply current at f_{SCL} = 100kHz, no load, R_{OSC} = 1MΩ			250	μA
V_{REF}	Power-on reset level[1]	0.9	1.3	2.0	V
	Input SCL; input/output SDA				
V_{IL}	input voltage Low	0		0.8	V
V_{IH}	input voltage High	2.0		9.0	V
I_{OL}	output current Low at V_{OL} = 0.4V	3.0			mA
I_{OH}	output leakage current High at $V_{OH} = V_{DD}$			100	nA
t_{SW}	tolerable spike width on bus			100	ns
C_I	input capacitance at $V_I = V_{SS}$			7	pF
I_I	A1 input leakage current at $V_I = V_{SS}$ or V_{DD}			100	nA
I_I	A2/BP2 input current at $V_I = V_{DD}$		5.0		μA
$\pm I_I$	A0/OSC input current at $V_I = V_{SS}$ or V_{DD}		5.0		μA
$\pm V_{BP}$	DC component of LCD driver		20		mV
C_{SX}	Segment loads			5	nF
R_{SX}		1			MΩ
I_{OL}	Segment output current at V_{OL} = 0.4V; V_{DD} = 5V	0.3			mA
$-I_{OH}$	Segment output current at $V_{OH} = V_{DD}$ − 0.4V; V_{DD} = 5V	0.3			mA
C_{BP}	Backplane load (direct drive)			50	nF
R_{BP}		100			kΩ
C_{BP}	Backplane loads (duplex drive)			35	nF
R_{BP}		100			kΩ
t_R, t_F	Rise and fall times ($V_{BP} - V_{SX}$) at maximum load			200	μs
f_{LCD}	Display frequency at C_{OSC} = 680pF; R_{OSC} = 1MΩ	65	90	120	Hz

NOTE:
1. The power-on reset circuit resets the I^2C bus logic with $V_{DD} < V_{REF}$.

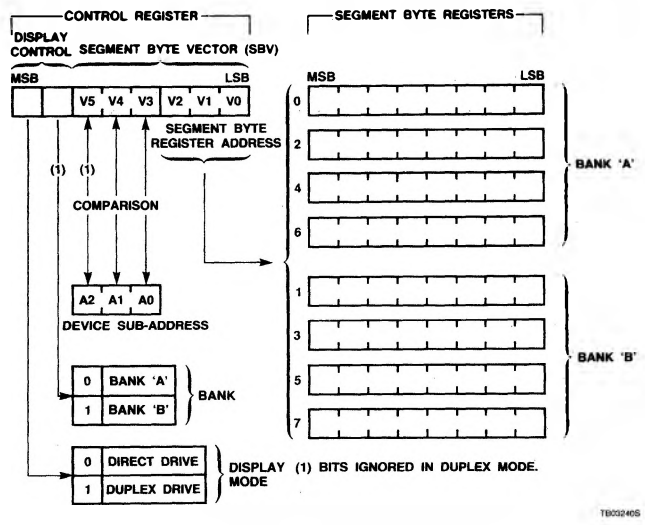


Figure 1. PCF8577 Register Organization

FUNCTIONAL DESCRIPTION

Hardware Sub-Address A0, A1, A2

The hardware sub-address lines A0, A1, A2 are used to program the device sub-address for each PCF8577 on the bus. Lines A0 and A2 are shared with OSC and BP2, respectively, to reduce pinout requirements.

A0/OSC Line A0 is defined as Low (logic 0) when this pin is used for the local oscillator or when connected to V_{SS}. Line A0 is defined as High (logic 1) when connected to V_{DD}.

A1 Line A1 must be defined as Low (logic 0) or as High (logic 1) by connection to V_{SS} or V_{DD}, respectively.

A2/BP2 In the direct drive mode, the second backplane signal BP2 is not used and the A2/BP2 pin is exclusively the A2 input. Line A2 is defined as Low (logic 0) when connected to V_{SS} or, if this is not possible, by leaving it unconnected (internal pull-down). Line A2 is defined as High (logic 1) when connected to V_{DD}.

In the duplex drive mode, the second backplane signal BP2 is required, and the A2 signal is undefined. In this mode, device selection is made exclusively from lines A0 and A1.

Oscillator A0/OSC

The PCF8577 has a single-pin built-in oscillator which provides the modulation for the LCD segment driver outputs. One external resistor and one external capacitor are connected to the A0/OSC pin to form the oscillator. In an expanded system containing more than one PCF8577, the backplane signals are usually common to all devices and only one oscillator is needed. The devices which are not used for the oscillator are put into the expansion mode by connecting the A0/OSC pin to either V_{DD} or V_{SS} depending on the required state for A0. In the expansion mode, each PCF8577 is synchronized from the backplane signal(s).

User-Accessible Registers

There are nine user-accessible 1-byte registers. The first is a control register which is used to control the loading of data into the segment byte registers and to select display options. The other eight are segment byte registers, split into two banks of storage, which store the segment data. The set of even-numbered segment byte registers is called BANK A. Odd-numbered segment byte registers are called BANK B.

All PCF8577 have the same slave address (see Figure 12). All devices load the second byte into the control register, and each device maintains an identical copy of the control byte in the control register at all times (see I^2C bus protocol Figure 13).

The control register is shown in more detail in Figure 1. The least-significant bits select which device and which segment byte register are loaded next. This part of the register is therefore called the Segment Byte Vector (SBV).

The upper three bits of the SBV (V5 to V3) are compared with the hardware sub-address input signals A2, A1, and A0. If they are the same, then the device is enabled for loading; if not, the device ignores incoming data but remains active.

The three least-significant bits of the SBV (V2 to V0) address one of the segment byte registers within the enabled chip for loading segment data.

The control register also has two display control bits. These bits are named MODE and BANK. The MODE bit selects whether the display outputs are configured for direct- or duplex-drive displays. The BANK bit allows the user to display BANK A or BANK B.

Auto-Incremented Loading

After each segment byte is loaded, the SBV is incremented automatically, thus auto-incremented loading occurs if more than one segment byte is received in a data transfer.

Since the SBV addresses both device and segment registers, auto-incremented loading may proceed across device boundaries provided that the hardware sub-addresses are arranged contiguously.

Direct-Drive Mode

The PCF8577 is set to the direct-drive mode by loading the MODE control bit with logic 0. In this mode, only four bytes are needed to store the data for the 32 segment drivers. Setting the BANK bit to logic 0 selects even bytes (BANK A); setting the BANK bit to logic 1 selects odd bytes (BANK B).

In the direct-drive mode, the SBV is auto-incremented by two after the loading of each segment byte register. This means that auto-incremented loading of BANK A or BANK B is possible. Either bank may be completely or partially loaded regardless of which bank is being displayed. Direct-drive output waveforms are shown in Figure 2.

Duplex Mode

The PCF8577 is set to the duplex mode by loading the MODE bit with logic 1. In this mode, a second backplane signal (BP2) is needed and pin A2/BP2 is used for this; therefore, A2 and its equivalent SBV Bit V5 are undefined. The SBV auto-increments by one between loaded bytes.

All of the segment bytes are needed to store data for the 32 segment drivers and the BANK bit is ignored.

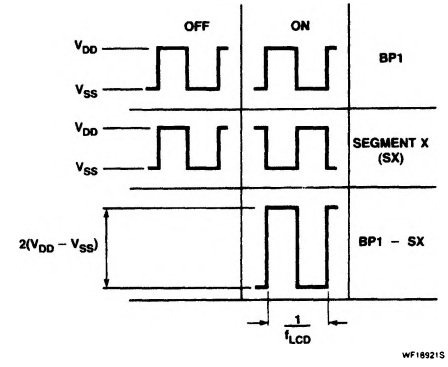
Duplex mode output waveforms are shown in Figure 3.

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

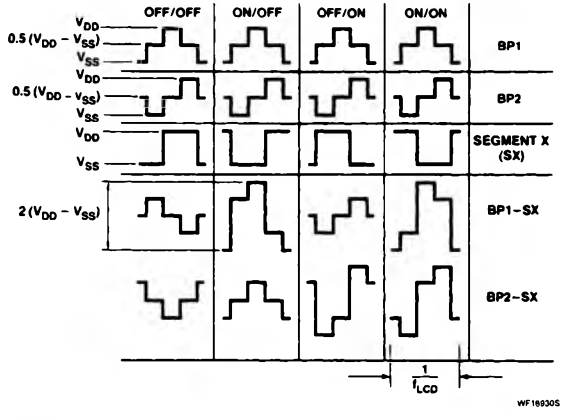
Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the High period of the clock pulse as changes in the data line at this time will be interpreted as control signals.



NOTES:
$V_{ON} = V_{DD} - V_{SS}$
$V_{OFF} = 0$

Figure 2. Direct-Drive Mode Display Output Waveforms



NOTES:
$V_{ON} = 0.79\ (V_{DD} - V_{SS})$
$V_{OFF} = 0.35\ (V_{DD} - V_{SS})$
$\frac{V_{ON}}{V_{OFF}} \approx 2.26$

Figure 3. Duplex Mode Display Output Waveforms

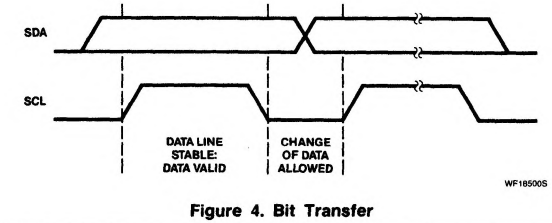


Figure 4. Bit Transfer

Start and Stop Conditions

Both data and clock lines remain High when the bus is not busy. A High-to-Low transition of the data line while the clock is High is defined as the start condition (S). A Low-to-High transition of the data line while the clock is High is defined as the stop condition (P).

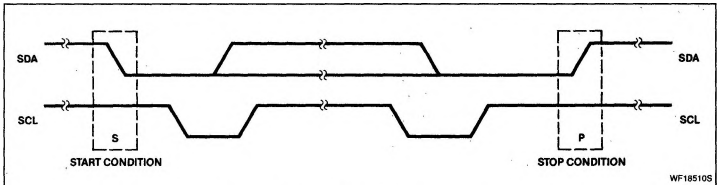


Figure 5. Definition of Start and Stop Conditions

System Configuration

A device generating a message is a "transmitter"; a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

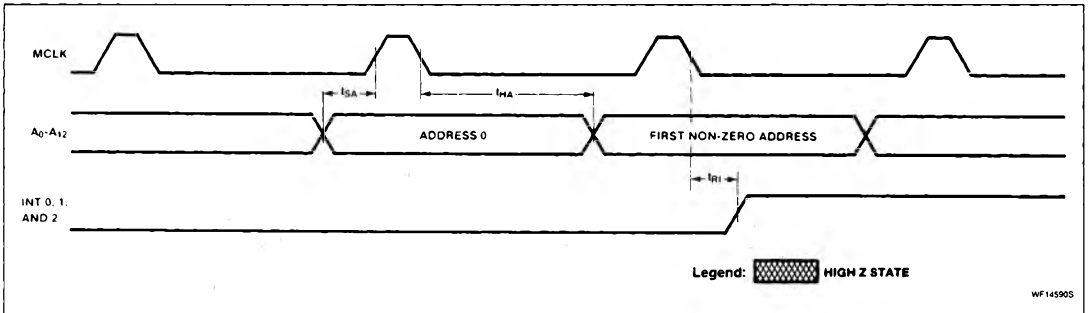


Figure 6. System Configuration

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte is followed by one acknowledge bit. The acknowledge bit is a High level put on the bus by the transmitter, whereas the master generates an extra acknowledge-related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also, a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable Low during the High period of the acknowledge-related clock pulse. Set-up and hold times must also be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line High to enable the master to generate a stop condition.

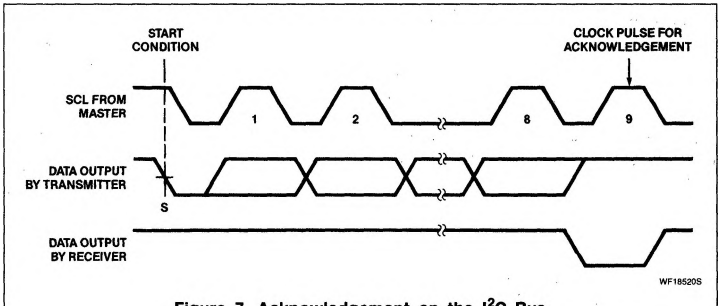
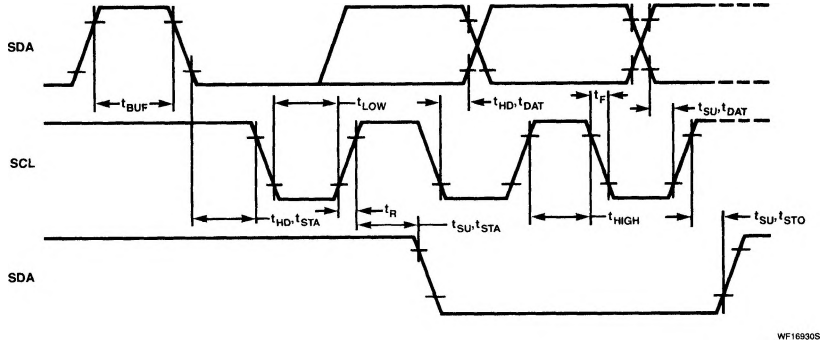


Figure 7. Acknowledgement on the I^2C Bus

Timing Specifications

Masters generate a bus clock with a maximum frequency of 100kHz. Detailed timing is shown in Figure 8.

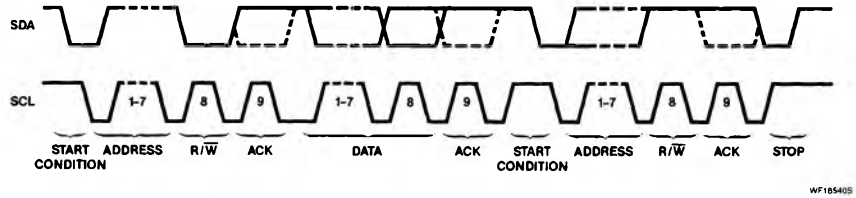


Where:

t_{BUF}	$t \geq t_{LOW\ min}$	The minimum time the bus must be free before a new transmission can start
$t_{HD};\ t_{STA}$	$t \geq t_{HIGH\ min}$	Start condition hold time
t_{LOWmin}	4.7μs	Clock Low period
$t_{HIGHmin}$	4μs	Clock High period
$t_{SU};\ t_{STA}$	$t \geq t_{LOW\ min}$	Start condition setup time; only valid for repeated start code
$t_{HD};\ t_{DAT}$	$t \geq 0\mu s$	Data hold time
$t_{SU};\ t_{DAT}$	$t \geq 250ns$	Data setup time
t_R	$t \leq 1\mu s$	Rise time of both the SDA and SCL line
t_F	$t \leq 300ns$	Fall time of both the SDA and SCL line
$t_{SU};\ t_{STO}$	$t \geq t_{LOW\ min}$	Stop condition setup time

NOTE:
All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}.

Figure 8. Timing



Where:

Clock t_{LOWmin}	4.7μs
$t_{HIGHmin}$	4μs
The dashed line is the acknowledgement of the receiver	
Mark-to-space ratio	1:1 (Low-to-High)
Maximum number of bytes	Unrestricted
Premature termination of transfer	Allowed by generation of STOP condition
Acknowledge clock bit	Must be provided by the master

Figure 9. Complete Data Transfer

ADDRESSING

Before any data is transmitted on the I^2C bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure.

Slave Address

The slave address for PCF8577 is shown in Figure 10.

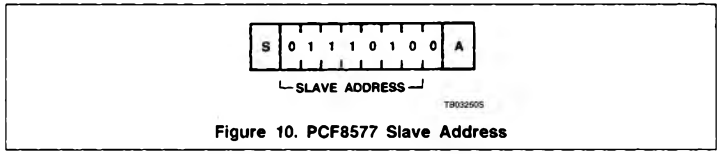


Figure 10. PCF8577 Slave Address

I^2C Bus Protocol

The PCF8577 I^2C bus protocol is shown in Figure 11.

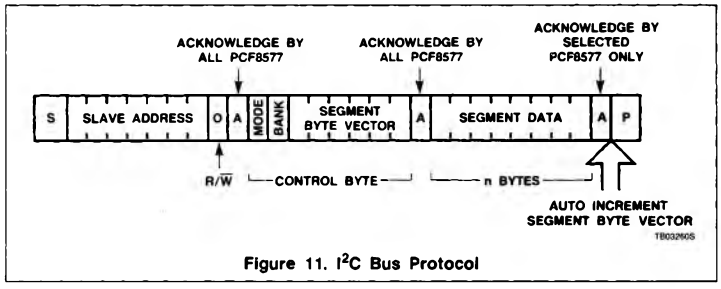


Figure 11. I^2C Bus Protocol

The PCF8577 is a slave receiver and has a fixed slave address (Figure 10). All PCF8577 on the same bus acknowledge the slave address in parallel. The second byte is always the control byte and is loaded into the control register of each PCF8577 on the bus. Subsequent data bytes are loaded into the segment registers of the selected device. Any number of data bytes may be loaded in one transfer and in an expanded system rollover of the SBV from 111 111 to 000 000 is allowed. If a stop (P) condition is given after the control byte acknowledge, the segment data remains unchanged. This allows the BANK bit to be toggled without changing the segment register contents. During loading of segment data, only the selected PCF8577 gives an acknowledge. Loading is terminated by generating a stop (P) condition.

DISPLAY MEMORY MAPPING

The mapping between the eight segment registers and the segment outputs S1 to S32 is shown in Tables 1 and 2.

Since only one register bit per segment is needed in the direct-drive mode, the BANK bit allows swapping of display information. If BANK is set to logic 0, even bytes (BANK A) are displayed; if BANK is set to logic 1, odd bytes (BANK B) are displayed. BP1 is always used for the backplane output in the direct-drive mode.

Table 1. Segment Byte — Segment Driver Mapping in the Direct-Drive Mode

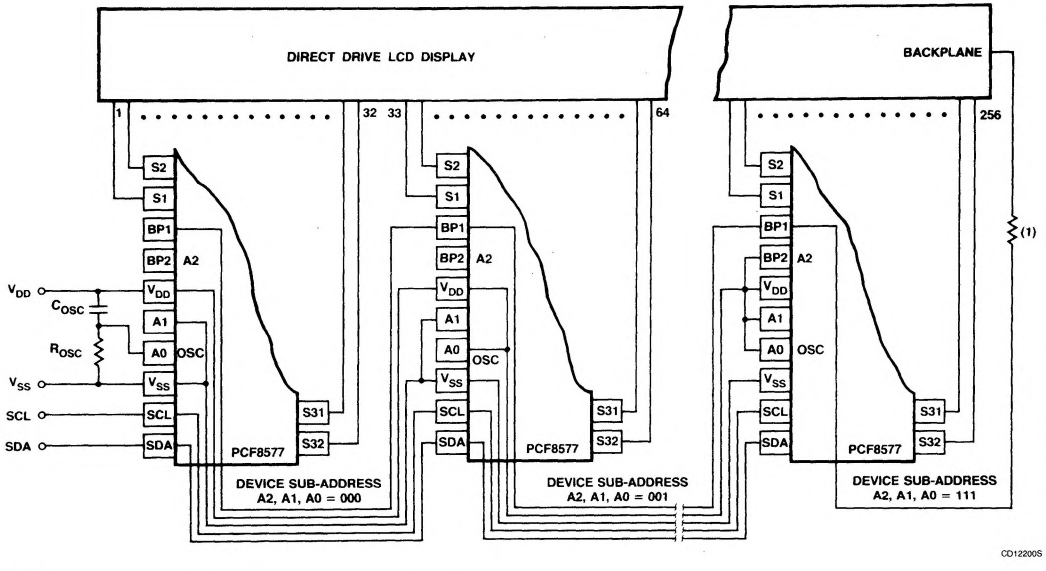
MODE	BANK	V2	V1	V0	SEGMENT REGISTER	BIT	MSB 7	6	5	4	3	2	1	LSB 0	BACKPLANE
0	0	0	0	0	0		S8	S7	S6	S5	S4	S3	S2	S1	BP1
0	1	0	0	1	1		S8	S7	S6	S5	S4	S3	S2	S1	BP1
0	0	0	1	0	2		S16	S15	S14	S13	S12	S11	S10	S9	BP1
0	1	0	1	1	3		S16	S15	S14	S13	S12	S11	S10	S9	BP1
0	0	1	0	0	4		S24	S23	S22	S21	S20	S19	S18	S17	BP1
0	1	1	0	1	5		S24	S23	S22	S21	S20	S19	S18	S17	BP1
0	0	1	1	0	6		S32	S31	S30	S29	S28	S27	S26	S25	BP1
0	1	1	1	1	7		S32	S31	S30	S29	S28	S27	S26	S25	BP1

NOTES:
Mapping example: Bit 0 of Register 7 controls the LCD segment S25 if BANK bit is a logic 1.
Even bytes (BANK A) correspond to backplane 1 (BP1) and odd bytes (BANK B) correspond to backplane 2 (BP2).

Table 2. Segment Byte — Segment Driver Mapping in the Duplex Mode

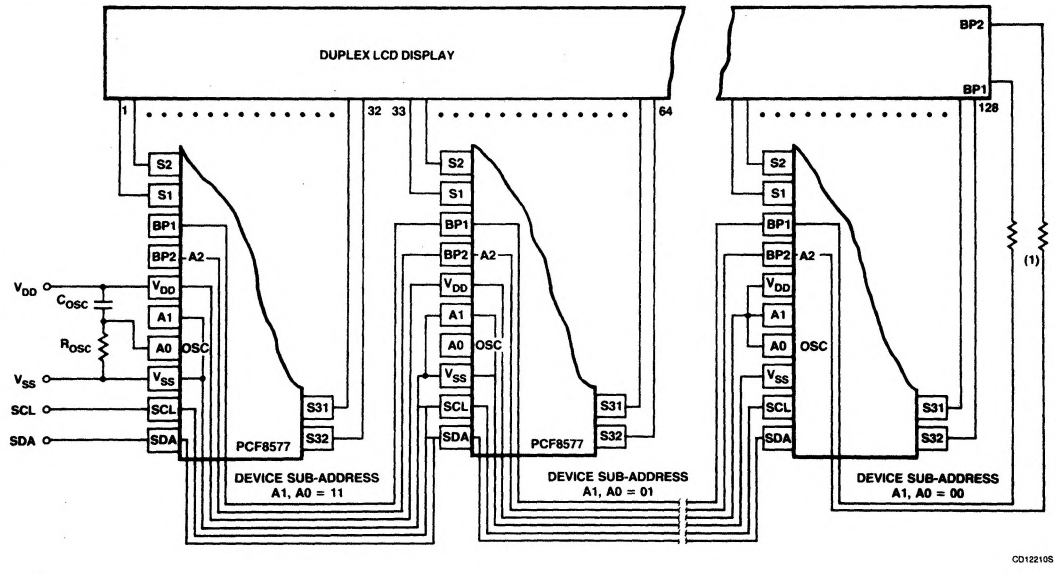
MODE	BANK	V2	V1	V0	SEGMENT REGISTER	BIT	MSB 7	6	5	4	3	2	1	LSB 0	BACKPLANE
1	x	0	0	0	0		S8	S7	S6	S5	S4	S3	S2	S1	BP1
1	x	0	0	1	1		S8	S7	S6	S5	S4	S3	S2	S1	BP2
1	x	0	1	0	2		S16	S15	S14	S13	S12	S11	S10	S9	BP1
1	x	0	1	1	3		S16	S15	S14	S13	S12	S11	S10	S9	BP2
1	x	1	0	0	4		S24	S23	S22	S21	S20	S19	S18	S17	BP1
1	x	1	0	1	5		S24	S23	S22	S21	S20	S19	S18	S17	BP2
1	x	1	1	0	6		S32	S31	S30	S29	S28	S27	S26	S25	BP1
1	x	1	1	1	7		S32	S31	S30	S29	S28	S27	S26	S25	BP2

NOTES:
X = don't care.
Mapping example: Bit 7 of Register 5 controls the LCD segment S24/BP2.



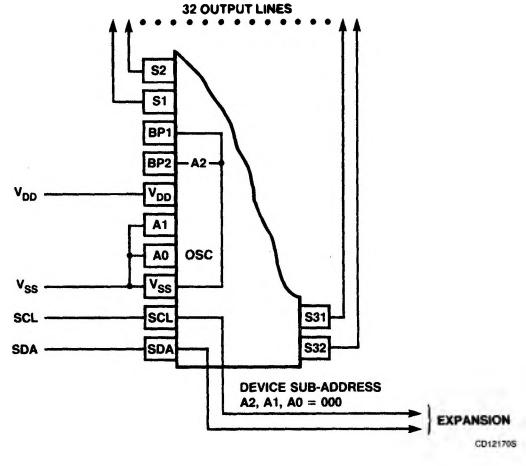
NOTE:
1. The series resistance of the display backplane must be greater than 1kΩ.

Figure 12. Direct-Drive Display; Expansion to 256 Segments Using Eight PCF8577s



NOTE:
1. The series resistances of the display backplanes must be greater than 1kΩ.

Figure 13. Duplex Display; Expansion to 2 × 128 Segments Using Four PCF8577s



NOTES:
1. MODE bit must always be set to 0 (direct-drive).
2. BANK switching is permitted.
3. BP1 must always be connected to V_{SS} and A0/OSC must be connnected to either V_{DD} or V_{SS} (no LCD modulation).

Figure 14. Use of PCF8577 as 32-Bit Output Expander in I^2C Bus Application