Signetics

PCF8573
Clock/Calendar With Serial I/O

Product Specification

Linear Products

DESCRIPTION

The PCF8573 is a low threshold, monolithic CMOS circuit that functions as a real-time clock/calendar in the Inter IC (I^2C) bus-oriented microcomputer systems. The device includes an addressable time counter and alarm register, both for minutes, hours, days and months. Three special control/status flags, COMP, POWF and NODA, are also available. Information is transferred serially via a two-lin bidirectional bus (I^2C). Back-up for the clock during supply interruptions is provided by a 1.2V nickel cadmium battery. The time base is generated from a 32.768kHz crystal-controlled oscillator.

FEATURES

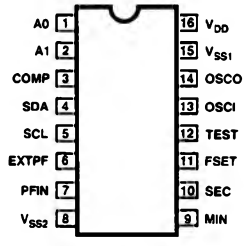
- **Serial input/output bus (I^2C) interface for minutes, hours, days and months**
- **Additional pulse outputs for seconds and minutes**
- **Alarm register for presetting a time for alarm or remote switching functions**
- **Battery back-up for clock function during supply interruption**
- **Crystal oscillator control (32.768kHz)**

APPLICATIONS

- **Automotive**
- **Telephony**

PIN CONFIGURATION

N, D Packages



TOP VIEW

CD10281S

PIN NO.	SYMBOL	DESCRIPTION
1	A0	Address input
2	A1	Address input
3	COMP	Comparator output
4	SDA	Serial data line (I^2C bus)
5	SCL	Serial clock line (I^2C bus)
6	EXTPF	Enable power fail flag input
7	PFIN	Power fail flag input
8	V_{SS2}	Negative supply 2 (I^2C interface)
9	MIN	One pulse per minute output
10	SEC	One pulse per second output
11	FSET	Oscillator tuning output
12	TEST	Test input; must be connected to V_{SS2} when not in use
13	OSCI	Oscillator input
14	OSCO	Oscillator input/output
15	V_{SS1}	Negative supply 1 (clock)
16	V_{DD}	Common positive supply

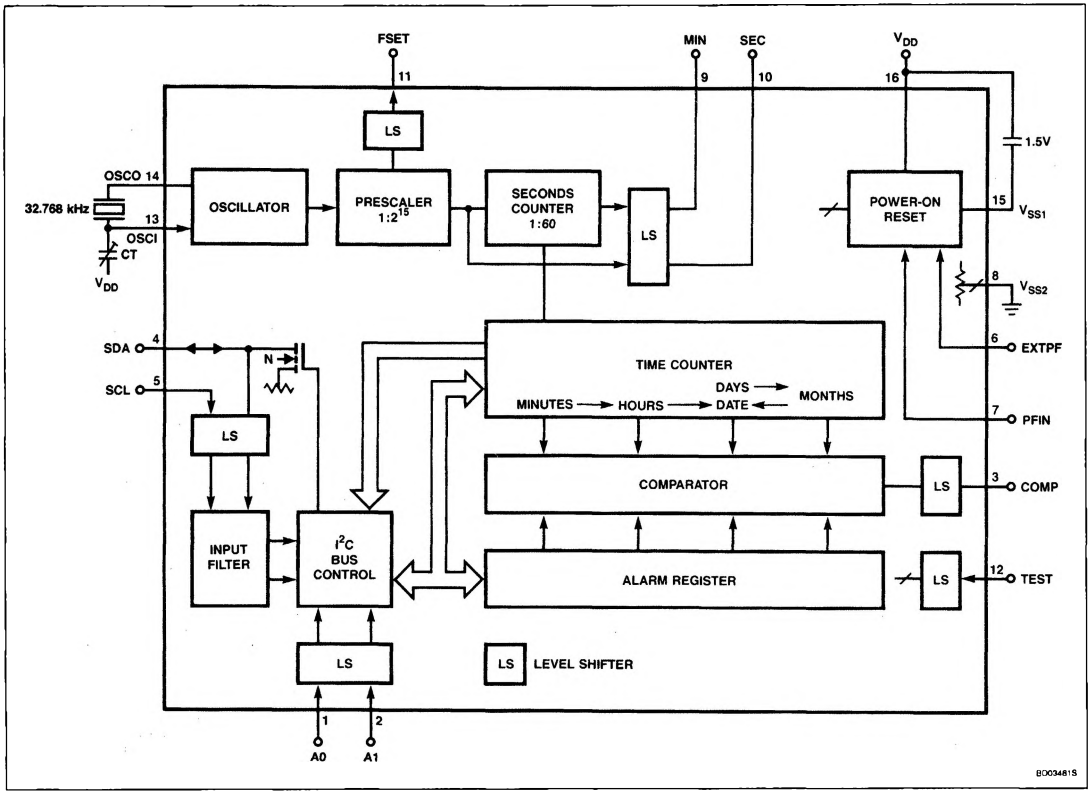
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP (SOT-38)	−40°C to +85°C	PCF8573PN
16-Pin Plastic SOL (SOT-162A)	−40°C to +85°C	PCF8573T

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Supply voltage range (clock)	−0.3 to 8	V
V_{SS2}	Supply voltage range (I^2C interface)	−0.3 to 8	V
I_{IN}	Input current	10	mA
I_{OUT}	Output current	10	mA
P_D	Maximum power dissipation per package	200	mW
T_A	Operating ambient temperature range	−40 to +85	°C
T_{STG}	Storage temperature range	−65 to +150	°C

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS V_{SS2} = 0V; T_A = −40 to + 85°C, unless otherwise specified. Typical values at T_A = + 25°C.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supply					
$V_{DD} - V_{SS2}$	Supply voltage (I^2C interface)	2.5	5	6.0	V
$V_{DD} - V_{SS1}$	Supply voltage (clock)	1.1	1.5	$(V_{DD} - V_{SS2})$	V
$-I_{SS1}$	Supply current V_{SS1} at $V_{DD} - V_{SS1}$ = 1.5V		3	10	μA
$-I_{SS1}$	at $V_{DD} - V_{SS1}$ = 5V		12	50	μA
$-I_{SS2}$	Supply current V_{SS2} at $V_{DD} - V_{SS2}$ = 5V (I_O = 0mA on all outputs)			50	μA
Inputs SCL, SDA, A0, A1, TEST					
V_{IH}	Input voltage HIGH	0.7 × V_{DD}			V
V_{IL}	Input voltage LOW			0.3 × V_{DD}	V
$\pm I_I$	Input leakage current at $V_I = V_{SS2}$ to V_{DD}			1	μA
Inputs EXTPF, PFIN					
$V_{IH} - V_{SS1}$	Input voltage HIGH	0.7 × $(V_{DD} - V_{SS1})$			V
$V_{IL} - V_{SS1}$	Input voltage LOW	0		0.3 × $(V_{DD} - V_{SS1})$	V
$\pm I_I$	Input leakage current at $V_I = V_{SS1}$ to V_{DD}			1	μA
$\pm I_I$	at T_A = 25°C; $V_I = V_{SS1}$ to V_{DD}			0.1	μA
Outputs SEC, MIN, COMP, FSET (normal buffer outputs)					
V_{OH}	Output voltage HIGH at $V_{DD} - V_{SS2}$ = 2.5V; $-I_O$ = 0.1mA	V_{DD} − 0.4			V
V_{OH}	at $V_{DD} - V_{SS2}$ = 4 to 6V; $-I_O$ = 0.5mA	V_{DD} − 0.4			V
V_{OL}	Output voltage LOW at $V_{DD} - V_{SS2}$ = 2.5V; I_O = 0.3mA			0.4	V
V_{OL}	at $V_{DD} - V_{SS2}$ = 4 to 6V; I_O = 1.6mA			0.4	V
Output SDA (N-Channel open drain)					
V_{OL}	Output 'ON': I_O = 3mA at $V_{DD} - V_{SS2}$ = 2.5 to 6V			0.4	V
I_O	Output 'OFF' (leakage current) at $V_{DD} - V_{SS2}$ = 6V; V_O = 6V			1	μA
Internal Threshold Voltage					
V_{TH1}	Power failure detection	1	1.2	1.4	V
V_{TH2}	Power 'ON' reset at $V_{SCL} = V_{SDA} = V_{DD}$	1.5	2.0	2.5	V

AC ELECTRICAL CHARACTERISTICS

V_{SS2} = 0V; T_A = −40 to + 85°C, unless otherwise specified. Typical values at T_A = + 25°C.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Rise and Fall Times of Input Signals					
t_R, t_F	Input EXTPF			1	μs
t_R, t_F	Input PFIN			∞	μs
	Input signals except EXTPF and PFIN between V_{IL} and V_{IH} levels				
t_R	rise time			1	μs
t_F	fall time			0.3	μs
Frequency at SCL					
	at $V_{DD} - V_{SS2}$ = 4 to 6V				
t_{LOW}	Pulse width LOW (see Figures 7 and 9	4.7			μs
t_{HIGH}	Pulse width HIGH (see Figures 7 and 9	4			μs
t_I	Noise suppression time constant at SCL and SDA input	0.25	1	2.5	μs
c_{IN}	Input capacitance (SCL, SDA)			7	pF
Oscillator					
C_{OUT}	Integrated oscillator capacitance		40		pF
R_F	Oscillator feedback resistance		3		MΩ
	Oscillator stability for: $\Delta(V_{DD} - V_{SS1})$ = 100mV at $V_{DD} - V_{SS1}$ = 1.55V;				
f/f_{OSC}	T_A = 25°C		2×10^{-6}		
	Quartz crystal parameters				
	Frequency = 32.768 kHz				
R_S	Series resistance			40	kΩ
C_L	Parallel capacitance		9		pF
C_T	Trimmer capacitance	5		25	pF

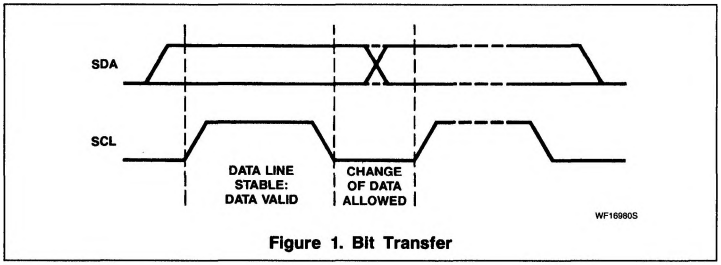


Figure 1. Bit Transfer

Table 1. Cycle Length of the Time Counter

UNIT	NUMBER OF BITS	COUNTING CYCLE	CARRY FOR FOLLOWING UNIT	CONTENT OF MONTH COUNTER
Minutes	7	00 to 59	59 → 00	
Hours	6	00 to 23	23 → 00	
Days	6	01 to 28	28 → 01	} 2 (see note)
			or 29 → 01	
		01 to 30	30 → 01	4, 6, 9, 11
		01 to 31	31 → 01	1, 3, 5, 7, 8, 10, 12
Months	5	01 to 12	12 → 01	

NOTE: Day counter may be set to 29 by a write transmission with EXECUTE ADDRESS.

FUNCTIONAL DESCRIPTION

Oscillator

The PCF8573 has an integrated crystal-controlled oscillator which provides the time base for the prescaler. The frequency is determined by a single 32.768kHz crystal connected between OSCI and OSCO. A trimmer is connected between OSCI and V_{DD}.

Prescaler and Time Counter

The prescaler provides a 128Hz signal at the FSET output for fine adjustment of the crystal oscillator without loading it. The prescaler also generates a pulse once a second to advance the seconds counter. The carry of the prescaler and the seconds counter are available at the outputs SEC and MIN, respectively, and are also readable via the I^2C bus. The mark-to-space ratio of both signals is 1:1. The time counter is advanced one count by the falling edge of output signal MIN. A transition from HIGH to LOW of output signal SEC triggers MIN to change state. The time counter counts minutes, hours, days and months, and provides a full calendar function which needs to be corrected once every four years. Cycle lengths are shown in Table 1.

Alarm Register

The alarm register is a 24-bit memory. It stores the time-point for the next setting of the status flag COMP. Details of writing and reading of the alarm register are included in the description of the characteristics of the I^2C bus.

Table 2. Power Fail Selection

EXTPF	PFIN	FUNCTION
0	0	Power fail is sensed internally
0	1	Test mode
1	0	Power fail is sensed externally
1	1	No power fail sensed

NOTE:
0: connected to V_{SS1} (LOW)
1: connected to V_{DD} (HIGH)

Comparator

The comparator compares the contents of the alarm register and the time counter, each with a length of 24 bits. When these contents are equal, the flag COMP will be set 4ms after the falling edge of MIN. This set condition occurs once at the beginning of each minute. This information is latched, but can be cleared by an instruction via the I^2C bus. A clear instruction may be transmitted immediately after the flag is set, and then it will be executed. Flag COMP information is also available at the output COMP. The comparison may be based upon hours and minutes only if the internal flag NODA (no date) is set. Flag NODA can be set and cleared by separate instructions via the I^2C bus, but it is undefined until the first set or clear instruction has been received. Both COMP and NODA flags are readable via the I^2C bus.

Power On/Power Fail Detection

If the voltage $V_{DD} - V_{SS1}$ falls below a certain value, the operation of the clock becomes undefined. Thus, a warning signal is required to indicate that faultless operation of the clock is not guaranteed. This information is latched in a flag called POWF (Power Fail) and remains latched after restoration of the correct supply voltage until a write procedure with EXECUTIVE ADDRESS has been received. The flag POWF can be set by an internally-generated power fail level-discriminator signal for application with $(V_{DD} - V_{SS1})$ greater than V_{TH1}, or by an externally-generated power fail signal for application with $(V_{DD} - V_{SS1})$ less than V_{TH1}. The external signal must be applied to the input PFIN. The input stage operates with signals of any slow rise and fall times. Internally-or externally-controlled POWF can be selected by input EXTPF as shown in Table 2.

The external power fail control operates by absence of the $V_{DD} - V_{SS2}$ supply. Therefore, the input levels applied to PFIN and EXTPF must be within the range of $V_{DD} - V_{SS1}$. A LOW level at PFIN indicates a power fail. POWF is readable via the I^2C bus. A power-on reset for the I^2C bus control is generated on-chip when the supply voltage $V_{DD} - V_{SS2}$ is less than V_{TH2}.

Interface Level Shifters

The level shifters adjust the 5V operating voltage ($V_{DD} - V_{SS2}$) of the microcontroller to the internal supply voltage ($V_{DD} - V_{SS1}$) of the clock/calendar. The oscillator and counter are not influenced by the $V_{DD} - V_{SS2}$ supply voltage. If the voltage $V_{DD} - V_{SS2}$ is absent ($V_{SS2} = V_{DD}$) the output signal of the level shifter is HIGH because V_{DD} is the common node of the $V_{DD} - V_{SS2}$ and the $V_{DD} - V_{SS1}$ supplies. Because the level shifters invert the input signal, the internal circuit behaves as if a LOW signal is present on the inputs. FSET, SEC, MIN and COMP are CMOS push-pull output stages. The driving capability of these outputs is lost when the supply voltage $V_{DD} - V_{SS2} = 0$.

CHARACTERISTICS OF THE I^2C BUS

The I^2C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit Transfer (see Figure 1)

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

Start and Stop Conditions (see Figure 2)

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

System Configuration (see Figure 3)

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

Acknowledge (see Figure 4)

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge-related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse. So that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, setup and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a stop condition (see Figures 11 and 12).

Timing Specifications

Within the I^2C bus specifications a high-speed mode and a low-speed mode are defined. The PCF8573 operates in both modes and the timing requirements are as follows:

High-Speed Mode — Masters generate a bus clock with a maximum frequency of 100kHz. Detailed timing is shown in Figure 5.

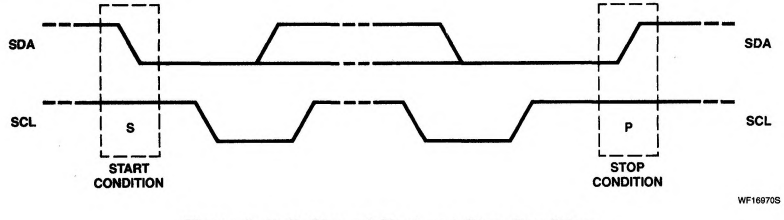


Figure 2. Definition of Start and Stop Conditions

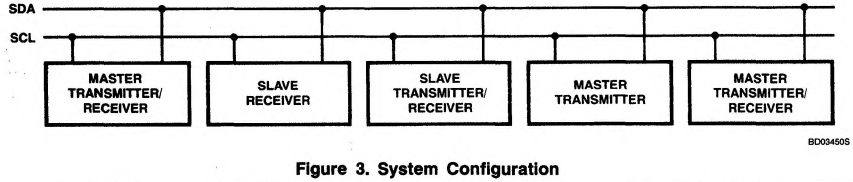


Figure 3. System Configuration

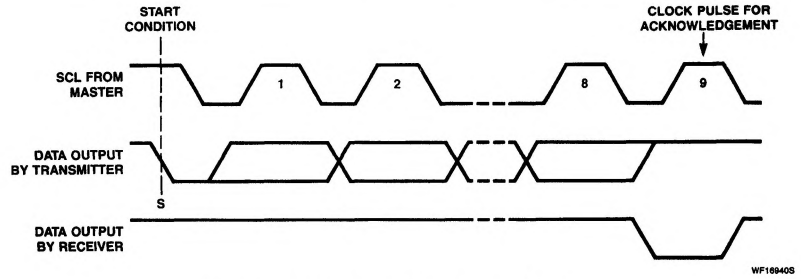
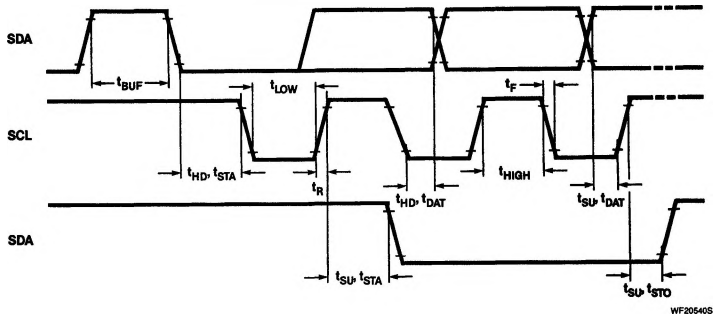


Figure 4. Acknowledgement on the I^2C Bus

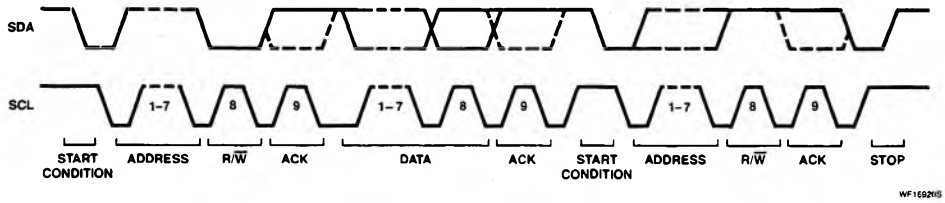


Where:

t_{BUF}	$t \geq t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
t_{HD}, t_{STA}	$t \geq t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4.7μs	Clock LOW period
$t_{HIGHmin}$	4μs	Clock HIGH period
t_{SU}, t_{STA}	$t \geq t_{LOWmin}$	Start condition setup time, only valid for repeated start code
t_{HD}, t_{DAT}	$t \geq 0\mu s$	Data hold time
t_{SU}, t_{DAT}	$t \geq 250ns$	Data setup time
t_R	$t \leq 1\mu s$	Rise time of both the SDA and SCL line
t_F	$t \leq 300ns$	Fall time of both the SDA and SCL line
t_{SU}, t_{STO}	$t \geq t_{LOWmin}$	Stop condition setup time

NOTE:
1. All the values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{DD} to V_{SS2}.

Figure 5. Timing of the High-Speed Mode

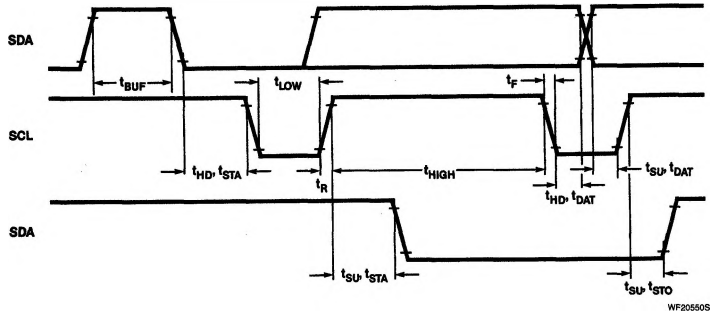


Where:

Clock t_{LOWmin}	4.7μs
$t_{HIGHmin}$	4μs
The dashed line is the acknowledgement of the receiver	
Mark-to-space ratio	1:1 (LOW-to-HIGH)
Max. number of bytes	unrestricted
Premature termination of transfer	allowed by generation of STOP condition
Acknowledge clock bit	must be provided by the master

Figure 6. Complete Data Transfer in the High-Speed Mode

Low-Speed Mode — Masters generate a bus clock with a maximum frequency of 2kHz; a minimum LOW period of 105μs and a minimum HIGH period of 365μs. The mark-to-space ratio is 1:3 LOW-to-HIGH. Detailed timing is shown in Figure 7.



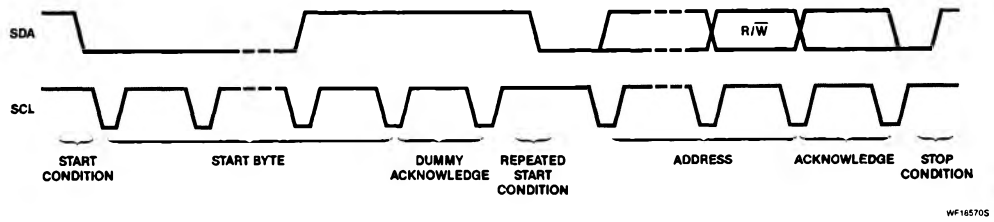
Where:

t_{BUF}	$t \geq 105\mu s$ (t_{LOWmin})
t_{HD}, t_{STA}	$t \geq 365\mu s$ ($t_{HIGHmin}$)
t_{LOW}	130μs ± 25μs
t_{HIGH}	390μs ± 25μs
t_{SU}, t_{STA}	130μs ± 25μs*
t_{HD}, t_{DAT}	$t \geq 0\mu s$
t_{SU}, t_{DAT}	$t \geq 250ns$
t_R	$t \leq 1\mu s$
t_F	$t \leq 300ns$
t_{SU}, t_{STO}	130μs ± 25μs

*Only valid for repeated start code.

NOTE:
1. All the values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{DD} to V_{SS2}; for definitions see high-speed mode.

Figure 7. Timing of the Low-Speed Mode



Where:

Clock t_{LOWmin}	130μs ± 25μs
$t_{HIGHmin}$	390μs ± 25μs
Mark-to-space ratio	1:3 (LOW-to-HIGH)
Start byte	0000 0001
Maximum number of bytes	6
Premature termination of transfer	not allowed
Acknowledge clock bit	must be provided by master

NOTE:
1. The general characteristics and detailed specification of the I^2C bus are described in a separate data sheet (serial data buses) in handbook: *ICs for digital systems in radio, audio and video equipment.*

Figure 8. Complete Data Transfer in the Low-Speed Mode

ADDRESSING

Before any data is transmitted on the I^2C bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure.

Slave Address

The clock/calendar acts as a slave receiver or slave transmitter. Therefore, the clock signal SCL is only an input signal, but the data signal SDA is a bidirectional line. The clock calendar slave address is shown in Figure 9.

The subaddress bits A0 and A1 correspond to the two hardware address pins A0 and A1 which allows the device to have 1 of 4 different addresses.

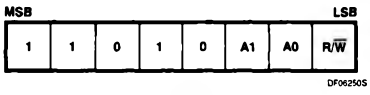


Figure 9. Slave Address

Clock/Calendar READ/WRITE Cycles

The I^2C bus configuration for different clock/calendar READ and WRITE cycles is shown in Figures 10 and 11.

The write cycle is used to set the time counter, the alarm register and the flags. The transmission of the clock/calendar address is followed by the MODE-POINTER-WORD which contains a CONTROL-nibble (Table 3) and an ADDRESS-nibble (Table 4). The ADDRESS-nibble is valid only if the preceding CONTROL-nibble is set to EXECUTE ADDRESS. The third transmitted word contains the data to be written into the time counter or alarm register.

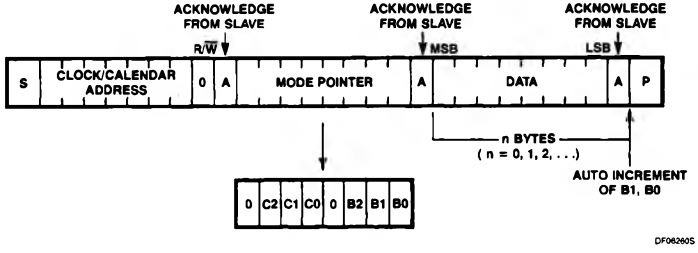


Figure 10. Master Transmitter Transmits to Clock/Calendar Slave Receiver

Table 3. CONTROL-nibble

	C2	C1	C0	FUNCTION
0	0	0	0	Execute address
0	0	0	1	Read control/status flags
0	0	1	0	Reset prescaler, including seconds counter; without carry for minute counter
0	0	1	1	Time adjust, with carry for minute counter[1]
0	1	0	0	Reset NODA flag
0	1	0	1	Set NODA flag
0	1	1	0	Reset COMP flag

NOTE:
1. If the seconds counter is below 30 there is no carry. This causes a time adjustment of max. −30 sec. From the count 30 there is a carry which adjusts the time by max. +30 sec.

At the end of each data word the address bits B1, B0 will be incremented automatically provided the preceding CONTROL-nibble is set to EXECUTE ADDRESS. There is no carry to B2.

Table 5 shows the placement of the BCD upper and lower digits in the DATA byte for writing into the addressed part of the time counter and alarm register, respectively.

Acknowledgement response of the clock calendar as slave receiver is shown in Table 6.

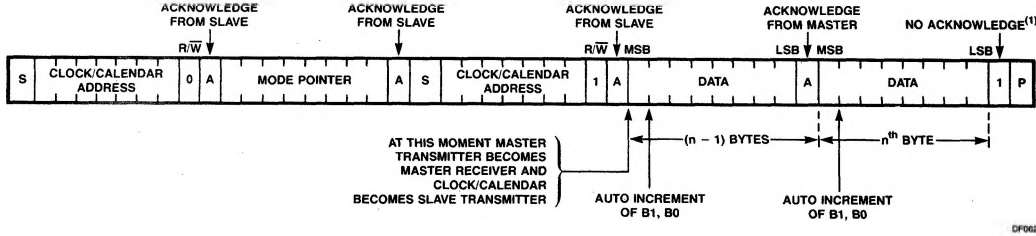
Table 4. ADDRESS-nibble

	B2	B1	B0	ADDRESSED TO:
0	0	0	0	Time counter hours
0	0	0	1	Time counter minutes
0	0	1	0	Time counter days
0	0	1	1	Time counter months
0	1	0	0	Alarm register hours
0	1	0	1	Alarm register minutes
0	1	1	0	Alarm register days
0	1	1	1	Alarm register months

Table 5. Placement of BCD Digits in the DATA Byte

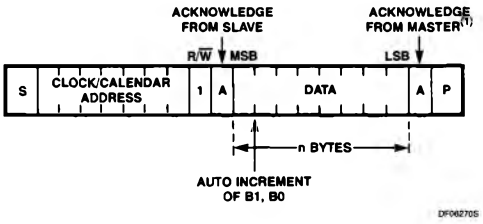
MSB				DATA			LSB	
UPPER DIGIT				LOWER DIGIT				
UD	UC	UB	UA	LD	LC	LB	LA	ADDRESSED TO:
X	X	D	D	D	D	D	D	Hours
X	D	D	D	D	D	D	D	Minutes
X	X	D	D	D	D	D	D	Days
X	X	X	D	D	D	D	D	Months

NOTE:
1. Where "X" is the don't care bit and "D" is the data bit.



NOTE:
The master receiver must signal an end-of-data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave.

Figure 11. Master Transmitter Reads Clock/Calendar After Setting Mode Pointer



NOTE:
The master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave.

Figure 12. Master Reads Clock/Calendar Immediately After First Byte

To read the addressed part of the time counter and alarm register, plus information from specified control/status flags, the BCD digits in the DATA byte are organized as shown in Table 7.
The status of the MODE-POINTER-WORD concerning the CONTROL-nibble remains unchanged until a write to MODE POINTER conditon occurs.

Table 6. Slave Receiver Acknowledgement

MODE POINTER								ACKNOWLEDGE ON BYTE		
								Address	Mode pointer	Data
	C2	C1	C0		B2	B1	B0			
0	0	0	0	0	X	X	X	yes	yes	yes
0	0	0	0	1	X	X	X	yes	no	no
0	0	0	1	X	X	X	X	yes	yes	no
0	0	1	0	X	X	X	X	yes	yes	no
0	0	1	1	X	X	X	X	yes	yes	no
0	1	0	0	X	X	X	X	yes	yes	no
0	1	0	1	X	X	X	X	yes	yes	no
0	1	1	0	X	X	X	X	yes	yes	no
0	1	1	1	X	X	X	X	yes	no	no
1	X	X	X	X	X	X	X	yes	no	no

NOTE:
1. Where "X" is the don't care bit.

Table 7. Organization of the BCD Digits in the DATA Byte

MSB DATA LSB								ADDRESSED TO:
UPPER DIGIT				LOWER DIGIT				
UD	UC	UB	UA	LD	LC	LB	LA	
0	0	D	D	D	D	D	D	Hours
0	D	D	D	D	D	D	D	Minutes
0	0	D	D	D	D	D	D	Days
0	0	0	D	D	D	D	D	Months
0	0	0	*	**	NODA	COMP	POWF	Control/status flags

NOTES:
1. Where: "D" is the data bit, * = minutes, ** = seconds.

APPLICATION INFORMATION

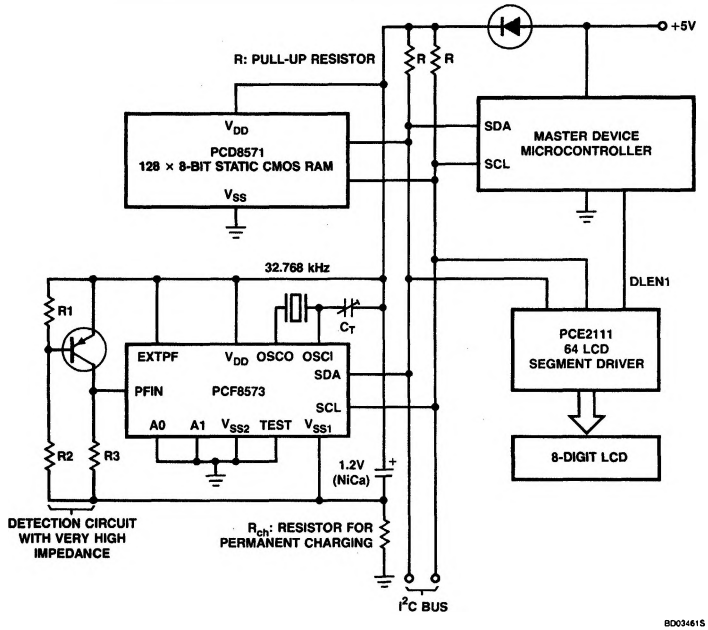


Figure 13. Application Example of the PCF8573 Clock/Calendar

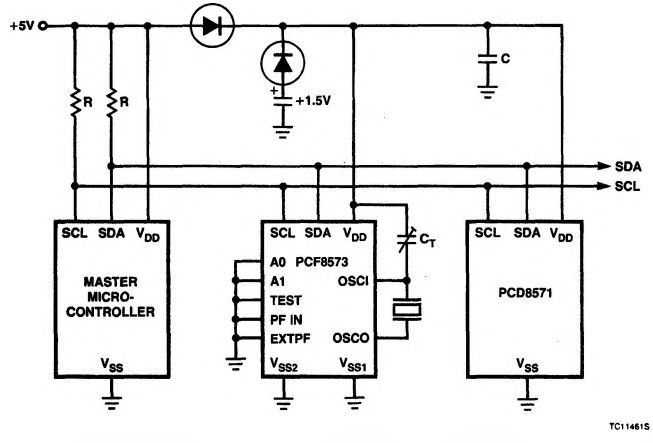


Figure 14. Application Example of the PCF8573 With Common V_{SS1} and V_{SS2} Supply