# Signetics

## PCF8570
## 256 × 8 Static RAM

### Product Specification

**Linear Products**

## DESCRIPTION
The PCF8570 is a low power 2048-bit static CMOS RAM organized as 256 words by 8-bits. Addresses and data are transferred serially via a two-line bidirectional bus ($I^2C$). The built-in word address register is incremented automatically after each written or read data byte. Three address pins — A0, A1, and A2 — are used for programming the hardware address, allowing the use of up to eight devices connected to the bus without additional hardware.
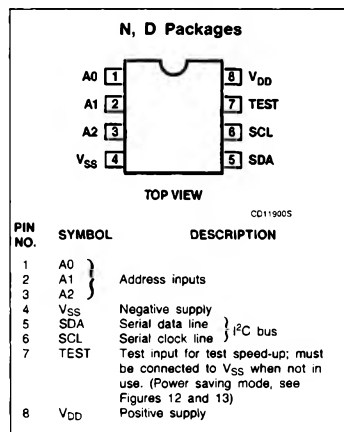
## FEATURES
- **Operating supply voltage: 2.5V to 6V**
- **Low data retention voltage: min. 1.0V**
- **Low standby current: max. 5$\mu$A**
- **Power saving mode: typ. 50nA**
- **Serial input/output bus ($I^2C$)**
- **Address by 3 hardware address pins**
- **Automatic word address incrementing**
- **8-lead DIP package**

## APPLICATIONS
- **Telephony RAM expansion for stored numbers in repertory dialing (e.g., PCD3343 applications)**
- **Radio and television channel presets**
- **Video cassette recorder**
- **General purpose RAM expansion for the microcomputer families MAB8400 and PCF84C00**

## PIN CONFIGURATION

N, D Packages

| | | |
|---|---|---|
| A0 [1] | | [8] $V_{DD}$ |
| A1 [2] | | [7] TEST |
| A2 [3] | | [6] SCL |
| $V_{SS}$ [4] | | [5] SDA |

**TOP VIEW**

CD11900S

| PIN NO. | SYMBOL | DESCRIPTION |
|---|---|---|
| 1 | A0 | |
| 2 | A1 | Address inputs |
| 3 | A2 | |
| 4 | $V_{SS}$ | Negative supply |
| 5 | SDA | Serial data line $\}$ $I^2C$ bus |
| 6 | SCL | Serial clock line |
| 7 | TEST | Test input for test speed-up; must be connected to $V_{SS}$ when not in use. (Power saving mode, see Figures 12 and 13) |
| 8 | $V_{DD}$ | Positive supply |

## ORDERING INFORMATION

| DESCRIPTION | TEMPERATURE RANGE | ORDER CODE |
|---|---|---|
| 8-Pin Plastic DIP (SOT-97A) | −40°C to +85°C | PCF8570PN |
| 8-Pin Plastic SO (SO-8L; SOT-176) | −40°C to +85°C | PCF8570TD |

## ABSOLUTE MAXIMUM RATINGS

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $V_{DD}$ | Supply voltage range (Pin 8) | −0.8 to +8.0 | V |
| $V_I$ | Voltage range on any input | −0.8 to $V_{DD}$ +0.8 | V |
| ± $I_I$ | DC input current (any input) | 10 | mA |
| ± $I_O$ | DC output current (any output) | 10 | mA |
| ± $I_{DD}$; $I_{SS}$ | Supply current (Pin 4 or Pin 8) | 50 | mA |
| $P_{TOT}$ | Power dissipation per package | 300 | mW |
| $P_O$ | Power dissipation per output | 50 | mW |
| $T_{STG}$ | Storage temperature range | −65 to +150 | °C |
| $T_A$ | Operating ambient temperature range | −40 to +85 | °C |

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## BLOCK DIAGRAM
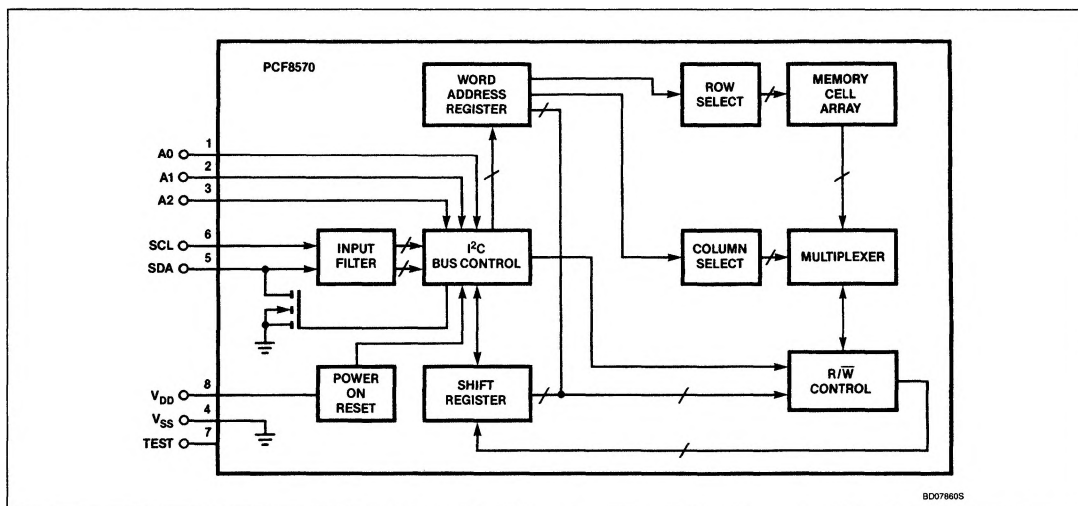


## DC ELECTRICAL CHARACTERISTICS $V_{DD}$ = 2.5 to 6V; $V_{SS}$ = 0V; $T_A$ = −40°C to +85°C, unless otherwise specified.

| SYMBOL | PARAMETER | LIMITS | | | UNIT |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| **Supply** | | | | | |
| $V_{DD}$ | Supply voltage | 2.5 | | 6 | V |
| $I_{DD}$ $I_{DDO}$ $I_{DDO}$ | Supply current at $f_{SCL}$ = 100kHz; $V_I$ = $V_{SS}$ or $V_{DD}$ operating standby standby at $T_A$ = −25 to +70°C | | | 200 15 5 | μA μA μA |
| $V_{POR}$ | Power-on reset voltage level[1] | 1.5 | 1.9 | 2.3 | V |
| **Input SCL; input/output SDA** | | | | | |
| $V_{IL}$ | Input voltage LOW[2] | −0.8 | | 0.3 × $V_{DD}$ | V |
| $V_{IH}$ | Input voltage HIGH[2] | 0.7 × $V_{DD}$ | | $V_{DD}$ + 0.8 | V |
| $I_{OL}$ | Output current LOW at $V_{OL}$ = 0.4V | 3 | | | mA |
| $I_{OH}$ | Output leakage current HIGH at $V_{OH}$ = $V_{DD}$ | | | 250 | nA |
| ± $I_I$ | Input leakage current (A0, A1, A2) at $V_I$ = $V_{DD}$ or $V_{SS}$ | | | 250 | nA |
| $f_{SCL}$ | Clock frequency (Figure 5) | 0 | | 100 | kHz |
| $C_I$ | Input capacitance (SCL, SDA) at $V_I$ = $V_{SS}$ | | | 7 | pF |
| $t_{SW}$ | Tolerable spike width on bus | | | 100 | ns |
| **LOW $V_{DD}$ data retention** | | | | | |
| $V_{DDR}$ | Supply voltage for data retention | 1 | | 6 | V |
| $I_{DDR}$ | Supply current at $V_{DDR}$ = 1V | | | 5 | μA |
| $I_{DDR}$ | Supply current at $V_{DDR}$ = 1V; $T_A$ = −25 to +70°C | | | 2 | μA |
| **Power saving mode** | | | | | |
| $I_{DDR}$ | Supply current at $T_A$ = 25°C; TEST = $V_{DDR}$ | | 50 | 400 | nA |

**NOTES:**
1. The power-on reset circuit resets the I²C bus logic when $V_{DD}$ < $V_{POR}$.
2. If the input voltages are a diode voltage above or below the supply voltage $V_{DD}$ or $V_{SS}$ an input current will flow; this current must not exceed ± 0.5mA.

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## CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

## Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse, as changes in the data line at this time will be interpreted as control signals.
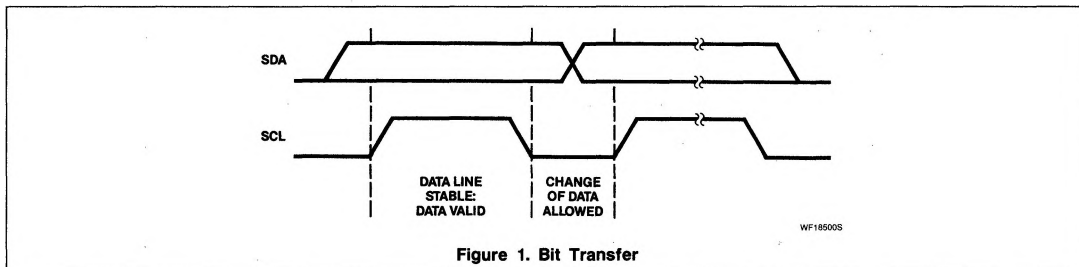


**Figure 1. Bit Transfer**

## Start and Stop Conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).
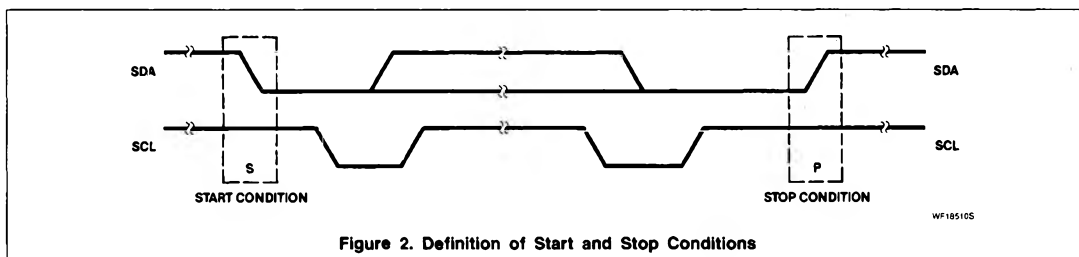


**Figure 2. Definition of Start and Stop Conditions**

## System Configuration

A device generating a message is a "transmitter"; a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".
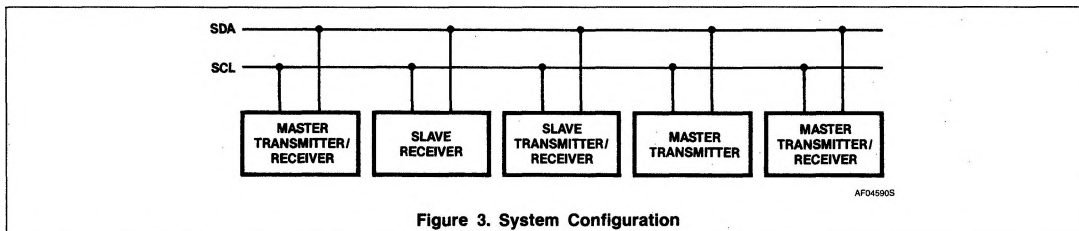


**Figure 3. System Configuration**

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## Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. During the HIGH period of the acknowledge related clock pulse, setup and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.
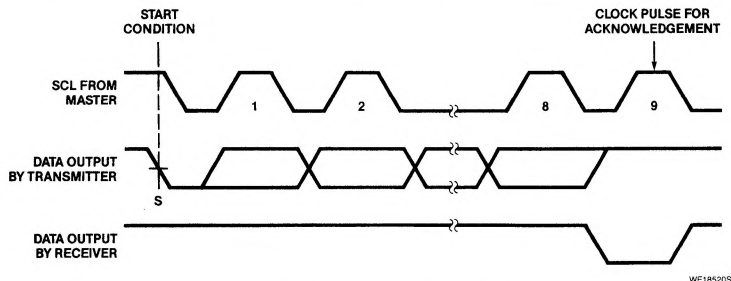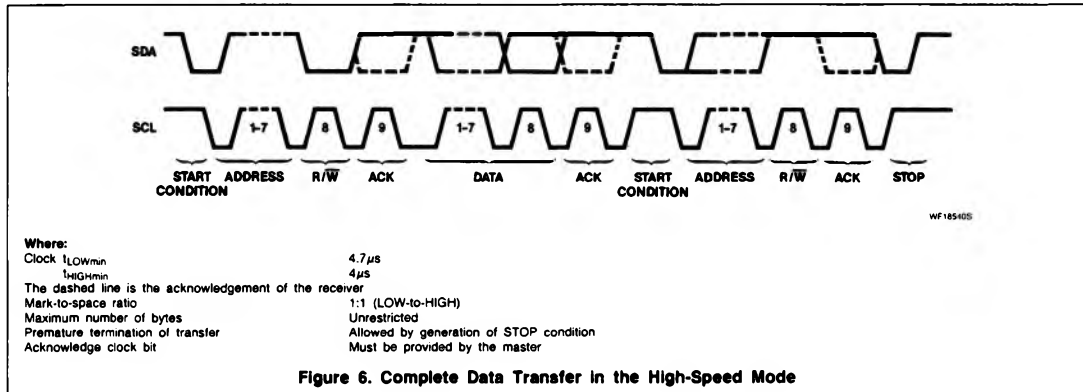


Figure 4. Acknowledge on the I$^2$C Bus
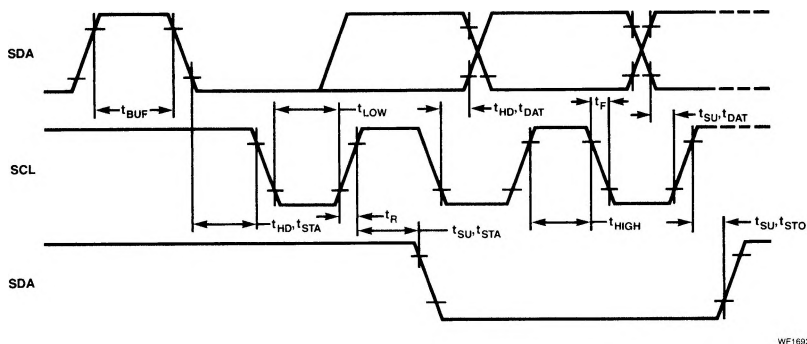


**Where:**

| | | |
|---|---|---|
| $t_{BUF}$ | $t \geqslant t_{LOWmin}$ | The minimum time the bus must be free before a new transmission can start |
| $t_{HD;STA}$ | $t \geqslant t_{HIGHmin}$ | Start condition hold time |
| $t_{LOWSmin}$ | 4.7μs | Clock LOW period |
| $t_{HIGHmin;}$ | 4μs | Clock HIGH period |
| $t_{SU;STA}$ | $t \geqslant t_{LOWmin}$ | Start condition set-up time; only valid for repeated start code |
| $t_{HD;DAT}$ | $t = 0$μs | Data hold time |
| $t_{SU;DAT}$ | $t \geqslant 250$ns | Data setup time |
| $t_R$ | $t \leqslant 1$μs | Rise time of both the SDA and SCL line |
| $t_F$ | $t \leqslant 300$ns | Fall time of both the SDA and SCL line |
| $t_{SU;STO}$ | $t \geqslant t_{LOWmin}$ | Stop condition setup time |

**NOTE:**
All the timing values refer to $V_{IH}$ and $V_{IL}$ levels with a voltage swing of $V_{SS}$ to $V_{DD}$.

Figure 5. Timing

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**Where:**

| | |
|---|---|
| Clock $t_{LOWmin}$ | 4.7μs |
| $t_{HIGHmin}$ | 4μs |
| The dashed line is the acknowledgement of the receiver | |
| Mark-to-space ratio | 1:1 (LOW-to-HIGH) |
| Maximum number of bytes | Unrestricted |
| Premature termination of transfer | Allowed by generation of STOP condition |
| Acknowledge clock bit | Must be provided by the master |

**Figure 6. Complete Data Transfer in the High-Speed Mode**

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## Bus Protocol

Before any data is transmitted on the I²C bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure. The I²C bus configuration for different PCF8570 READ and WRITE cycles is shown in Figure 7.
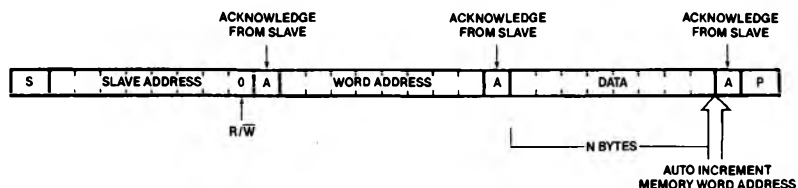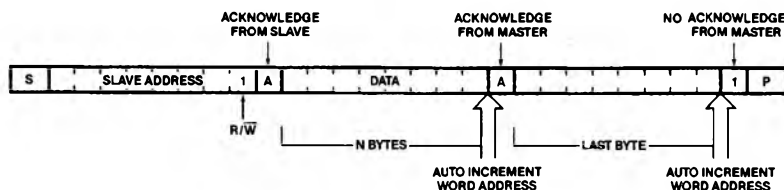


a. Master Transmits to Slave Receiver (WRITE Mode)
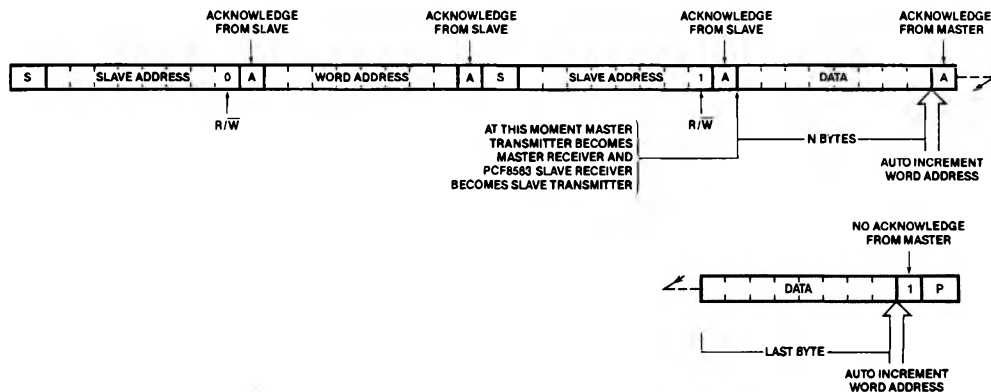
b. Master Reads After Setting Word Address (WRITE Word Address; READ Data)

c. Master Reads Slave Immediately After First Byte (READ Mode)
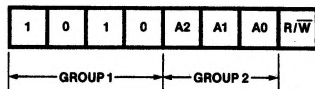
Figure 7

## 256 × 8 Static RAM                                                    PCF8570

## APPLICATION INFORMATION

The PCF8570 slave address has a fixed combination 1010 as group 1, while group 2 is fully programmable (see Figure 8.)
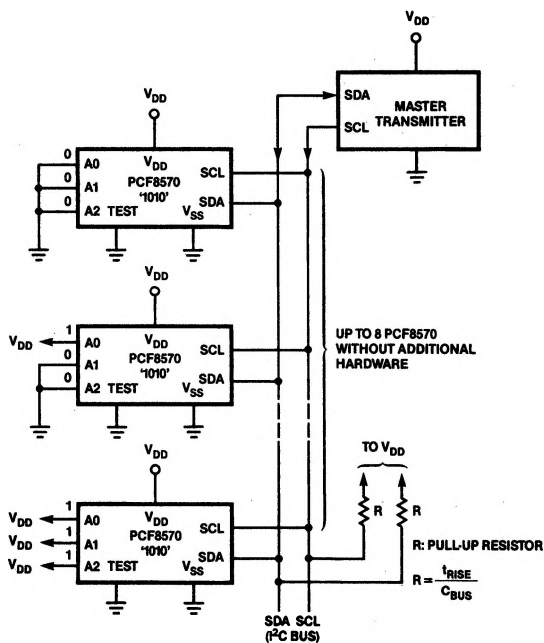


**NOTE:**
PCF8570A version: the slave address A0 state is X (don't care); however, the hardware address A0 input must still be connected to $V_{SS}$ or $V_{DD}$.

**Figure 8. PCF8570 Address**



**NOTE:**
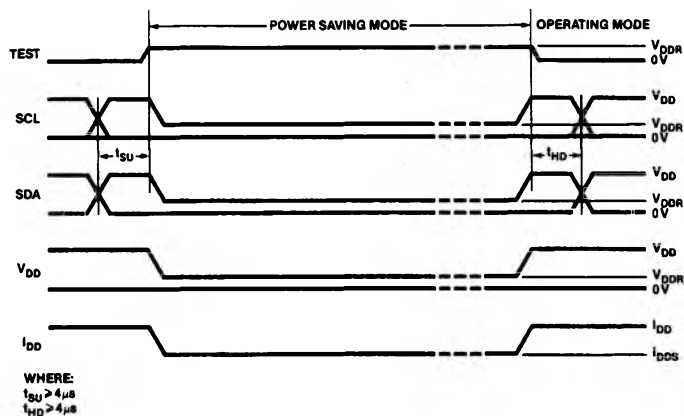A0, A1, and A2 inputs must be connected to $V_{DD}$ or $V_{SS}$ but not left open.

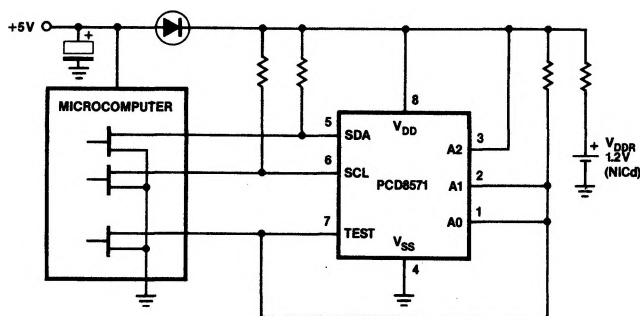**Figure 9. PCF8570 Application Diagram**

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## POWER SAVING MODE

With the condition TEST = $V_{DDR}$, the PCF8570 goes into the power saving mode.



**Figure 10. Timing for Power Saving Mode**



NOTE:
1. In the operating mode, TEST = 0.
2. In the power saving mode, TEST = $V_{DDR}$.

**Figure 11. Application Example for Power Saving Mode**