## PAL10/10016P8 ECL Programmable Array Logic

## General Description

The PAL1016P8/10016P8 is the first member of an ECL programmable logic device family possessing common electrical characteristics, utilizing an easily accommodated programming procedure, and produced with National Semiconductor's advanced oxide-isolated process. This family includes combinatorial, and registered output devices.
These devices are fabricated using National's proven Ti-W (Titanium-Tungsten) fuse technology to allow fast, efficient, and reliable programming.
This family allows the designer to quickly implement the defined logic function by removing the fuses required to properly configure the internal gates and/or registers. Product terms with all fuses removed assume a logical high state. All devices in this series are provided with an output polarity fuse that, if removed, will permit any output to independently provide a logic low when the equation is satisfied. When these fuses are intact the outputs provide a logic true (most positive voltage level) in response to the input conditions defined by the applicable equation. All input and I/O pins have on-chip $50 \mathrm{k} \Omega$ pull-down resistors.

Fuse symbols have been omitted from the logic diagrams to allow the designer use of the diagrams to create fuse maps representing the programmed device.
All devices in this family can be programmed using conventional programmers. After the device has been programmed and verified, an additional fuse may be removed to inhibit further verification or programming. This "security" feature can provide a proprietary circuit which cannot easily be duplicated.

## Features

- tpD $=6$ ns max
- Eight combinatorial outputs with programmable polarity
- Programmable replacement for conventional ECL logic
m Both 10 KH and 100 K I/O compatible versions
- Simplifies prototyping and board layout
- 24-pin thin DIP packages.
a Programmed on conventional TTL PLD programmers
- Security fuse to prevent direct copying
- Reliable titanium-tungsten fuses


## Ordering Information



## Absolute Maximum Ratings

If Military/Aerospace specified devices are required,
please contact the National Semiconductor Sales
Office/Distributors for avallability and specifications.
Temperature Under Bias (Ambient)
$-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$
$-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$
$\begin{array}{ll}V_{E E} \text { Relative to } V_{C C} & -7 \mathrm{~V} \text { to }+0.5 \mathrm{~V} \\ \text { Any Input Relative to } \mathrm{V}_{\mathrm{CC}} & \mathrm{V}_{\mathrm{EE}} \text { to }+0.5 \mathrm{~V}\end{array}$

Lead Temperature (Soldering, 10 seconds)
$300^{\circ} \mathrm{C}$
ESD Tolerance
1000V
$C_{\text {ZAP }}=100 \mathrm{pF}$ $R_{\text {ZAP }}=1500 \Omega$
Test Method: Human Body Model
Test Specification: NSC SOP-5-028

Recommended Operating Conditions

| Symbol | Parameter |  | Min | Typ | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| VEE | Supply Voltage | 10 kH | -5.46 | -5.2 | -4.94 | V |
|  |  | 100k | -4.73 | -4.5 | -4.27 |  |
| $\mathrm{R}_{\mathrm{L}}$ | Standard $10 \mathrm{kH} / 100 \mathrm{k}$ Load |  |  | 50 |  | $\Omega$ |
| $C_{L}$ | Standard $10 \mathrm{kH} / 100 \mathrm{k}$ Load |  |  | 5 |  | pF |
| $\mathrm{T}_{\text {A }}$ | Operating Ambient Temperature | 10 kH | 0 |  | +75 | ${ }^{\circ} \mathrm{C}$ |
|  |  | 100k | 0 |  | +85 |  |

Electrical Characteristics Over Recommended Operating Conditions. Output Load $=50 \Omega$ to -2.0 V .

| Symbol | Parameter | Conditions |  | $\mathrm{T}_{\mathbf{A}}$ | Min | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{IH}}$ | High Level Input Voltage | Guaranteed input voltage high for all inputs | 10 kH | $\begin{gathered} \\ 0^{\circ} \mathrm{C} \\ + \\ +25^{\circ} \mathrm{C} \\ +75^{\circ} \mathrm{C} \end{gathered}$ | $\begin{aligned} & -1170 \\ & -1130 \\ & -1070 \end{aligned}$ |  | mV |
|  |  |  | 100k | $0^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$ | -1165 | -880 |  |
| $V_{\text {IL }}$ | Low Level Input Voltage | Guaranteed input voltage low for all inputs | 10 kH | $\begin{gathered} \\ 0^{\circ} \mathrm{C} \\ + \\ +25^{\circ} \mathrm{C} \\ +75^{\circ} \mathrm{C} \end{gathered}$ |  | $\begin{aligned} & -1480 \\ & -1480 \\ & -1450 \end{aligned}$ | mV |
|  |  |  | 100k | $0^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$ | -1810 | -1475 |  |
| $\mathrm{V}_{\mathrm{OH}}$ | High Level Output Voltage | $\mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\text {IH }}$ Max. or $\mathrm{V}_{\text {IL }}$ Min. | 10 kH | $\begin{gathered} 0^{\circ} \mathrm{C} \\ + \\ +25^{\circ} \mathrm{C} \\ +75^{\circ} \mathrm{C} \end{gathered}$ | $\begin{aligned} & -1020 \\ & -980 \\ & -920 \end{aligned}$ | $\begin{aligned} & -840 \\ & -810 \\ & -735 \end{aligned}$ | mV |
|  |  |  | 100k | $0^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$ | -1025 | -880 |  |
| $\mathrm{V}_{\mathrm{OL}}$ | Low Level Output Voltage | $\mathrm{V}_{\text {IN }}=\mathrm{V}_{\text {IH }}$ Max. or $\mathrm{V}_{\text {IL }}$ Min. | 10 kH | $\begin{aligned} & 0^{\circ} \mathrm{C} \\ + & 25^{\circ} \mathrm{C} \\ + & 75^{\circ} \mathrm{C} \end{aligned}$ | $\begin{array}{r} -1950 \\ -1950 \\ -1950 \\ \hline \end{array}$ | $\begin{array}{r} -1630 \\ -1630 \\ -1600 \\ \hline \end{array}$ | mV |
|  |  |  | 100k | $0^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$ | -1810 | -1620 |  |
| ${ }_{1 / H}$ | High Level Input Current | $\mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{IH}} \mathrm{Max}$. | 10 kH | $\begin{gathered} 0^{\circ} \mathrm{C} \\ +75^{\circ} \mathrm{C} \end{gathered}$ |  | 220 | $\mu \mathrm{A}$ |
|  |  |  | 100k | $0^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$ |  |  |  |
| ILL | Low Level Input Current | $\mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\text {IL }}$ Min. Except I/O Pins | 10 kH | $\begin{gathered} 0^{\circ} \mathrm{C} \\ +75^{\circ} \mathrm{C} \end{gathered}$ | 0.5 |  | $\mu \mathrm{A}$ |
|  |  |  | 100k | $0^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$ |  |  |  |
| ${ }^{\text {I EE }}$ | Supply Current | $\mathrm{V}_{\mathrm{EE}}=$ Max. All inputs and outputs open | 10 kH | $0^{\circ} \mathrm{C}$ to $75^{\circ} \mathrm{C}$ | -240 |  | A |
|  |  |  | 100k | $0^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$ |  |  |  |

Note: This product family has been designed to meet the specification in the test table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained.


TL/L/6161-4

Over Recommended Operating Conditions; Output load: $\mathrm{R}_{\mathrm{L}}=50 \Omega$ to $-2.0 \mathrm{~V}, \mathrm{C}_{\mathrm{L}}=5 \mathrm{pF}$ to GND .

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
| :--- | :--- | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{t}_{\mathrm{pD}}$ | Input to Output |  |  | 4 | 6 | ns |
| $\mathrm{t}_{\mathrm{r}}$ | Output Rise Time |  | 0.5 | 1 | 2.5 | ns |
| $\mathrm{t}_{\mathrm{f}}$ | Output Fall Time |  | 0.5 | 1 | 2.5 | ns |

-Measure tpo at threshold points

## Connection Diagram



## PAL Design

The first step in designing a PAL device is the selection of the appropriate device to accommodate the logic equations. This is accomplished by partitioning the system into logic blocks with a defined number of inputs and outputs. Next, a device with an equal or greater I/O capability is selected to implement each logic block. The assignment of inputs and outputs to specific pins follows the device selection.
This device selection procedure is most easily accomplished with the use of computer software such as the PLANTM package of programs by National Semiconductor Corporation, but can be done manually using the logic diagram and logic symbols provided in this document.

## Specifying the Fuse Pattern

Once a device with pinout is selected, the fuse pattern may be specified. The best procedure is the use of the PLAN, or a similar software package which will create the fuse pattern from the defined logic for the device and download the pattern to a programmer. Most common device programmers are provided with an RS-232 port which accesses the data provided in JEDEC or a selected HEX format.

Logic diagrams can be translated to PAL logic diagrams if desired. Fuses left intact are indicated on the logic diagram by an " $X$ " at the intersection of the input line and the AND gate product line. A blown fuse is not marked. The PAL logic diagrams are provided with no fuse locations marked, allowing the designer to use the diagram to manually create a fuse map. Actually, the unprogrammed device is shipped with all Xs (fuses) intact. Each fuse node is identified by a product line number and an input line number.
Each device in the ECL PAL family has the capability for its output polarity to be user-determined. The selection of output polarity is logically determined by the equations and implemented, if an active low output is required, by removing the fuse representing the appropriate output.

## National Masked Logic

If a large number of devices with the same pattern are required, it may be more economical to consider mask programming. These mask-programmed devices will meet or exceed all of the performance specifications of the fuseprogrammed devices they replace.
To generate a mask-programmed device, National Semiconductor requires a set of logic equations, written in a format such as PLAN, plus test vectors which the user generates as acceptance criteria for the finished product.

## Logic Diagram PAL1016P8/PAL10016P8



TL/L/6161-3
JEDEC logic array cell number $=$ product line first cell number + input line number.

Programming Specification
This specification defines the programming and verification procedure for the first programmable logic devices in Na tionals generic ECL family. The internal fuse arrays consists of 64 product lines ( 8 for each output), each containing 32 fuse locations ( 1 for each of 16 inputs and its complement) for a total of 2048 array fuses. Eight additional fuses exist to allow changing the active output polarity.

Each ECL device is programmed and verified as a $2048 \times 1$ TTL PROM. The connection diagrams in Figure 1 illustrate the difference between the logical ECL device and the PROGRAMMABLE TTL device.
For a list of current software and programming support tools available for these devices, please contact your local Na tional Semiconductor sales representative or distributor.

TTL PROGRAMMING


TL/L/6161-5
FIGURE 1. Connection Dlagrams

ECL LOGIC


## Array Fuse Addressing

When programming or verifying a fuse location, the output (equation) is addressed by the 3 address pins 13, 14, and 15. The eight product lines, within the equation, are selected by the 3 address pins 9,10 , and 11 . The fuse pair locations representing the logical inputs are selected by the 4 address pins 2, 3, 22, and 23, with the complementing fuse within the pair by the address pin 1 . The programming address data is detailed in Tables I-III.

Table I. Logic Output (Equation) Selection vs. Programming Address Inputs.

| Output <br> Pin | Address Pin |  |  |
| :---: | :---: | :---: | :---: |
|  | 15 | 14 | 13 |
| 21 | 0 | 0 | 0 |
| 4 | 0 | 0 | 1 |
| 20 | 0 | 1 | 0 |
| 5 | 0 | 1 | 1 |
| 18 | 1 | 0 | 0 |
| 7 | 1 | 0 | 1 |
| 17 | 1 | 1 | 0 |
| 8 | 1 | 1 | 1 |

Note that the sequence of outputs represent the physical, not numeric, order of logical outputs.

Table II. Product Line (within Equation, or Output) vs. Programming Address Inputs.

| Product <br> Pin | Address Pin |  |  |
| :---: | :---: | :---: | :---: |
|  | 11 | 10 | 9 |
| 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 |
| 2 | 0 | 1 | 0 |
| 3 | 0 | 1 | 1 |
| 4 | 1 | 0 | 0 |
| 5 | 1 | 0 | 1 |
| 6 | 1 | 1 | 0 |
| 7 | 1 | 1 | 1 |

Table III. Input Line Selection vs. Programming Address Inputs.

| Input Line | Address Pin |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | 23 | 22 | 3 | 2 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 1 |
| 2 | 0 | 0 | 0 | 1 | 0 |
| 3 | 0 | 0 | 0 | 1 | 1 |
| 4 | 0 | 0 | 1 | 0 | 0 |
| 5 | 0 | 0 | 1 | 0 | 1 |
| 6 | 0 | 0 | 1 | 1 | 0 |
| 7 | 0 | 0 | 1 | 1 | 1 |
| 8 | 0 | 1 | 0 | 0 | 0 |
| 9 | 0 | 1 | 0 | 0 | 1 |
| 10 | 0 | 1 | 0 | 1 | 0 |
| 11 | 0 | 1 | 0 | 1 | 1 |
| 12 | 0 | 1 | 1 | 0 | 0 |
| 13 | 0 | 1 | 1 | 0 | 1 |
| 14 | 0 | 1 | 1 | 1 | 0 |
| 15 | 0 | 1 | 1 | 1 | 1 |
| 16 | 1 | 0 | 0 | 0 | 0 |
| 17 | 1 | 0 | 0 | 0 | 1 |
| 18 | 1 | 0 | 0 | 1 | 0 |
| 19 | 1 | 0 | 0 | 1 | 1 |
| 20 | 1 | 0 | 1 | 0 | 0 |
| 21 | 1 | 0 | 1 | 0 | 1 |
| 22 | 1 | 0 | 1 | 1 | 0 |
| 23 | 1 | 0 | 1 | 1 | 1 |
| 24 | 1 | 1 | 0 | 0 | 0 |
| 25 | 1 | 1 | 0 | 0 | 1 |
| 26 | 1 | 1 | 0 | 1 | 0 |
| 27 | 1 | 1 | 0 | 1 | 1 |
| 28 | 1 | 1 | 1 | 0 | 0 |
| 29 | 1 | 1 | 1 | 0 | 1 |
| 30 | 1 | 1 | 1 | 1 | 0 |
| 31 | 1 | 1 | 1 | 1 | 1 |

Note pin 1 affects complementing fuse only.

## Fuse Programming and Verification

The array and output polarity fuse programming waveform diagram is shown in Figure 2. The 8 output pins $0_{N}$ are used only to change the polarity of the selected device output and for removing the "security" fuse. Tables 4 and 5 define the voltage and timing requirements.

## Programming Procedure

1. Power is applied to the device. VCC, VCC1, and VCC2 (pins 24, 6, and 19) go to VCC. (The voltage applied to pin 24 cannot precede the voltage applied to pin 6) The output pins ( $4,5,7,8,17,18,20$, and 21 ), are open circuited, or held at a logic low level, while programming the array.
2. After TO, VCC1 (pin 6) can be raised from 5.0 to 10.75 V at a slew rate not to exceed $10 \mathrm{~V} / \mu \mathrm{S}$, or not less than $1 \mathrm{~V} / \mu \mathrm{s}$.
3. The 11 address inputs (pins 1-3, 9-11, 13-15, 22, and 23) will define the location of the array fuse to be opened or the applicable output pin will define the polarity fuse to be opened.
4. After VCC1 has been stable at 10.75 V for period T1 and the address has been stable defining the applicable fuse location for period T2, VCC2 (pin 19) may slew from 5.0 to 10.75 V at a slew rate of 1 to $10 \mathrm{~V} / \mu \mathrm{S}$.
5. VCC2 must remain stable at 10.75 V for the duration of the programming pulse (TP) before returning to 5.0 V .
6. With VCC1 at 10.75 V and after VCC2 has been stable at 5.0V for the period T3, VER pin (16) may be sampled. If the fuse was properly opened, a logic low level will be observed. If the fuse did not open, steps 4 through 6 may be repeated up to 15 times.
7. If additional locations are to be addressed, steps 3 through 6 must be repeated for each fuse to be opened while observing the maximum power up time and duty cycle.

## Fuse Verification

Fuse verification may be performed independent of programming. As seen in Figure 2, with VCC1 at VCCP and VCC2 at VCC verification may occur within the defined timing constraints. (See Table V)

TABLE IV. DC Requirements

| Symbol | Description | Min | Nom | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: |
| VCC | Pin 24 Voltage While Programming or Verifying (Pin 19 Verifying) (Note 1) | 4.75 | 5.00 | 5.25 | V |
| Icc | Pin 24 Current While Programming (Note 2) |  | 200 | 300 | mA |
| $\mathrm{V}_{\mathrm{CCp}}$ | $V_{C C 1} / V_{C C 2}$ (Pins 6 and 19) Voltage While Programming (Note 3) | 10.50 | 10.75 | 11.00 | V |
| ICC1 | $\mathrm{V}_{\text {CC1 }}$ (Pin 6) Current While Programming (Note 2) |  | 300 | 450 | mA |
| ICC2 | VCC2 (Pin 19) Current While Programming (Note 2) |  | 10 | 25 | mA |
| VIL | Input LOW Level - If Left Open, Pins 4, 5, 7, 8, 17, 18, 20, and 21 are Held Low by Internal 50K Resistor | 0 |  | 0.8 | V |
| ILL | $\begin{aligned} & \text { Input LOW Current - Pins; } \\ & 1-3,9-11,13-15,22 \text {, and } 23 \\ & V_{C C} / V_{C C 1} / V_{C C 2}=M \mathrm{Max}, \mathrm{~V}_{\mathrm{IN}}=0.4 \mathrm{~V} \end{aligned}$ |  | -1.0 | -1.5 | mA |
|  | $\begin{aligned} & 4,5,7,8,17,18,20 \text {, and } 21 \text { (Note 4) } \\ & V_{C C} / V_{C C 1} / V_{C C 2}=M a x, V_{I N}=0.8 \mathrm{~V} \end{aligned}$ |  | -0.25 | -1.5 | mA |
| $\mathrm{V}_{\mathrm{IH}}$ | Input HIGH Level | 2.20 |  | $\mathrm{V}_{\mathrm{CC}}$ | V |
| $\mathrm{I}_{\mathrm{H}}$ | Input HIGH Current $V_{C C} / V_{C C 1} / V_{C C 2}=M a x, V_{I N}=V_{C C}$ Max Pins 1-3, 9-11, 13-15, 22, and 23 |  | 90 | 300 | $\mu \mathrm{A}$ |
|  | $4,5,7,8,17,18,20$, and 21 |  | 3 | 5 | mA |
| VOL | Output (Pin 16) LOW Level $\mathrm{V}_{\mathrm{CC}} / \mathrm{V}_{\mathrm{CC} 1} / \mathrm{V}_{\mathrm{CC} 2}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=4 \mathrm{~mA}$ |  |  | 0.8 | V |
| V OH | Output (Pin 16) HIGH Level <br> $\mathrm{V}_{\mathrm{CC}} / \mathrm{V}_{\mathrm{CC} 1} / \mathrm{V}_{\mathrm{CC} 2}=\mathrm{Max}, \mathrm{I}_{\mathrm{OH}}=-0.6 \mathrm{~mA}$ | 2.20 |  |  | V |

Note 1: While programming/verifying, power can be applied to the device for 5 mS maximum with a duty cycle of $20 \%$ maximum.
Note 2: Current measurements are taken with $V_{C C} / V_{C C 1} / V_{C C 2}$ at maximum and with all device inputs and outputs open.
Note 3: The difference between $\mathrm{V}_{\mathrm{CC}}$ and $\mathrm{v}_{\mathrm{CC}}$ must not exceed 6 V .
Note 4: If $\mathrm{V}_{\mathrm{IN}}\left(\mathrm{V}_{1} \mathrm{~J}\right.$ ) less than 0.8 volts at pins $4,5,7,8,17,18,20$, or 21 , means must be provided to limit the current sourced by the device pins to 10 mA .
Note 5: All programming and verification to be performed at $25^{\circ} \mathrm{C} \pm 5^{\circ} \mathrm{C}$
TABLE V. Timing

| Symbol | Description | Min | Nom | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: |
| T0 | Power-Up Before Raising $\mathrm{V}_{\mathrm{CC} 1}$ (Note 1) | 0 | 500 |  | ns |
| T1 | $\mathrm{V}_{\mathrm{CC} 1}$ at $\mathrm{V}_{\mathrm{CCp}}$ Before Raising $\mathrm{V}_{\mathrm{CC} 2}$ | 400 | 500 |  | ns |
| T2 | Address Set-Up Time to $\mathrm{V}_{\text {CC2 }}>\mathrm{V}_{\text {CCP }}$ | 400 | 500 |  | ns |
| T3 | VER Valid After $\mathrm{V}_{\mathrm{CC} 2}$ at $\mathrm{V}_{\mathrm{CC}}$ (Note 2) |  | 200 | 500 | ns |
| T4 | $\mathrm{V}_{\mathrm{CC} 2}$ at $\mathrm{V}_{\mathrm{CC}}$ Before Lowering $\mathrm{V}_{\mathrm{CC} 1}$ | 400 | 500 |  | ns |
| T5 | VER Valid After Raising V $\mathrm{CC1}$ ( (Note 2) |  | 200 | 500 | ns |
| T5b | Address Set-Up Time to VER Valid (Note 2) |  | 200 | 500 | ns |
| T6 | VER Valid Hold Time From Address |  |  | 0 | ns |
| T7 | $\mathrm{V}_{\mathrm{CC} 2}$ at $\mathrm{V}_{\mathrm{CC}}$ Before Address Change | 400 | 500 |  | ns |
| T8 | VER Valid Hold Time From $\mathrm{V}_{\text {CC2 }}>\mathrm{V}_{\text {CCP }}$ (Note 2) | 0 | 100 |  | ns |
| T9 | $\mathrm{V}_{\mathrm{CC} 1}$ at $\mathrm{V}_{\mathrm{CC}}$ Before Power Down | 0 |  |  | ns |
| TP | Programming Pulse | 10 | 10 | 30 | $\mu \mathrm{S}$ |

Note 1: Observe the maximum power-up time or 5 ms and duty cycle of $\mathbf{2 0 \%}$ for $V_{\mathrm{CC}} / V_{\mathrm{CC}} / V_{\mathrm{CC}}$ during programming.
Note 2: VER is valid when $V_{C C 2}=V_{C C}$ and $V_{C C 1}=V_{C C P}$.

## Security Fuse Programming

The security fuse is opened using the same procedure as used for changing the output polarity, except all 8 outputs (pins $4,5,7$, $8,17,18,20$, and 21) must be selected with the application of $V_{I H}$. Verification is determined by the inability to further verify the array.


TL/L/6161-8
FIGURE 3. Security Fuse Programming Diagram

