National Semiconductor

PRELIMINARY

NS32CG821 microCMOS Programmable 1M Dynamic RAM Controller/Driver

General Description

The NS32CG821 dynamic RAM controller provides a low cost, single chip interface between dynamic RAM and the NS32CG16. The NS32CG821 generates all the required access control signal timing for DRAMs. An on-chip refresh request clock is used to automatically refresh the DRAM array. Refreshes and accesses are arbitrated on chip. If necessary, a $\overline{WAIT}$ output inserts wait states into memory access cycles, including burst mode accesses. $\overline{RAS}$ low time during refreshes and $\overline{RAS}$ precharge time after refreshes and back to back accesses are guaranteed through the insertion of wait states. Separate on-chip precharge counters for each $\overline{RAS}$ output can be used for memory interleaving to avoid delayed back to back accesses because of precharge.

Features

- Allows zero wait state operation
- On chip high precision delay line to guarantee critical DRAM access timing parameters
- microCMOS process for low power
- High capacitance drivers for $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and DRAM address on chip
- On chip support for page and static column DRAMs
- Byte enable signals on chip allow byte writing with no external logic
- Selection of controller speeds: 20 MHz and 25 MHz
- On board access refresh arbitration logic
- Direct interface to the NS32CG16 microprocessor
- 4 $\overline{RAS}$ and 4 $\overline{CAS}$ drivers (the $\overline{RAS}$ and $\overline{CAS}$ configuration is programmable)

Control	# of Pins (PLCC)	# of Address Outputs	Largest DRAM Possible	Direct Drive Memory Capacity
NS32CG821	68	10	1 Mbit	8 Mbytes

Block Diagram

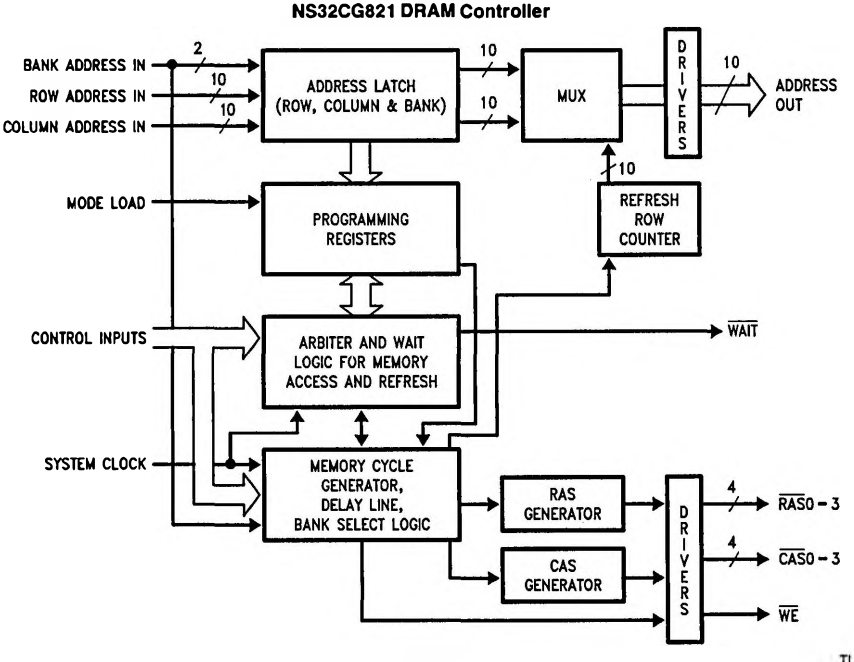

FIGURE 1