HIGH SPEED FSK MODEM TRANSMITTER — NE5080

DESCRIPTION

The NE5080 is the transmitter chip, of a two chip set, designed to be the heart of an FSK modem. (The NE5081 is the receiver chip.) The chips are compatible with the IEEE 802.4 standard for a "Single Channel Phase-Continuous-FSK Bus." The specifications shown in this data sheet are those guaranteed when the transmitter is tuned for the frequencies given in the 802 standard. However, both the NE5080 and the NE5081 may be used at other frequencies. The ratio of logic high to logic low frequencies remains fixed at 1.67 to 1.00 at any center frequency.

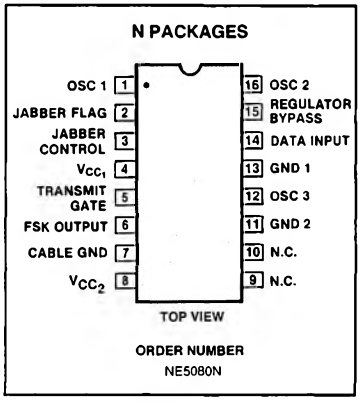
FEATURES

- **Meets IEEE 802.4 standard**
- **Data rates to several Megabaud**
- **Half or full duplex operation**
- **Jabber function on chip**

APPLICATIONS

- **Local Area Networks**
- **Point-to-point communications**
- **Factory automation**
- **Process control**
- **Office automation**

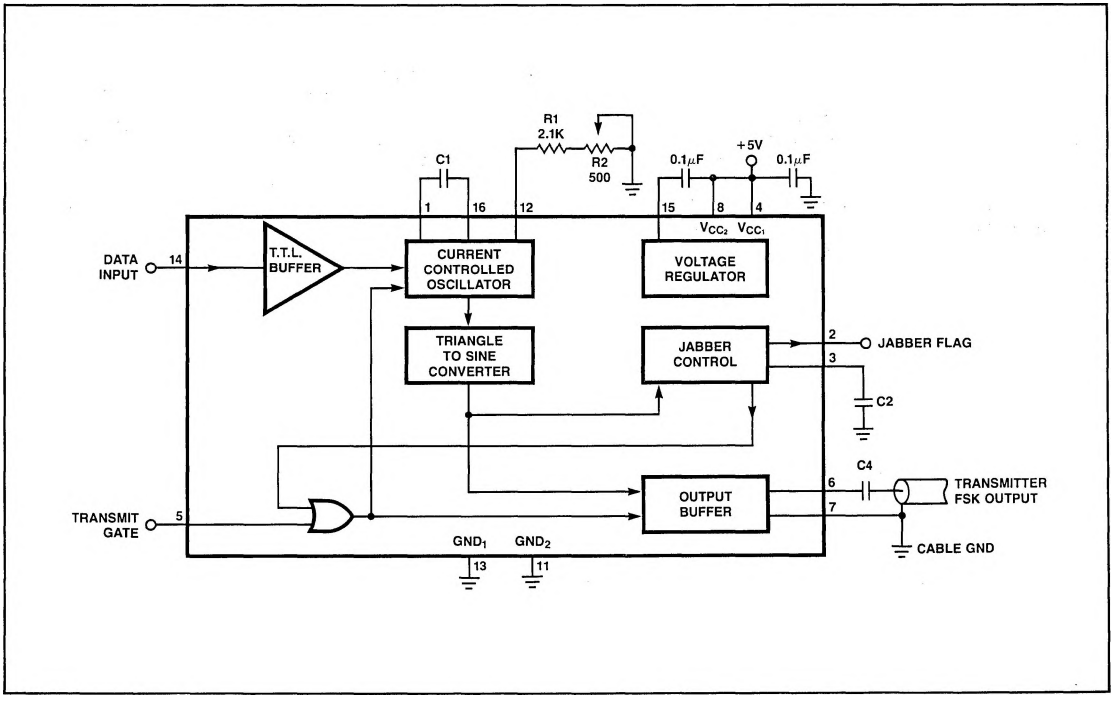
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

SYMBOL & PARAMETER	RATING	UNIT
Supply Voltage V_{CC_1} V_{CC_2}	+ 6	V
Input Voltage Range (Data, Gate)	− 0.3 to + V_{CC}	V
Power Dissipation	800	mW
Operating Temperature Range	0 to + 70	°C
Max Junction Temperature	+ 150	°C
Storage Temperature Range	− 65 to + 150	°C
Lead Temperature (soldering, 10 sec)	300	°C

BLOCK DIAGRAM



HIGH SPEED FSK MODEM TRANSMITTER NE5080

GENERAL DESCRIPTION

The NE5080 is designed to transmit high frequency asynchronous data on coaxial cable, at rates from DC to 2 Megabaud (see note 1). The chip accepts serial data and transmits it as a periodic signal whose frequency depends on whether the data is high or low.

The device is meant to operate at a frequency of 6.25MHz for a logic high and 3.75MHz for a logic low (see note 2). The frequency is set up by external trimming components; however, the ratio of the high and low frequencies is set internally and cannot be altered.

The FSK output can be turned off by use of the transmit gate pin. When turned off, the transmitter has a high output impedance and the oscillator is disabled.

The length of time a transmitter can transmit can be controlled by the use of the Jabber control pin (see description of Jabber Control Pin).

Jabber Control Pin

During the time the transmitter is transmitting, this pin sources a current. This current can be used to set the maximum time that the transmitter can be on. There are three options that can be used:

1. Use the current to charge a capacitor. When the voltage across the cap gets to approx. 1.4V the transmitter will turn off. A logic low applied to pin 3 will reset the Jabber function; an open collector output should be used for this purpose. A logic high applied to the pin will disable the transmitter.
2. Use to externally sense the current and have external circuitry to control the length of time the transmitter is on.
3. The pin can be tied to ground and is then not active. Transmission is then controlled solely by the signal at the transmit gate pin.

Jabber Flag Pin

This pin will go to a logic high when the Jabber Control pin is used to shut off the transmitter. It will latch and can be reset by applying a logic low to the Jabber Control pin.

NE5080 PIN FUNCTION

PIN	FUNCTION
1	**OSC 1**—one end of an external capacitor used to set the carrier frequency
2	**JABBER FLAG**—this pin goes to a logic high if the transmitter attempts to transmit for a longer time than allowed by the Jabber control function
3	**JABBER CONTROL**—used to control transmit time. See note on Jabber function
4	V_{CC_1}—voltage supply
5	**TRANSMIT GATE**—a logic low on this pin will enable the transmitter; a logic high will disable it
6	**TRANSMITTER FSK OUTPUT**
7	**CABLE GROUND**—the shield of the coax cable should be connected to this pin and to Pin 11
8	V_{CC_2}—Connect to pin 4 close to device
9	**No Connection**
10	**No Connection**
11	**GROUND 2**—connect to Analog ground close to device
12	**OSC 3**—a variable resistor between this point and ground is used to set the carrier frequencies.
13	**GROUND 1**—connect to Analog ground close to device
14	**DATA INPUT**
15	**REGULATOR BYPASS**—a bypass capacitor between this pin and V_{CC_1} is required for the internal voltage regulator function
16	**OSC 2**—one end of a capacitor that is between pin 1 and pin 16 and is used to set the carrier frequency

Notes:

1. The NE5080 is capable of transmitting up to 1 Megabaud of differential Manchester code at a center frequency of 5MHz.
2. Although the chip is designed to meet the requirements of IEEE standard 802.4 (Token-Passing Single Channel Phase-Continuous-FSK Bus), it can be used at other frequencies. See "Determining Component Values."

HIGH SPEED FSK MODEM TRANSMITTER — NE5080

ELECTRICAL CHARACTERISTICS $V_{CC_{1,2}}$ = 4.75-5.25V T_A = 0°C to +70°C

PARAMETER	SYMBOL	TEST CONDITIONS	NE5080 Min.	NE5080 Typ.	NE5080 Max.	UNIT
Output Frequency (Logic High)	F_1	Data Input ≥2.0V (See Note 1)	6.17	6.25	6.33	MHz
Output Frequency (Logic Low)	F_0	Data Input ≤0.8V (See Note 1)	3.67	3.75	3.83	MHz
Output Amplitude	V_0	Data Input ≥2.0V or ≤0.8V Output Load = 37.5Ω	0.5		1.0	V_{RMS}
Output Impedance (gated off)	R_{off}	Transmit gate ≥2.0V	100			KΩ
Output Impedance (gated on)	R_{on}	Transmit gate ≤0.8V			37.5	Ω
Output Capacitance	C_0	Transmit gate ≥2.0V or ≤0.8V			10	pF
Feed through	V_F	Transmit gate ≥2.0V 2.0MHz sq. wave (TTL Levels) Input			1	mV_{RMS}
Jabber Current	I_J	Transmit gate ≤0.8V Input ≥2.0V or ≤0.8V		1.25		μA
Supply Current	I_{CC}	V_{CC_1} connected to V_{CC_2}		75	100	mA
LOGIC LEVELS						
Data Input						
Logic High	V_{IH}	Input high voltage	2.0			Volts
Logic Low	V_{IL}	Input low voltage			0.8	Volts
Input Current	I_{IH}	Vin = 2.4V			40	μA
Input Current	I_{IL}	Vin = 0.4V			−1.6	mA
Transmit Gate						
Logic High	V_{IH}	Input high voltage	2.0			Volts
Logic Low	V_{IL}	Input low voltage			0.8	Volts
Input Current	I_{IH}	VG = 2.4V			40	μA
Input Current	I_{IL}	VG = 0.4V			−1.6	mA
Jabber Flag						
Logic High	V_{OH}	IOH = −400μA	2.4			Volts
Logic Low	V_{OL}	IOL = 4.0mA			0.4	Volts
Jabber Control						
Logic High	V_{IH}	Input high voltage	2.0			Volts
Logic Low	V_{IL}	Input low voltage			0.8	Volts

NOTE
(1) Tuned per instructions in Applications section.

AC ELECTRICAL CHARACTERISTICS

SYMBOL & PARAMETER	TO	FROM	TEST CONDITIONS	NE5080 Min.	NE5080 Typ.	NE5080 Max.	UNIT
Set Up Time — T_S	Data In	Gate On	Figure 1	2	0.1		μS
Delay Time — T_A	Output Freq. Change	Data Transition	Figure 2			150	nS
Delay Time — T_B	Output Disabled	Gate Off	Figure 3		0.4	2	μS
Delay Time — T_C	Output Disabled	Jabber Control	Figure 4			100	nS
Delay Time — T_D	Jabber Flag	Jabber Control	Figure 5			100	nS
Jabber Control Reset Pulse Width (Logic Low)				100			nS

TIMING DIAGRAMS

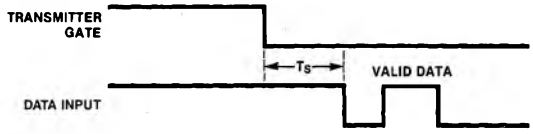


Figure 1. Set-up Time, T_S

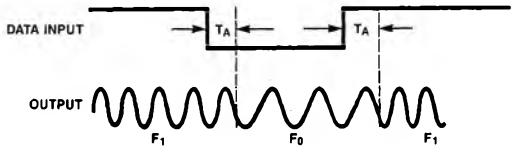


Figure 2. Delay Time, T_A

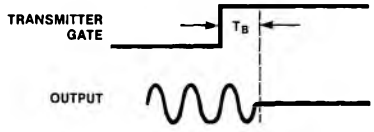


Figure 3. Delay Time, T_B

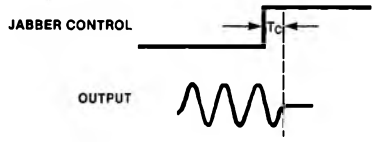


Figure 4. Delay Time, T_C

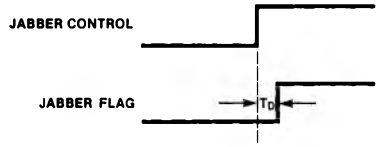


Figure 5. Delay Time, T_D