

Linear Products

DESCRIPTION

The NE5045 is a serial input, parallel output, decoder intended for applications in pulse width or pulse position modulation systems. The serial input pulse, either positive or negative, is shaped and amplified before being fed to the counter/decoder. An integrating type sync. separator detects pulses greater than $t_W = R_S C_S$. The amplified input pulse triggers an internal one-shot (minimum pulse) which in turn clocks the counter-decoder, thereby enhancing system noise rejection. A missing pulse detector resets the decoder during the sync. pause. An internal voltage regulator supplies power for the radio receiver, providing excellent isolation from the power supply as well as the decoder logic.

FEATURES

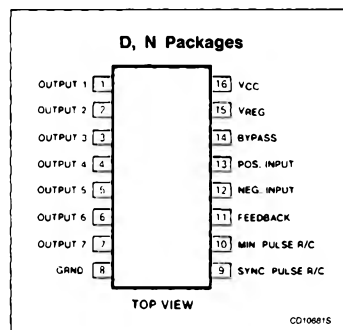
- Decodes up to 7 channels
- High gain input amplifier
- Externally set sync. pause and minimum pulse

- Wide supply voltage range, 3.6V – 8V
- Positive or negative pulse inputs
- Noise and flutter rejection
- Outputs reset to zero without inputs
- Compatible with all transmission mediums

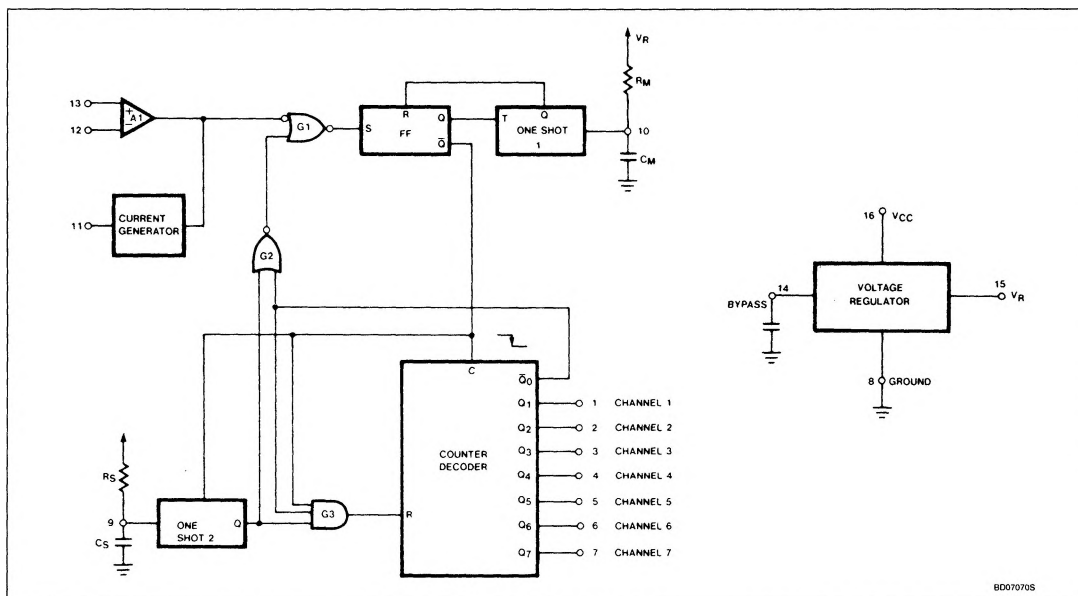
APPLICATIONS

- Radio-controlled aircraft, cars, boats, trains
- Industrial controllers
- Remote-controlled entertainment systems
- Security systems
- Instrumentation recorders/controls
- Remote analog/digital data transmission
- Automotive sensor systems
- Robotics
- Telemetry

PIN CONFIGURATION



BLOCK DIAGRAM



Seven-Channel RC Decoder

NE5045

ORDERING INFORMATION

| DESCRIPTION | TEMPERATURE RANGE | ORDER CODE |
|--------------------|-------------------|------------|
| 16-Pin Plastic SO | 0 to +70°C | NE5045D |
| 16-Pin Plastic DIP | 0 to +70°C | NE5045N |

ABSOLUTE MAXIMUM RATINGS¹

| SYMBOL | PARAMETER | RATING | UNIT |
|------------------|--------------------------|---------------------|------|
| V _{CC} | Supply voltage | 10 | V |
| I _{OUT} | Regulator output current | -25 | mA |
| | Decoded output current | ± 5 | mA |
| | Pause input voltage | 0 to V _R | V |
| V _{IN} | Input amplifier voltage | 0 to V _R | V |
| T _A | Operating temperature | 0 to +70 | °C |
| T _{STG} | Storage temperature | -65 to +150 | °C |

NOTE:

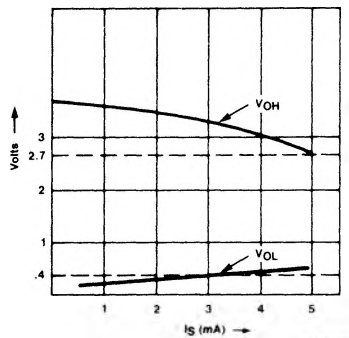
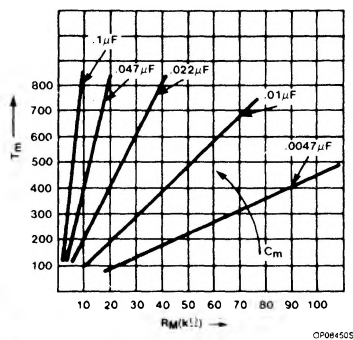
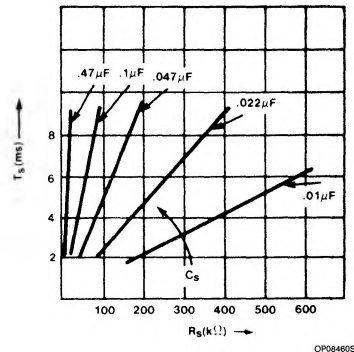
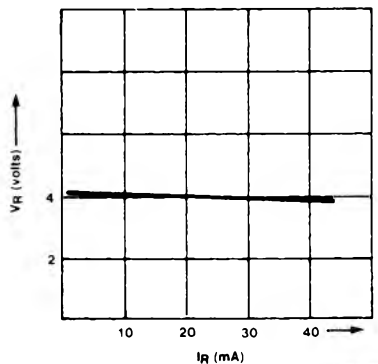
1. T_A = 25°C unless otherwise stated.DC ELECTRICAL CHARACTERISTICS Standard conditions: T_A = 25°C, V_{CC} = 5.0V, unless otherwise stated, using Test Circuit.

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | UNIT |
|---------------------------|----------------------------|--|--------|------|------|------|
| | | | Min | Typ | Max | |
| Power supply requirements | | | | | | |
| V _{CC} | Power supply voltage range | Test circuit | 3.6 | | 8.0 | V |
| I _{CC} | Power supply current | Excluding input bias current | | 9.0 | 14.0 | mA |
| Voltage regulator | | | | | | |
| V _R | Output voltage | | 3.7 | 4.1 | 4.5 | V |
| I _R | Output current | V _R ≥ 3.7V | | | -15 | mA |
| | Line regulation | V _{CC} = 6V to 8V | | 0.01 | 0.05 | V/V |
| | Voltage drop | V _{CC} = 4V, I _R = -10mA | | | 1.3 | V |
| Input amplifier | | | | | | |
| I _{BIAS} | Input bias current | | | 10 | 100 | nA |
| V _{IN} | Input voltage range | | 2.0 | | 4.0 | V |
| | Open-loop gain | | | 60 | | dB |
| | Feedback current | | 100 | 200 | 400 | μA |
| | Detection threshold | Test circuit, ΔV _{I2} & 13 | | 8 | 20 | mV |
| t _S | Sync. pause time | R _S C _S = 6.0ms | 5.1 | 6.0 | 6.9 | ms |
| t _M | Minimum pulse time | R _M C _M = 500μs | 405 | 475 | 545 | μs |
| Outputs — all channels | | | | | | |
| V _{OL} | Output voltage LOW | I _{SINK} = 1mA | | 0.25 | 0.5 | V |
| V _{OH} | Output voltage HIGH | I _{SOURCE} = 2mA | 2.7 | | | V |

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TYPICAL PERFORMANCE CHARACTERISTICS

 V_{OL} vs Sink Current
and V_{OH} vs Source CurrentMinimum Pulse Time,
 t_M vs R_M , C_M Sync Pause Time,
 t_S vs $R_S C_S$ Regulator Voltage
vs Load Current

Seven-Channel RC Decoder

NE5045

TEST CIRCUIT

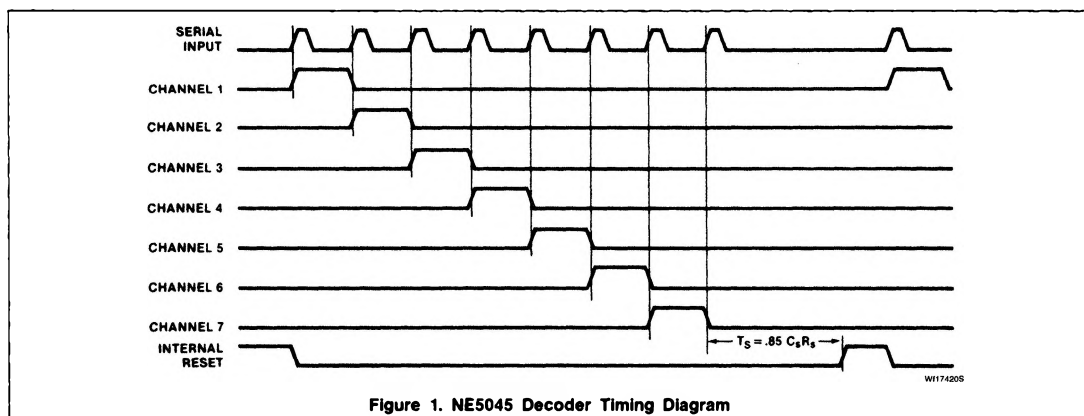
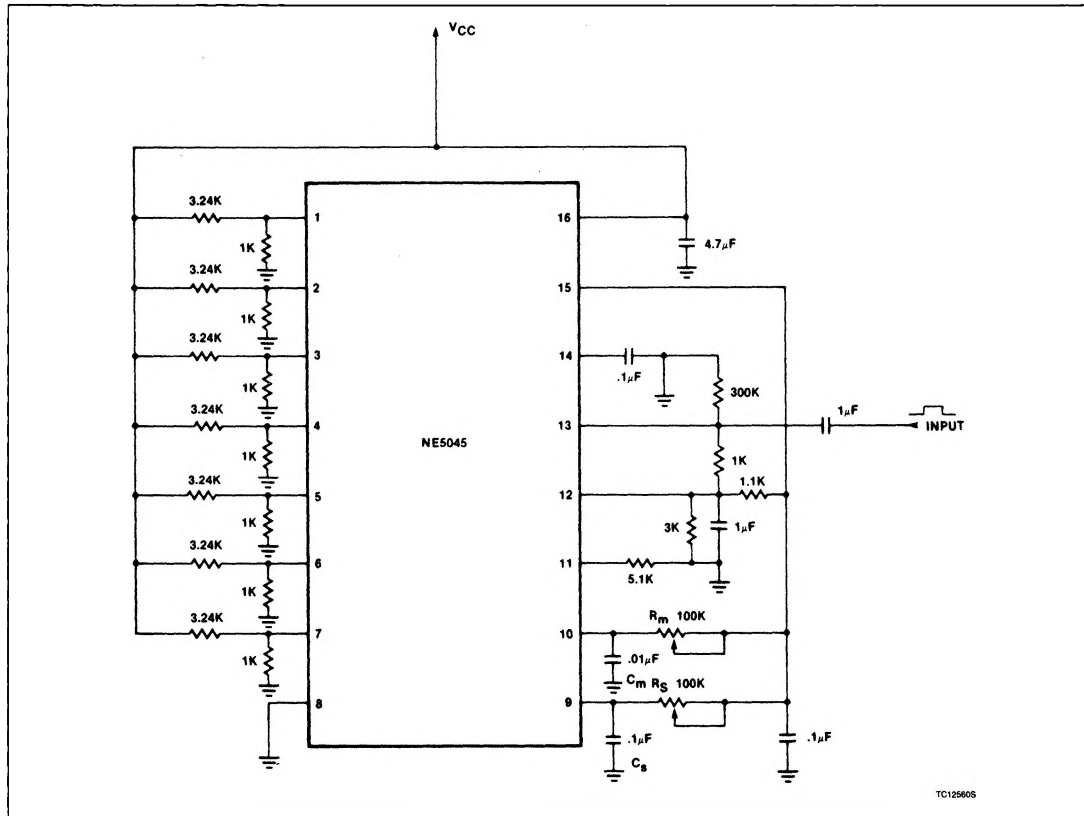


Figure 1. NE5045 Decoder Timing Diagram

Seven-Channel RC Decoder

NE5045

CIRCUIT OPERATION

The NE5045 is a serial input, parallel output decoder containing all the active circuitry necessary to separate up to 7 channels of information in a pulse width modulated system. An internal voltage regulator provides excellent power supply rejection for the decoder as well as a regulated output for a radio receiver, if used.

The high gain input amplifier, A1 ($A_v > 60\text{dB}$), allows either positive or negative pulses to be used and has input bias currents less than 10nA . Signals as low as $10\text{mV}_{\text{p-p}}$ can easily be demodulated. The feedback current generator can be used to provide positive feedback, thereby creating hysteresis in the input switching levels. Hysteresis prevents false triggering due to noise or IF amplifier distortion. If positive input pulses are used, the signal would be connected to the non-inverting input, Pin 13. In this case, the input threshold would be set by the voltage difference between Pin 12 and Pin 13, established externally with a resistive divider network. Design of the divider will be covered later. Negative input signals would be coupled to Pin 12, the inverting input.

The amplified signal from A1 is gated by G1 and in turn sets the flip-flop. Assume, for the time, that G2 is low. The combination of the flip-flop and One-Shot 1 produces a minimum pulse to clock the counter-decoder for each positive edge at Pin 13 which exceeds the voltage on Pin 12. The width of this pulse is: $t_M = R_M C_M$. With this arrangement, the system will not respond to any pulse after the first edge and before the end of t_M . In effect the input is turned off for a period equal to t_M following the leading edge of each input pulse. The noise immunity of the decoder is thus enhanced by the ratio of t_M to the period between input pulses. Obviously t_M must be less than the shortest period between input pulses.

The counter is clocked and One-Shot 2 is reset (capacitor C_S is discharged) each time the flip-flop is set. When the flip-flop is reset, C_S begins to charge up through R_S . The time constant $t_S = 0.85 R_S C_S$ is normally much larger than the time between input pulses so that the output of One-Shot 2 remains low until the last pulse of a given frame is received. Figure 1 shows the timing diagram for the decoder. After the last pulse in a frame (system synchronized) Q_O will go low and G2 will go high. The input is now disabled by G1 until One-Shot 2 times out, at which time G2 will go low.

This connection serves two purposes:

(1) establishes synchronization in no more than one frame and

(2) prevents the counter-decoder from overflowing due to extra noise pulses in a given frame. Thus, any noise pulses in a frame will only affect those channels after that pulse and only in that frame.

If fewer than 7 channels of input are used then Q_O is high after the last pulse and the counter-decoder is reset when One-Shot 2 goes high.

Each channel has a totem-pole output stage capable of sourcing 2mA and sinking 1mA .

The voltage regulator operates in two modes, depending on the power supply voltage. If V_{CC} is greater than 5V , the voltage regulator acts as a series pass regulator with a nominal output voltage of 4.1V . When V_{CC} is less than 5V , the regulator acts as a dynamic decoupler where the bypass capacitor on Pin 14 filters out line transients. The internal pass transistor acts like an emitter-follower whose base is decoupled by the bypass capacitor. The value of capacitance will depend upon the degree of smoothing required and the amplitude of the line transients. If the regulator provides power for the radio receiver, this capacitor may have to be as large as $33\mu\text{F}$. However, if this is not done, $1\mu\text{F}$ should be sufficient.

DECODER DESIGN EQUATIONS

The design of the decoder's external circuitry is quite simple. The minimum pulse One-Shot (#1) and the synchronization One-Shot (#2) each have time periods given by:

$$t_M = R_M C_M \quad \text{and}$$

$$t_S = 0.85 R_S C_S$$

respectively. The constraints on these time periods are $t_M < \text{the minimum input pulse width or time between leading edges of the input}$ and $t_S > \text{maximum input pulse width but } t_S < \text{the sync pause (time between last pulse}$

in frame and first pulse of the following frame).

The design of the input amplifier biasing network depends upon a number of factors, including:

1. Pulse polarity
2. Pulse amplitude
3. Variations in amplitude and noise
4. Detection threshold and hysteresis levels

For a very simple case, assume the input is a positive pulse train and the threshold of detection is desired to be 400mV without hysteresis. Figure 2 shows the input amplifier along with the associated biasing circuits. The resistors R_1 and R_2 set the voltage on Pin 12, which should be between 2V to 5V .

$$V_{12} = V_R \frac{1}{1 + R_1/R_2}$$

The threshold is set by the voltage drop across R_3 , that is, the decoder will not be triggered until the voltage on Pin 13 exceeds the voltage on Pin 12.

$$V_{\text{THRESHOLD}} = V_{12} - V_{13}$$

$$V_{\text{THRESHOLD}} = V_{12} \left(\frac{1}{1 + R_4/R_3} \right)$$

If we assume $V_R = 4.1\text{V}$ and let $V_{12} = 3\text{V}$ then

$$R_1 = 1.1\text{k}$$

$$R_2 = 3.0\text{k}$$

The threshold is then set to 400mV by setting

$$R_4/R_3 = 6.5$$

R_4 should be sufficiently large so as to not load the input signal. If we let $R_3 = 51\text{k}$ then $R_4 = 330\text{k}$. Figure 3 shows the external connections for a complete decoder. Note that this circuit does not have provisions for noise filtering or rejection of amplitude variations.

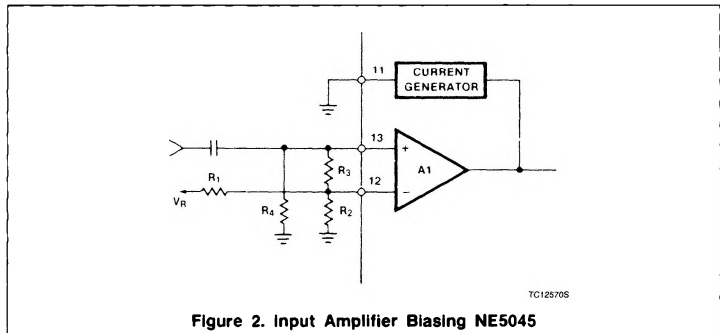


Figure 2. Input Amplifier Biasing NE5045

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