NCV8406, NCV8406A

Self-Protected Low Side Driver with Temperature and Current Limit

65 V, 7.0 A, Single N−Channel

NCV8406/A is a three terminal protected Low-Side Smart Discrete device. The protection features include overcurrent, overtemperature, ESD and integrated Drain-to-Gate clamping for overvoltage protection. This device offers protection and is suitable for harsh automotive environments.

Features

- Short Circuit Protection
- Thermal Shutdown with Automatic Restart
- Over Voltage Protection
- Integrated Clamp for Inductive Switching
- ESD Protection
- dV/dt Robustness
- Analog Drive Capability (Logic Level Input)
- These Devices are Faster than the Rest of the NCV Devices
- AEC−Q101 Qualified and PPAP Capable
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements
- These Devices are Pb−Free and are RoHS Compliant

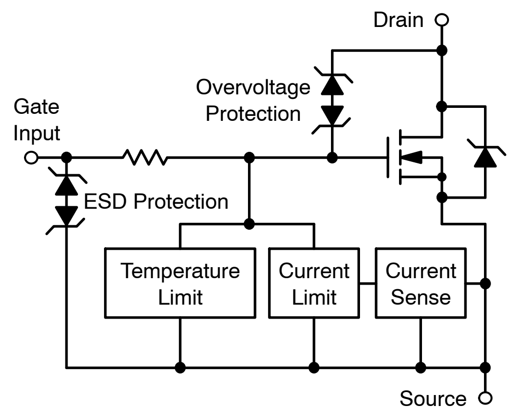
Typical Applications

- Switch a Variety of Resistive, Inductive and Capacitive Loads
- Can Replace Electromechanical Relays and Discrete Circuits
- Automotive / Industrial

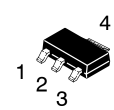
ON Semiconductor®

http://onsemi.com

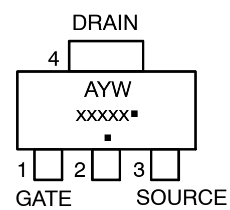
V_{DSS} (Clamped)	$R_{DS(on)}$ TYP	I_D TYP (Limited)
65 V	210 mΩ	7.0 A

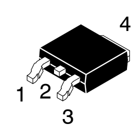


MARKING DIAGRAM

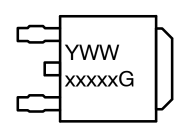


SOT−223
CASE 318E
STYLE 3





DPAK
CASE 369C



A = Assembly Location
Y = Year
W, WW = Work Week
xxxxx = V8406 or 8406A
G or ▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain−to−Source Voltage Internally Clamped	V_{DSS}	70	Vdc
Gate−to−Source Voltage	V_{GS}	± 14	Vdc
Drain Current Continuous	I_D	Internally Limited	
Total Power Dissipation − SOT−223 Version @ T_A = 25°C (Note 1) @ T_A = 25°C (Note 2)	P_D	 1.25 1.81	W
Total Power Dissipation − DPAK Version @ T_A = 25°C (Note 1) @ T_A = 25°C (Note 2)	P_D	 1.31 2.31	W
Thermal Resistance − SOT−223 Version Junction−to−Case Junction−to−Ambient (Note 1) Junction−to−Ambient (Note 2)	 $R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	 7.0 100 69	°C/W
Thermal Resistance − DPAK Version Junction−to−Case Junction−to−Ambient (Note 1) Junction−to−Ambient (Note 2)	 $R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	 1.0 95 54	°C/W
Single Pulse Inductive Load Switching Energy (Starting T_J = 25°C, V_{DD} = 50 Vdc, V_{GS} = 5.0 Vdc, I_L = 2.1 Apk, L = 50 mH, R_G = 25 Ω)	E_{AS}	110	mJ
Load Dump Voltage (V_{GS} = 0 and 10 V, R_I = 2 Ω, R_L = 7 Ω, t_d = 400 ms)	V_{LD}	75	V
Operating Junction Temperature Range	T_J	−40 to 150	°C
Storage Temperature Range	T_{stg}	−55 to 150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface mounted onto minimum pad size (100 sq/mm) FR4 PCB, 1 oz cu.
2. Mounted onto 1″ square pad size (700 sq/mm) FR4 PCB, 1 oz cu.

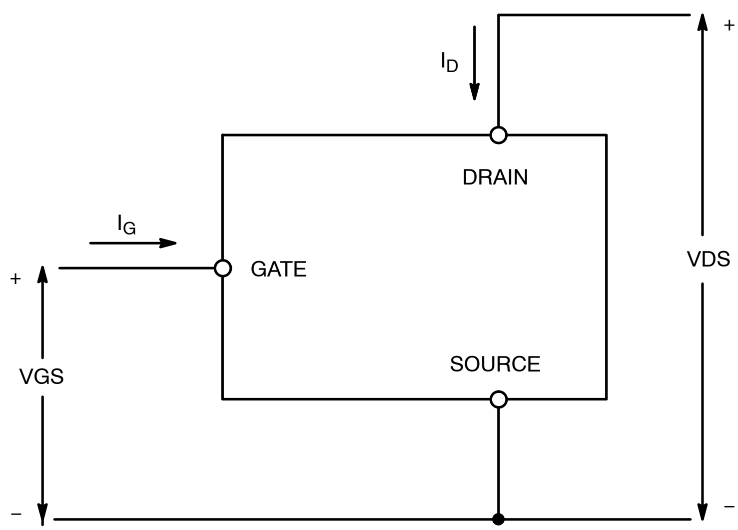


Figure 1. Voltage and Current Convention

MOSFET ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Clamped Breakdown Voltage (V_{GS} = 0 V, I_D = 2 mA)		$V_{(BR)DSS}$	60	65	70	V
Zero Gate Voltage Drain Current (V_{DS} = 52 V, V_{GS} = 0 V)		I_{DSS}	–	22	100	µA
Gate Input Current (V_{GS} = 5.0 V, V_{DS} = 0 V)		I_{GSS}	–	30	100	µA
ON CHARACTERISTICS						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 150 µA) Threshold Temperature Coefficient		$V_{GS(th)}$	1.2 –	1.66 4.0	2.0 –	V −mV/°C
Static Drain−to−Source On−Resistance (Note 3) (V_{GS} = 10 V, I_D = 2.0 A, T_J @ 25°C)		$R_{DS(on)}$	–	185	210	mΩ
Static Drain−to−Source On−Resistance (Note 3) (V_{GS} = 5.0 V, I_D = 2.0 A, T_J @ 25°C) (V_{GS} = 5.0 V, I_D = 2.0 A, T_J @ 150°C)		$R_{DS(on)}$	– –	210 445	240 520	mΩ
Source−Drain Forward On Voltage (I_S = 7.0 A, V_{GS} = 0 V)		V_{SD}	–	0.9	1.1	V
SWITCHING CHARACTERISTICS (Note 6)						
Turn−on Delay Time	R_L = 6.6 Ω, V_{in} = 0 to 10 V, V_{DD} = 13.8 V, I_D = 2.0 A, 10% V_{in} to 10% I_D	$td_{(on)}$	–	127	–	ns
Turn−on Rise Time	R_L = 6.6 Ω, V_{in} = 0 to 10 V, V_{DD} = 13.8 V, I_D = 2.0 A, 10% I_D to 90% I_D	t_{rise}	–	486	–	ns
Turn−off Delay Time	R_L = 6.6 Ω, V_{in} = 0 to 10 V, V_{DD} = 13.8 V, I_D = 2.0 A, 90% V_{in} to 90% I_D	$td_{(off)}$	–	1600	–	ns
Turn−off Fall Time	R_L = 6.6 Ω, V_{in} = 0 to 10 V, V_{DD} = 13.8 V, I_D = 2.0 A, 90% I_D to 10% I_D	t_{fall}	–	692	–	ns
Slew Rate ON	R_L = 6.6 Ω, V_{in} = 0 to 10 V, V_{DD} = 13.8 V, I_D = 2.0 A, 70% to 50% V_{DD}	dV_{DS}/dT_{on}	–	79	–	V/µs
Slew Rate OFF	R_L = 6.6 Ω, V_{in} = 0 to 10 V, V_{DD} = 13.8 V, I_D = 2.0 A, 50% to 70% V_{DD}	dV_{DS}/dT_{off}	–	27	–	V/µs
SELF PROTECTION CHARACTERISTICS (Note 4)						
Current Limit	V_{DS} = 10 V, V_{GS} = 5.0 V, T_J = 25°C (Note 5) V_{DS} = 10 V, V_{GS} = 5.0 V, T_J = 150°C (Notes 5, 6) V_{DS} = 10 V, V_{GS} = 10 V, T_J = 25°C (Notes 5)	I_{LIM}	5.0 3.5 6.5	7.0 4.5 8.5	9.5 6.0 10.5	A
Temperature Limit (Turn−off)	V_{GS} = 5.0 V (Note 6)	$T_{LIM(off)}$	150	180	200	°C
Thermal Hysteresis	V_{GS} = 5.0 V	$\Delta T_{LIM(on)}$	–	10	–	°C
Temperature Limit (Turn−off)	V_{GS} = 10 V (Note 6)	$T_{LIM(off)}$	150	180	200	°C
Thermal Hysteresis	V_{GS} = 10 V	$\Delta T_{LIM(on)}$	–	20	–	°C
Input Current during Thermal Fault	V_{DS} = 0 V, V_{GS} = 5.0 V, T_J = T_J > $T_{(fault)}$ (Note 6) V_{DS} = 0 V, V_{GS} = 10 V, T_J = T_J > $T_{(fault)}$ (Note 6)	$I_{g(fault)}$	– –	5.9 12.3	–	mA
ESD ELECTRICAL CHARACTERISTICS						
Electro−Static Discharge Capability Human Body Model (HBM) Machine Model (MM)		ESD	 6000 500	 – –	 – –	V

3. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.
4. Fault conditions are viewed as beyond the normal operating range of the part.
5. Current limit measured at 380 µs after gate pulse.
6. Not subject to production test.

TYPICAL PERFORMANCE CURVES

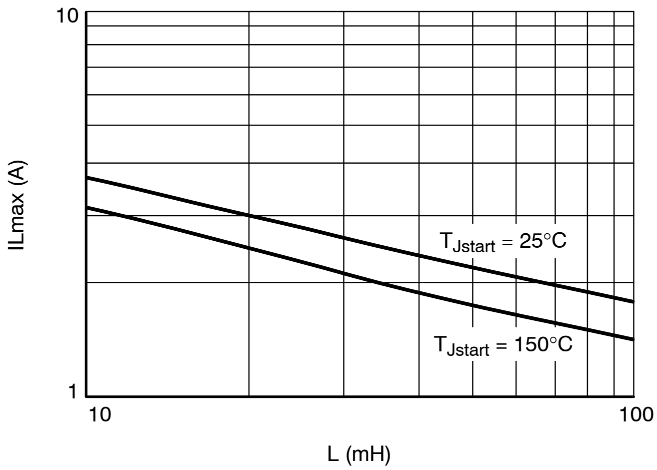


Figure 2. Single Pulse Maximum Switch−off Current vs. Load Inductance

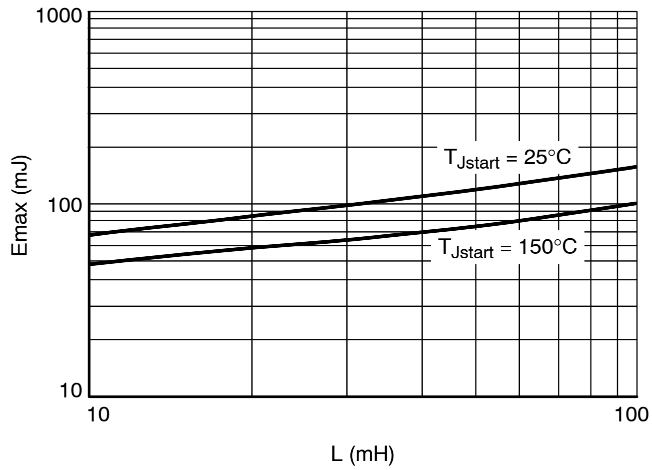


Figure 3. Single−Pulse Maximum Switching Energy vs. Load Inductance

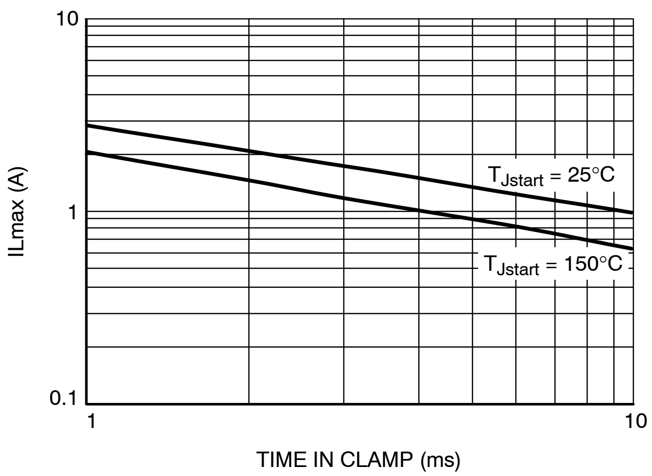


Figure 4. Single Pulse Maximum Inductive Switch−off Current vs. Time in Clamp

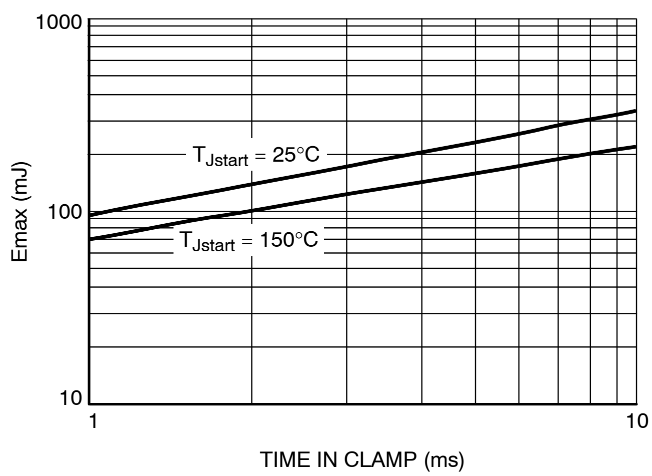


Figure 5. Single−Pulse Maximum Inductive Switching Energy vs. Time in Clamp

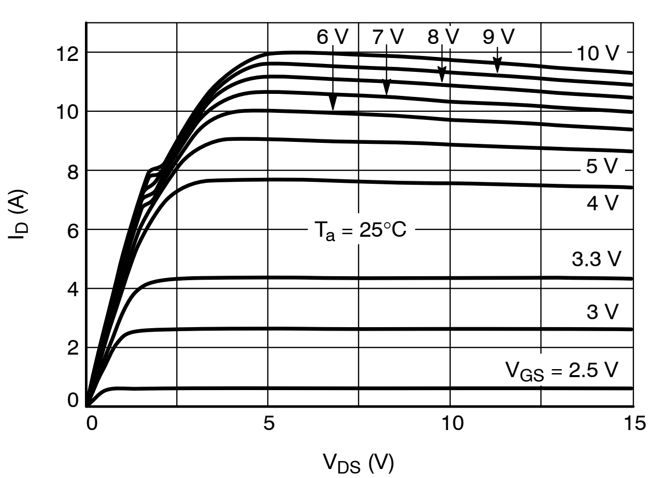


Figure 6. On−state Output Characteristics

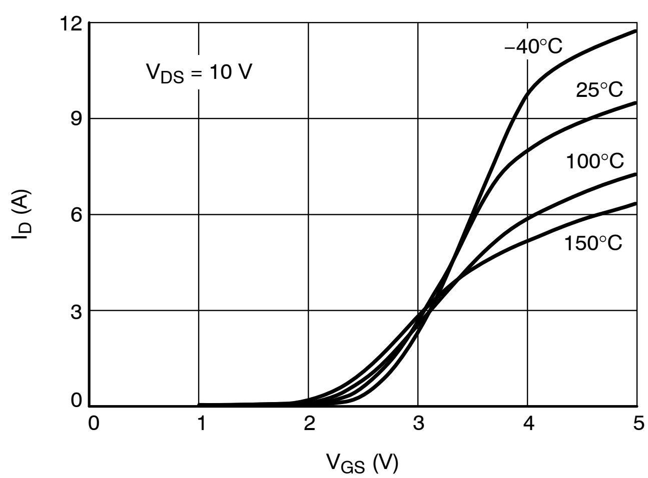


Figure 7. Transfer Characteristics

TYPICAL PERFORMANCE CURVES

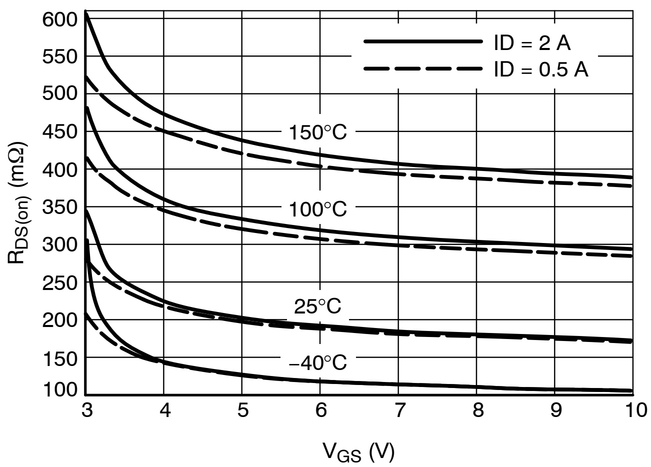


Figure 8. $R_{DS(on)}$ vs. Gate−Source Voltage

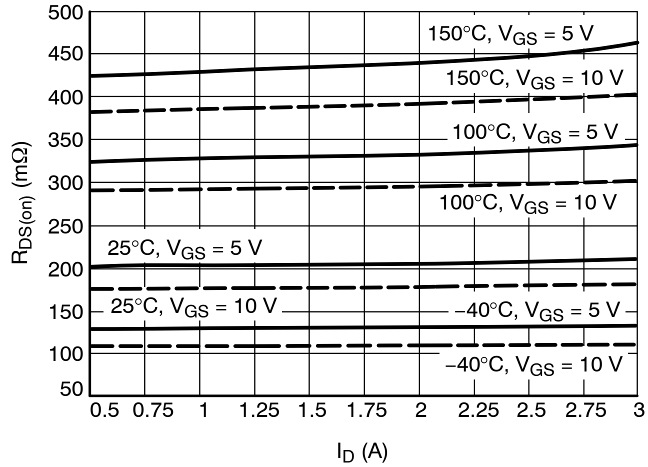


Figure 9. $R_{DS(on)}$ vs. Drain Current

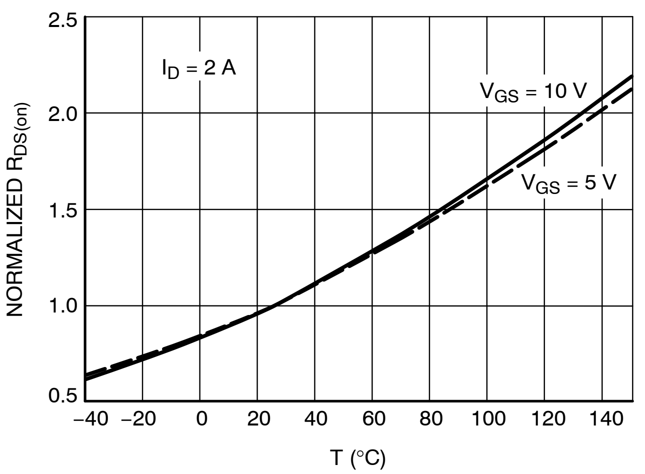


Figure 10. Normalized $R_{DS(on)}$ vs. Temperature

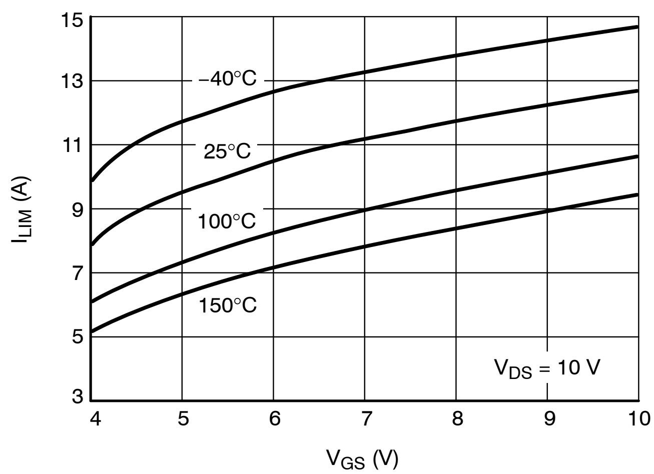


Figure 11. Current Limit vs. Gate−Source Voltage

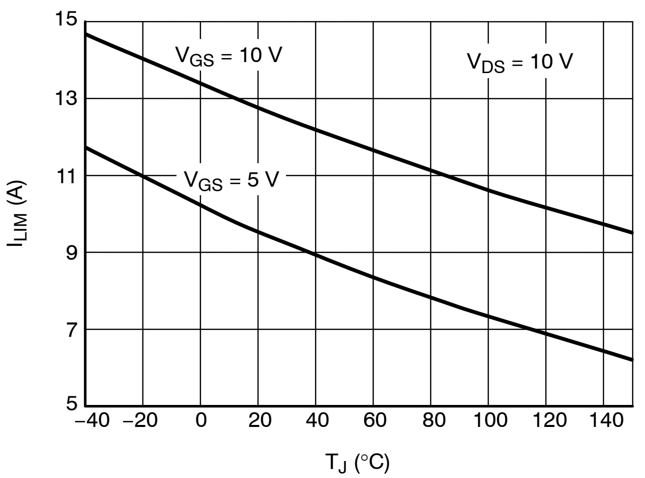


Figure 12. Current Limit vs. Junction Temperature

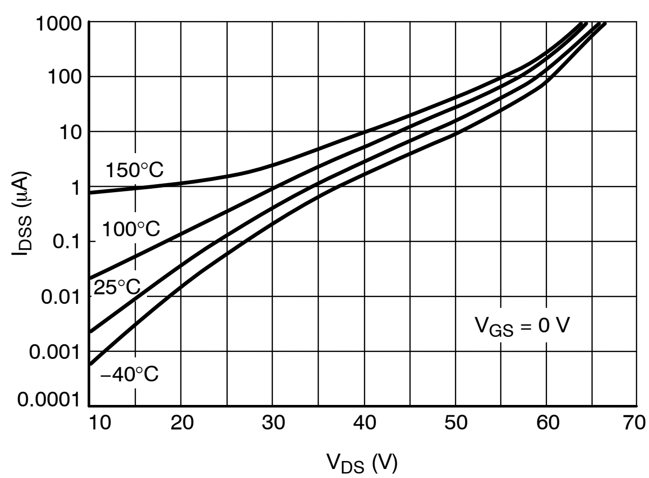


Figure 13. Drain−to−Source Leakage Current

TYPICAL PERFORMANCE CURVES

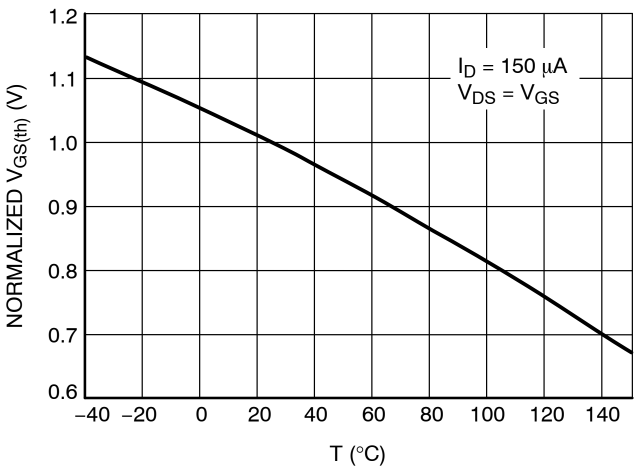


Figure 14. Normalized Threshold Voltage vs. Temperature

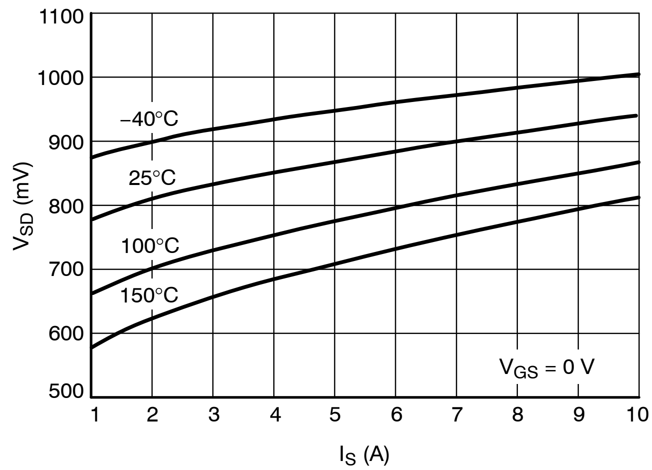


Figure 15. Source−Drain Diode Forward Characteristics

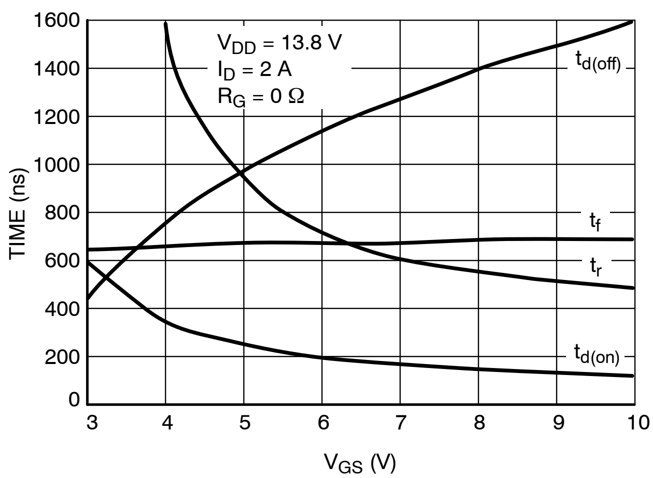


Figure 16. Resistive Load Switching Time vs. Gate−Source Voltage

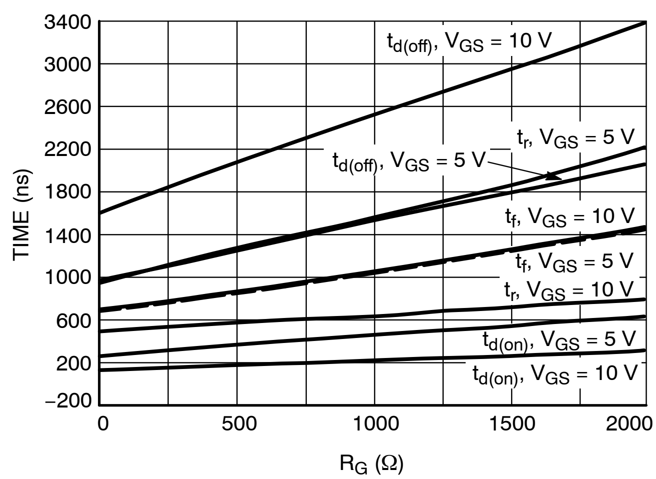


Figure 17. Resistive Load Switching Time vs. Gate Resistance

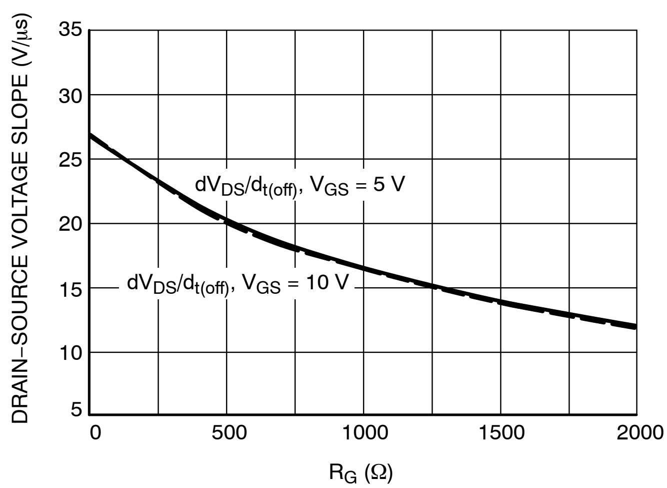


Figure 18. Drain−Source Voltage Slope during Turn On and Turn Off vs. Gate Resistance

TYPICAL PERFORMANCE CURVES

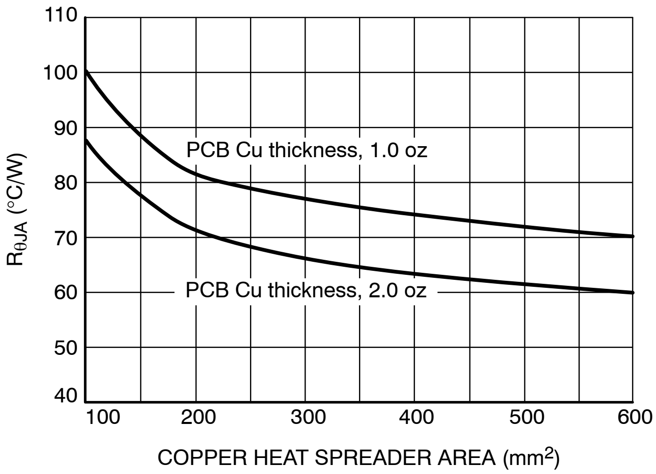


Figure 19. $R_{\theta JA}$ vs. Copper Area − SOT−223

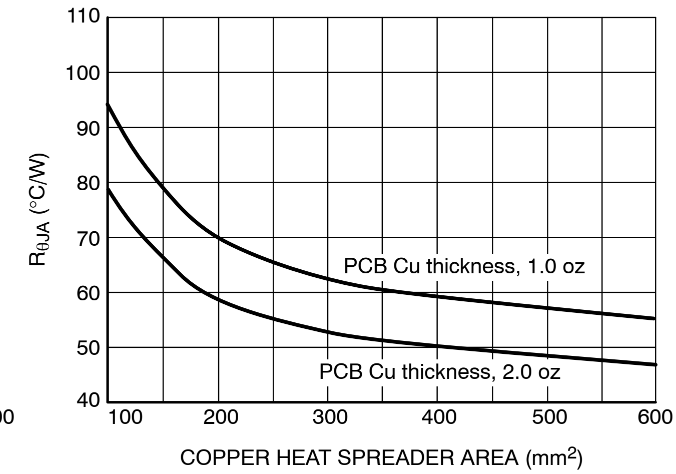


Figure 20. $R_{\theta JA}$ vs. Copper Area − DPAK

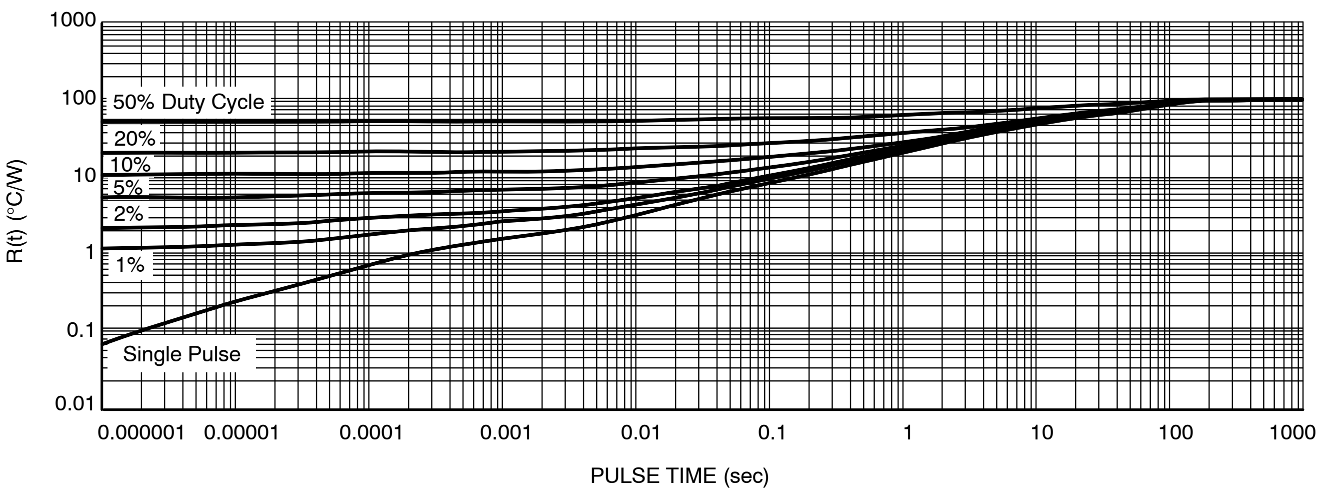


Figure 21. Transient Thermal Resistance − SOT−223 Version

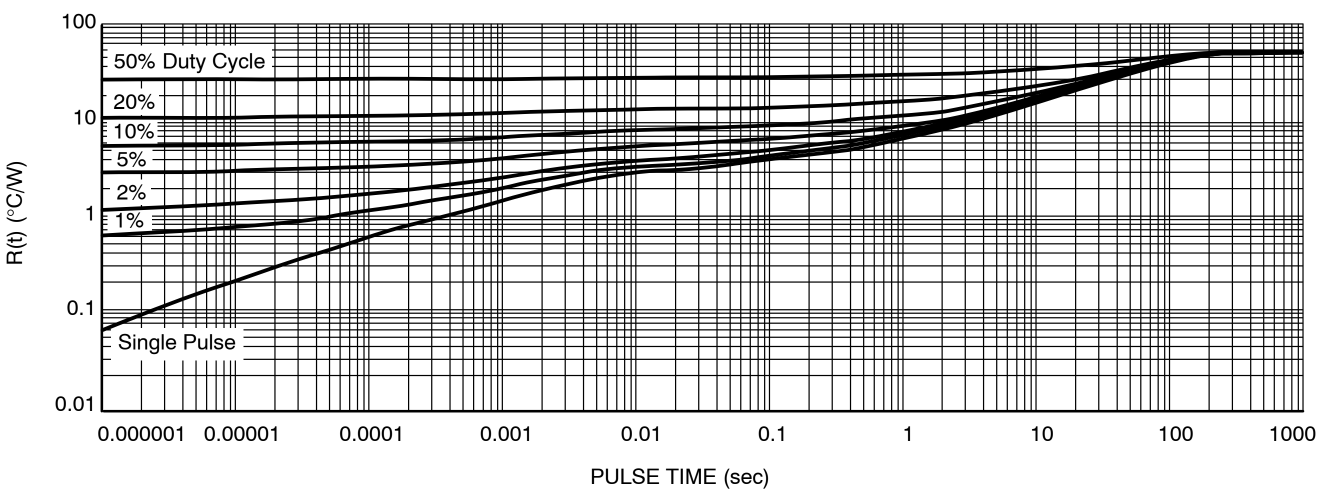


Figure 22. Transient Thermal Resistance − DPAK Version

TEST CIRCUITS AND WAVEFORMS

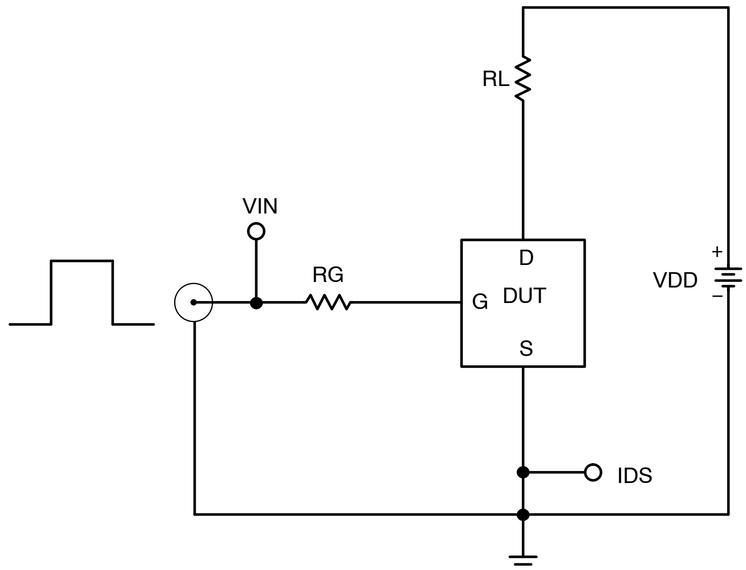


Figure 23. Resistive Load Switching Test Circuit

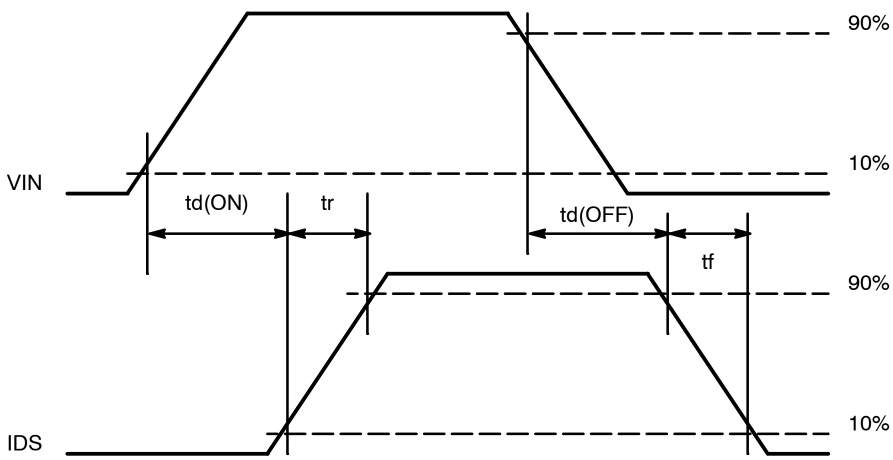


Figure 24. Resistive Load Switching Waveforms

TEST CIRCUITS AND WAVEFORMS

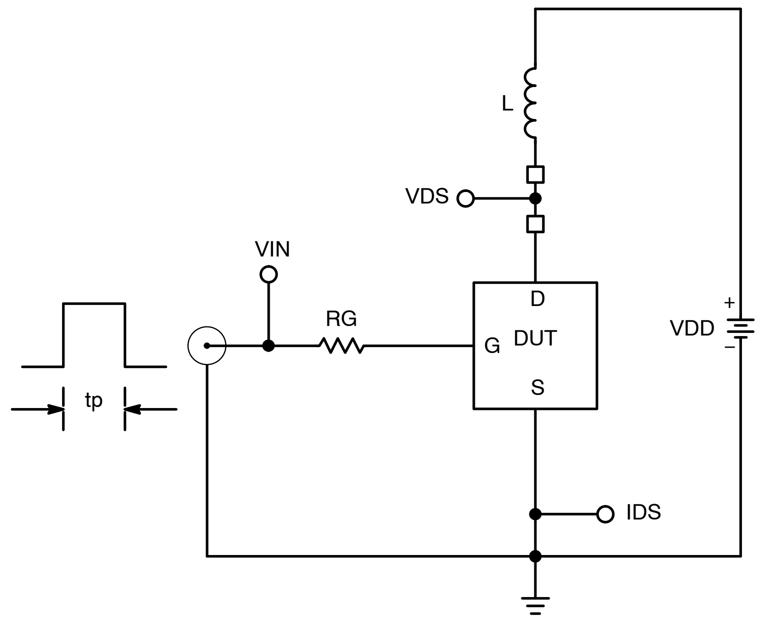


Figure 25. Inductive Load Switching Test Circuit

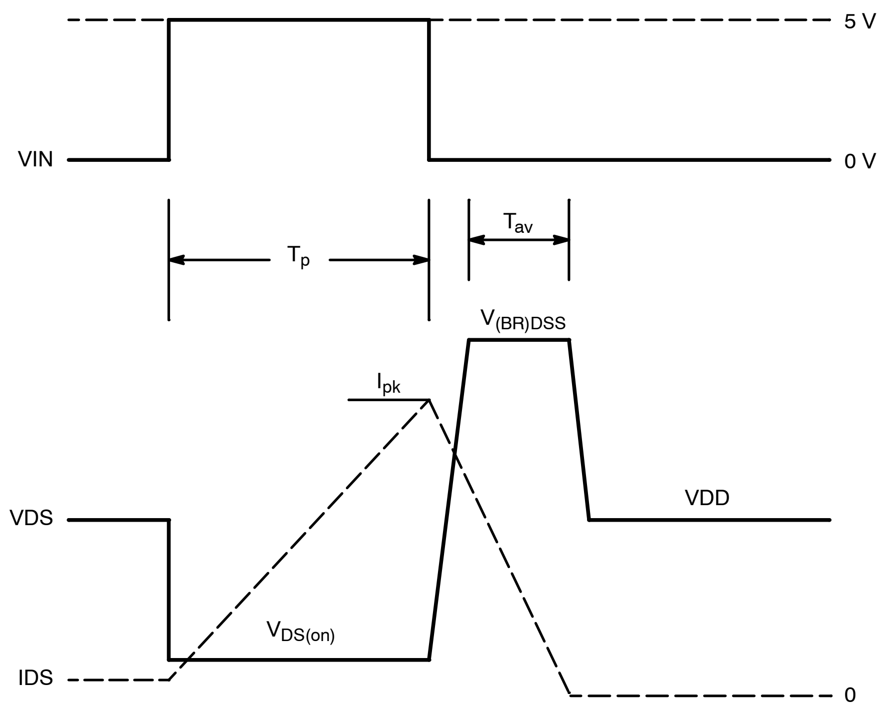


Figure 26. Inductive Load Switching Waveforms

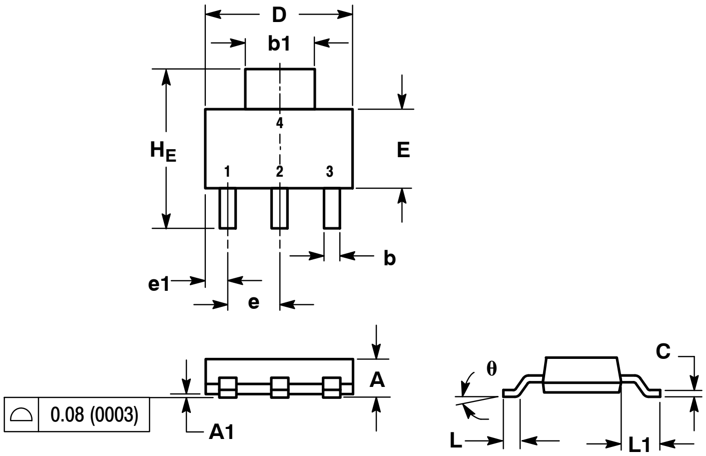
ORDERING INFORMATION

Device	Package	Shipping†
NCV8406STT3G	SOT−223 (Pb−Free)	4000 / Tape & Reel
NCV8406ASTT3G	SOT−223 (Pb−Free)	4000 / Tape & Reel
NCV8406DTRKG	DPAK (Pb−Free)	2500 / Tape & Reel
NCV8406ADTRKG	DPAK (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

SOT−223 (TO−261)
CASE 318E−04
ISSUE N

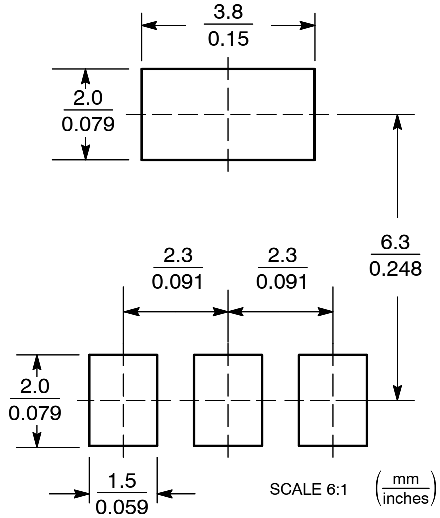


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCH.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	1.50	1.63	1.75	0.060	0.064	0.068
A1	0.02	0.06	0.10	0.001	0.002	0.004
b	0.60	0.75	0.89	0.024	0.030	0.035
b1	2.90	3.06	3.20	0.115	0.121	0.126
c	0.24	0.29	0.35	0.009	0.012	0.014
D	6.30	6.50	6.70	0.249	0.256	0.263
E	3.30	3.50	3.70	0.130	0.138	0.145
e	2.20	2.30	2.40	0.087	0.091	0.094
e1	0.85	0.94	1.05	0.033	0.037	0.041
L	0.20	---	---	0.008	---	---
L1	1.50	1.75	2.00	0.060	0.069	0.078
H_E	6.70	7.00	7.30	0.264	0.276	0.287
θ	0°	–	10°	0°	–	10°

STYLE 3:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

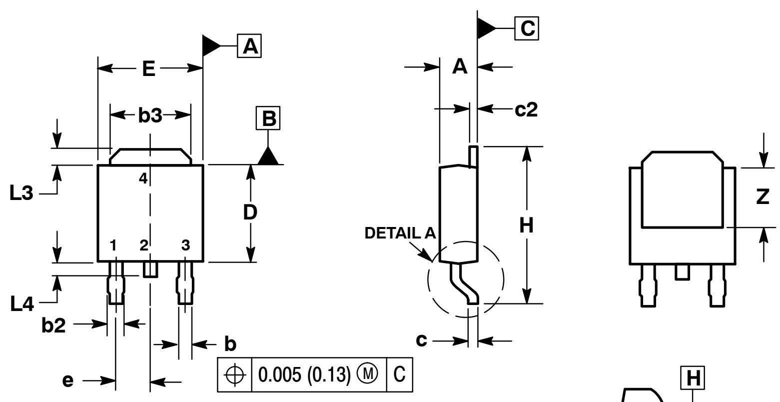
SOLDERING FOOTPRINT*

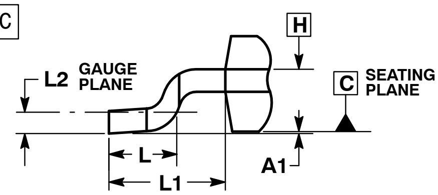


*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

DPAK (SINGLE GAUGE)
CASE 369C−01
ISSUE D





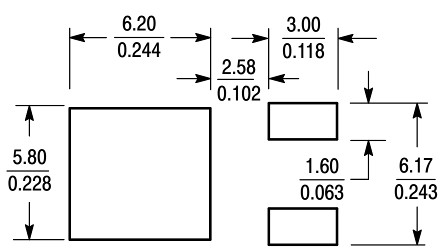
DETAIL A
ROTATED 90° CW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108 REF		2.74 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	−−−	0.040	−−−	1.01
Z	0.155	−−−	3.93	−−−

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

SOLDERING FOOTPRINT*



SCALE 3:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
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