NCP5351

Product Preview

Synchronous Power MOSFET Driver

The NCP5351 is a dual MOSFET gate driver optimized to drive the gates of both high and low side Power MOSFETs in a Synchronous Buck converter. The NCP5351 is an excellent companion to multiphase controllers that do not have integrated gate drivers, such as ON Semiconductor's CS5323, CS5305 or CS5307. This architecture provides a power supply designer great flexibility by being able to locate the gate drivers close to the MOSFETs.

4 Amp drive capability makes the NCP5351 ideal for minimizing switching losses in MOSFETs with large input capacitance. Optimized internal, adaptive non–overlap circuitry further reduces switching losses by preventing simultaneous conduction of both MOSFETs.

The floating top driver design can accommodate MOSFET drain voltages as high as 25 V. Both gate outputs can be driven low, and supply current reduced to less than 10 μA, by applying a low logic level to the Enable (EN) pin. An Undervoltage Lockout function ensures that both driver outputs are low when the supply voltage is low, and a Thermal Shutdown function provides the IC with overtemperature protection.

The NCP5351 is pin–to–pin compatible with the SC1205 and is available in a standard SO–8 package.

Features

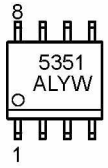
- 4 A Peak Drive Current
- Rise and Fall Times Typically < 15 ns
- Propagation Delay from Inputs to Outputs < 20 ns Maximum
- Adaptive Non–Overlap Time Optimized for Power MOSFETs Switching > 20 A/Phase
- Floating Top Driver Accommodates Applications Up to 25 V
- Undervoltage Lockout to Prevent Switching When the Power Supply Is Unreliable
- Thermal Shutdown Protection Against Overtemperature
- <1 mA Quiescent Current – Enable (EN) Asserted (No Switching)
- <10 μA Quiescent Current – Enable (EN) Deasserted (Disables Switching)

ON Semiconductor™

http://onsemi.com

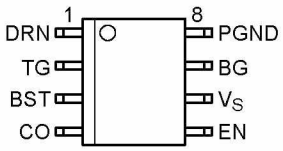
SO–8
D SUFFIX
CASE 751

MARKING DIAGRAM



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping
NCP5351D	SO–8	95 Units/Rail
NCP5351DR2	SO–8	2500 Tape & Reel

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

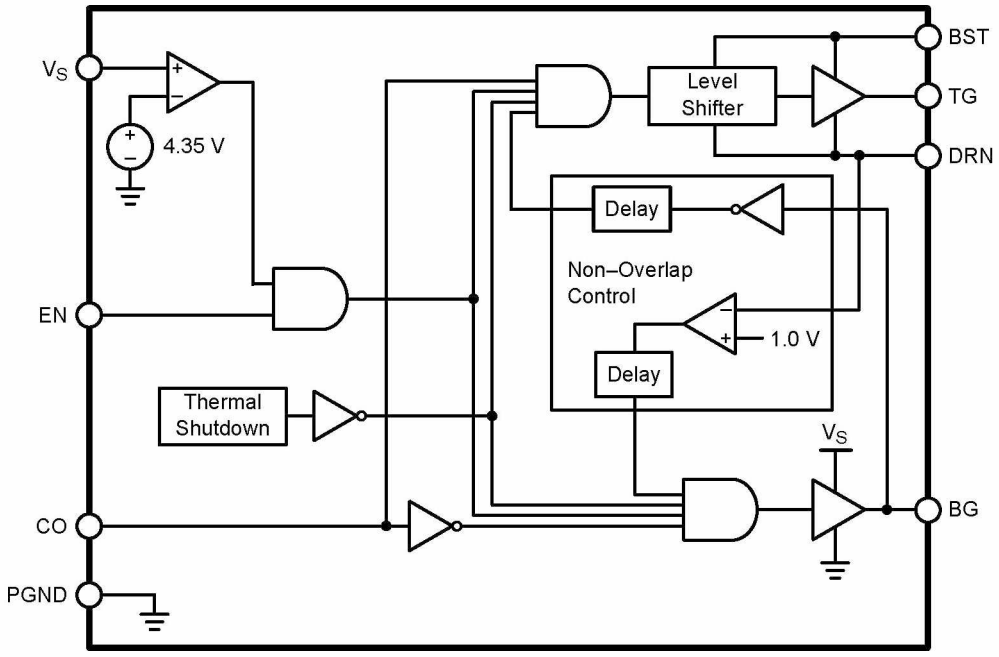


Figure 1. Block Diagram

Table 2. Input–Output Truth Table

EN	CO	DRN	TG	BG
L	X	X	L	L
H	L	< 0.5 V	L	H
H	H	< 0.5 V	H	L
H	L	< 0.5 V	L	H
H	H	< 0.5 V	H	L
H	L	> 1.5 V	L	L
H	H	> 1.5 V	H	L
H	L	> 1.5 V	L	L
H	H	> 1.5 V	H	L

MAXIMUM RATINGS*

Rating	Value	Unit
Operating Junction Temperature, T_J	Internally Limited	°C
Package Thermal Resistance: Junction to Case, $R_{\theta JC}$ Junction to Ambient, $R_{\theta JA}$	 45 165	 °C/W °C/W
Storage Temperature Range, T_S	–65 to 150	°C
ESD Susceptibility (Human Body Model)	2.0	kV
Lead Temperature Soldering: Reflow: (SMD styles only) (Note 3)	230 peak	°C

3. 60 seconds maximum above 183°C.

*The maximum package power dissipation must be observed.

MAXIMUM RATINGS

Pin Symbol	Pin Name	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
V_S	Main Supply Voltage Input	7.0 V	–0.3 V	NA	4.0 A Peak (< 100 μs) 250 mA DC
BST	Bootstrap Supply Voltage Input	30 V wrt/PGND 7.0 V wrt/DRN	–0.3 V wrt/DRN	NA	4.0 A Peak (< 100 μs) 250 mA DC
DRN	Switching Node (Bootstrap Supply Return)	25 V	–1.0 V DC –5.0 V for 100 ns	4.0 A Peak (< 100 μs) 250 mA DC	NA
TG	High Side Driver Output (Top Gate)	30 V wrt/PGND 7.0 V wrt/DRN	–0.3 V wrt/DRN	4.0 A Peak (< 100 μs) 250 mA DC	4.0 A Peak (< 100 μs) 250 mA DC
BG	Low Side Driver Output (Bottom Gate)	7.0 V	–0.3 V	4.0 A Peak (< 100 μs) 250 mA DC	4.0 A Peak (< 100 μs) 250 mA DC
CO	TG & BG Control Input	7.0 V	–0.3 V	1.0 mA	1.0 mA
EN	Enable Input	7.0 V	–0.3 V	1.0 mA	1.0 mA
PGND	Ground	0 V	0 V	4.0 A Peak (< 100 μs) 250 mA DC	NA

NOTE: All voltages are with respect to PGND except where noted.

ELECTRICAL CHARACTERISTICS ($0°C < T_J < 125°C$; $4.5\ V < V_S < 5.5\ V$; $4.0\ V < V_{BST} < 26\ V$; $V_{EN} = V_S$; unless otherwise noted.)

Parameter	Test Conditions	Min	Typ	Max	Unit
DC OPERATING SPECIFICATIONS					
Power Supply					
V_S Quiescent Current, Operating	V_{CO} = 0 V, 4.5 V; No output switching	–	1.0	–	mA
V_{BST} Quiescent Current, Operating	V_{CO} = 0 V, 4.5 V; No output switching	–	50	–	μA
Quiescent Current, Non–Operating	V_{EN} = 0 V; V_{CO} = 0 V, 4.5 V	–	–	10	μA
Undervoltage Lockout					
Start Threshold	CO = 0 V	4.2	4.35	4.5	V
Stop Threshold	CO = 0 V	4.1	4.28	4.45	V
Hysteresis	CO = 0 V	0.05	0.07	0.1	V
CO Input Characteristics					
High Threshold	–	2.0	–	–	V
Low Threshold	–	–	–	0.8	V
Input Bias Current	$0 < V_{CO} < V_S$	–	0	10	μA
EN Input Characteristics					
High Threshold	Both drivers respond to CO	2.0	–	–	V
Low Threshold	Both drivers are low independent of CO	–	–	0.8	V
Input Bias Current	$0 < V_{EN} < V_S$	–	0	10	μA
Thermal Shutdown					
Overtemperature Trip Point	Note 4.	–	170	–	°C
Recovery Temperature	Note 4.	125	–	–	°C
Hysteresis	Note 4.	–	30	–	°C
High Side Driver					
Peak Output Current	Note 4.	–	4.0	–	A
Output Resistance (Sourcing) (Note 4)	Duty Cycle < 2.0%, Pulse Width < 100 μs, $T_J = 125°C$, $V_{BST} - V_{DRN} = 4.5\ V$, $V_{TG} = 4.0\ V + V_{DRN}$	–	0.5	–	Ω
Output Resistance (Sinking) (Note 4)	Duty Cycle < 2.0%, Pulse Width < 100 μs, $T_J = 125°C$, $V_{BST} - V_{DRN} = 4.5\ V$, $V_{TG} = 0.5\ V + V_{DRN}$	–	0.35	–	Ω
Low Side Driver					
Peak Output Current	Note 4.	–	4.0	–	A
Output Resistance (Sourcing) (Note 4)	Duty Cycle < 2.0%, Pulse Width < 100 μs, $T_J = 125°C$, $V_S = 4.5\ V$, $V_{BG} = 4.0\ V$	–	0.6	–	Ω
Output Resistance (Sinking) (Note 4)	Duty Cycle < 2.0%, Pulse Width < 100 μs, $T_J = 125°C$, $V_S = 4.5\ V$, $V_{BG} = 0.5\ V$	–	0.5	–	Ω

4. Guaranteed by design, not 100% tested in production.

ELECTRICAL CHARACTERISTICS ($0°C < T_J < 125°C$; $4.5\ V < V_S < 5.5\ V$; $4.0\ V < V_{BST} < 26\ V$; $V_{EN} = V_S$, $C_{LOAD} = 6.0\ nF$; unless otherwise noted.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
AC OPERATING SPECIFICATIONS						
High Side Driver						
Rise Time	tr_{TG}	$V_{BST} - V_{DRN} = 4.5\ V$, $V_S = 5.0\ V$	–	8.0	16	ns
Fall Time	tf_{TG}	$V_{BST} - V_{DRN} = 4.5\ V$, $V_S = 5.0\ V$	–	14	21	ns
Propagation Delay Time, TG Going High (Non–Overlap Time)	$tpdh_{TG}$	$V_{BST} - V_{DRN} = 4.5\ V$, $V_S = 5.0\ V$	30	55	100	ns
Propagation Delay Time, TG Going Low	$tpdl_{TG}$	$V_{BST} - V_{DRN} = 4.5\ V$, $V_S = 5.0\ V$	–	18	37	ns
Low Side Driver						
Rise Time	tr_{BG}	$V_S = 4.5\ V$	–	10	15	ns
Fall Time	tf_{BG}	$V_S = 4.5\ V$	–	12	20	ns
Propagation Delay Time, BG Going High (Non–Overlap Time)	$tpdh_{BG}$	$V_S = 4.5\ V$	30	55	100	ns
Propagation Delay Time, BG Going Low	$tpdl_{BG}$	$V_S = 4.5\ V$	–	10	18	ns
Undervoltage Lockout						
V_S Rising	$tpdh_{UVLO}$	EN = V_S, CO = 0 V, $dV_S/dt > 1.0\ V/\mu s$, from 4.0 V to 4.5 V, time to BG > 1.0 V	–	10	–	μs
V_S Falling	$tpdl_{UVLO}$	EN = V_S, CO = 0 V, $dV_S/dt < -1.0\ V/\mu s$, from 4.5 V to 4.0 V, time to BG < 1.0 V	–	10	–	μs

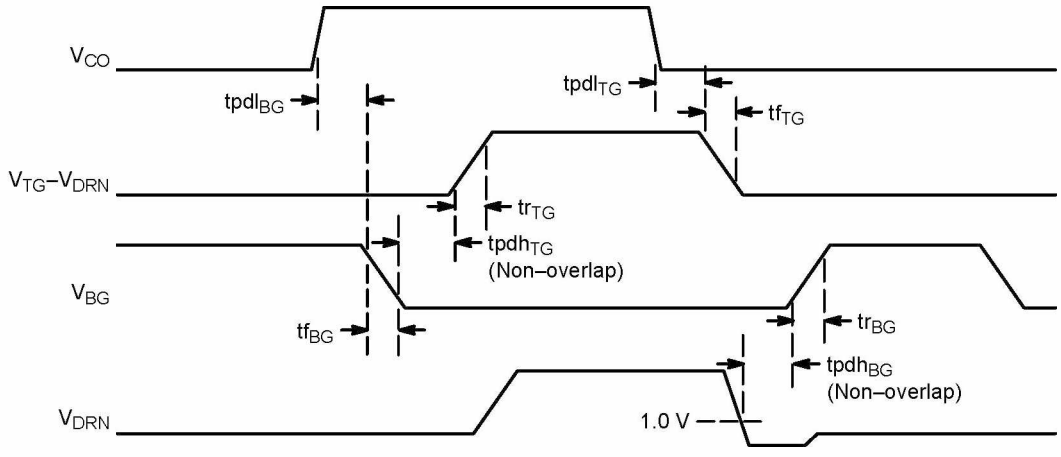


Figure 2. Timing Diagram

PACKAGE PIN DESCRIPTION

Pin Number	Pin Symbol	Description
1	DRN	The switching node common to the high and low–side FETs. The high–side (TG) driver and supply (BST) are referenced to this pin.
2	TG	Driver output to the high–side MOSFET gate.
3	BST	Bootstrap supply voltage input. In conjunction with a Schottky diode to V_S, a 0.1 μF to 1.0 μF ceramic capacitor connected between BST and DRN develops supply voltage for the high–side driver (TG).
4	CO	Logic level control input produces complementary output states – no inversion at TG; inversion at BG.
5	EN	Logic level enable input forces TG and BG low, and supply current to less than 10 μA when EN is low.
6	V_S	Power supply input. A 0.1 μF to 1.0 μF ceramic capacitor should be connected from this pin to PGND.
7	BG	Driver output to the low–side (synchronous rectifier) MOSFET gate.
8	PGND	Ground.

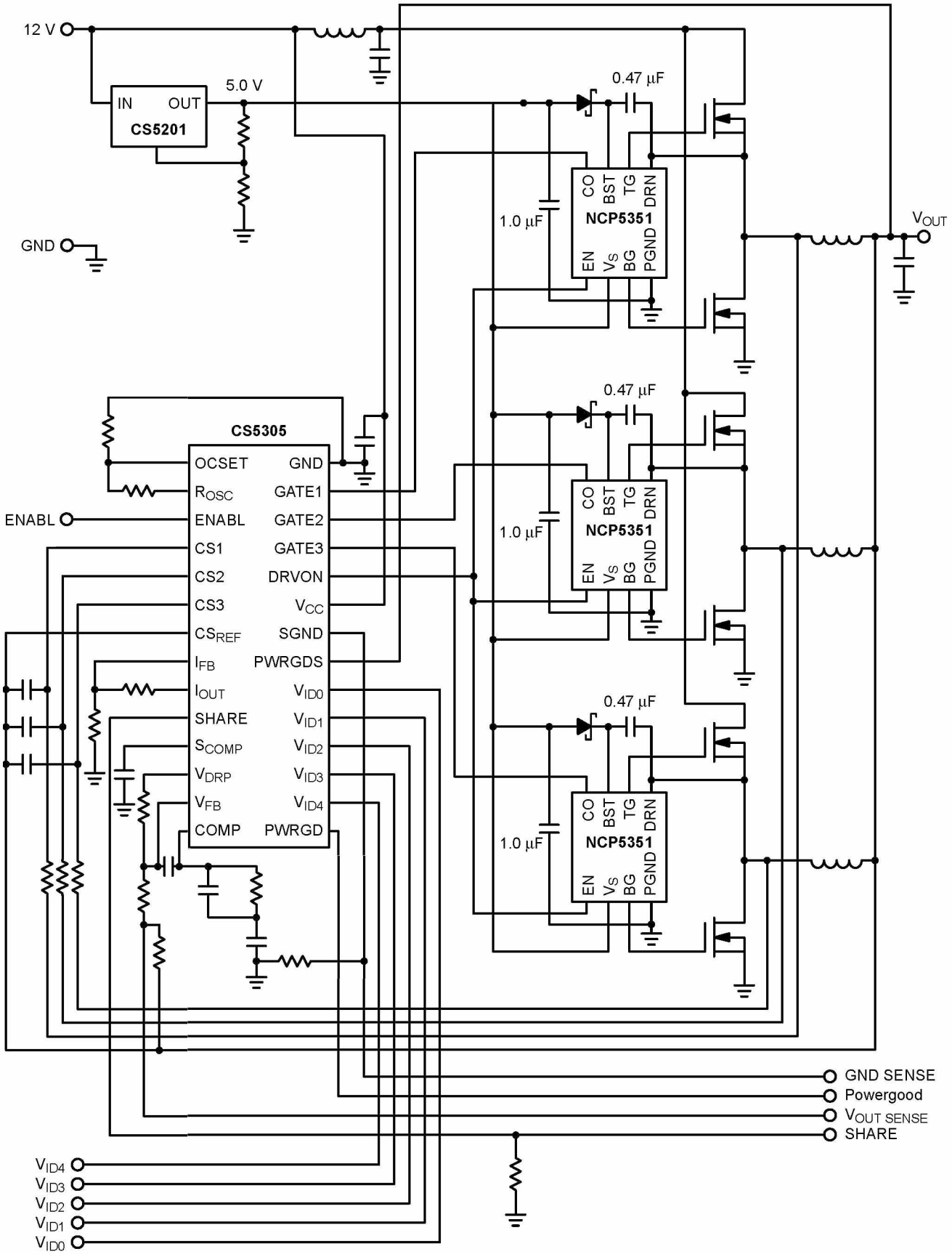


Figure 3. Application Diagram