NCP431A, NCP431B, NCP432B Series

Programmable Precision References

The NCP431/NCP432 integrated circuits are three−terminal programmable shunt regulator diodes. These monolithic IC voltage references operate as a low temperature coefficient zener which is programmable from Vref to 36 V using two external resistors. These devices exhibit a wide operating current range of 40 μA to 100 mA with a typical dynamic impedance of 0.22 Ω. The characteristics of these references make them excellent replacements for zener diodes in many applications such as digital voltmeters, power supplies, and op amp circuitry. The 2.5 V reference makes it convenient to obtain a stable reference from 5.0 V logic supplies, and since the NCP431/NCP432 operates as a shunt regulator, it can be used as either a positive or negative voltage reference. Low minimum operating current makes this device an ideal choice for secondary regulators in SMPS adapters with extremely low no−load consumption.

Features

- Programmable Output Voltage to 36 V
- Low Minimum Operating Current: 40 μA, Typ @ 25°C
- Voltage Reference Tolerance: ±0.5%, Typ @ 25°C (NCP431B/NCP432B)
- Low Dynamic Output Impedance, 0.22 Ω Typical
- Sink Current Capability of 40 μA to 100 mA
- Equivalent Full−Range Temperature Coefficient of 50 ppm/°C Typical
- Temperature Compensated for Operation over Full Rated Operating Temperature Range
- These are Pb−Free Devices

Typical Applications

- Voltage Adapters
- Switching Power Supply
- Precision Voltage Reference
- Charger
- Instrumentation

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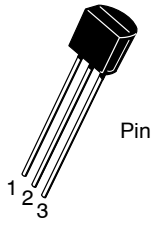
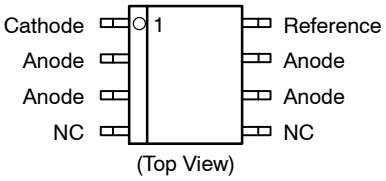
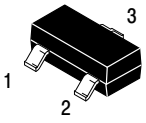


TO−92
LP SUFFIX
CASE 29−11

Pin 1. Reference
2. Anode
3. Cathode

SOIC−8 NB
D SUFFIX
CASE 751





SOT−23−3
SN1 SUFFIX
CASE 318

NCP431
Pin 1. Reference
2. Cathode
3. Anode

NCP432
Pin 1. Cathode
2. Reference
3. Anode

ORDERING AND MARKING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 13 of this data sheet.

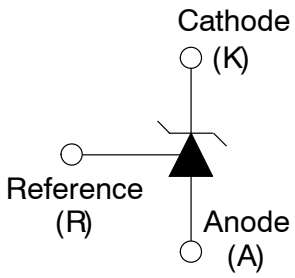


Figure 1. Symbol

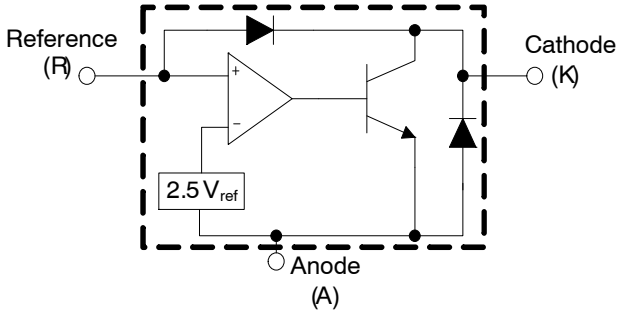


Figure 2. Representative Block diagram

MAXIMUM RATINGS (Full operating ambient temperature range applies, unless otherwise noted)

Symbol	Rating	Value	Unit
V_{KA}	Cathode to Anode Voltage	37	V
I_K	Cathode Current Range, Continuous	−100 to +150	mA
I_{ref}	Reference Input Current Range, Continuous	−0.05 to +10	mA
T_J	Operating Junction Temperature	150	°C
T_A	Operating Ambient Temperature Range	−40 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
P_D	Total Power Dissipation @ T_A = 25°C Derate above 25°C Ambient Temperature D, LP Suffix Plastic Package SN1 Suffix Plastic Package	 0.70 0.52	W
P_D	Total Power Dissipation @ T_C = 25°C Derate above 25°C Case Temperature D, LP Suffix Plastic Package	1.5	W
HBM MM	ESD Rating	>2000 >200	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Condition	Min	Max	Unit
V_{KA}	Cathode to Anode Voltage	V_{ref}	36	V
I_K	Cathode Current	0.04	100	mA

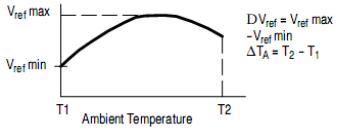
THERMAL CHARACTERISTICS

Symbol	Characteristic	LP Suffix Package (50 mm² x 35 μm Cu)	D Suffix Package (50 mm² x 35 μm Cu)	SN1 Suffix Package (10 mm² x 35 μm Cu)	Unit
$R_{\Theta JA}$	Thermal Resistance, Junction−to−Ambient	176	210	255	°C/W
$R_{\Theta JL}$	Thermal Resistance, Junction−to−Lead (Lead 3)	75	68	80	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C, unless otherwise noted.)

Symbol	Characteristic	NCP431AC			NCP431AI			NCP431AV			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{ref}	Reference Input Voltage $V_{KA} = V_{ref}$, I_K = 1 mA T_A = 25°C $T_A = T_{low}$ to T_{high} (Note 1)	 2.475 2.475	 2.500 2.500	 2.525 2.525	 2.475 2.465	 2.500 2.500	 2.525 2.525	 2.475 2.460	 2.500 2.500	 2.525 2.525	V
ΔV_{refT}	Reference Input Voltage Deviation Over Temperature Range (Figure 1, Notes 2, 3) $V_{KA} = V_{ref}$, I_K = 1 mA	–	–	–	–	5.0	10	–	10	15	mV
$\frac{\Delta V_{ref}}{\Delta V_{AK}}$	Ratio of Change in Reference Input Voltage to Change in Cathode to Anode Voltage I_K = 1 mA (Figure 2), ΔV_{KA} = 10 V to V_{ref} ΔV_{KA} = 36 V to 10 V	 – –	 −2.00 −1.28	 −3.1 −1.9	 – –	 −2.00 −1.28	 −3.1 −1.9	 – –	 −2.00 −1.28	 −3.1 −1.9	mV/V
I_{ref}	Reference Input Current (Figure 2) I_K = 1 mA, R1 = 220 k, R2 = ∞ T_A = −40°C to +125°C	–	81	190	–	81	190	–	81	190	nA
ΔI_{refT}	Reference Input Current Deviation Over Temperature Range (Figure 2, Note 2, 3) I_K = 1 mA, R1 = 10 k, R2 = ∞	–	22	55	–	22	55	–	22	55	nA
I_{min}	Minimum Cathode Current For Regulation $V_{KA} = V_{ref}$ (Figure 1)	–	40	80	–	40	80	–	40	80	μA
I_{off}	Off−State Cathode Current (Figure 3) V_{KA} = 36 V, V_{ref} = 0 V	–	180	1000	–	180	1000	–	180	1000	nA
$\lvert Z_{KA} \rvert$	Dynamic Impedance (Figure 1, Note 3) $V_{KA} = V_{ref}$, ΔI_K = 1.0 mA to 100 mA f ≤ 1.0 kHz	–	0.22	0.5	–	0.22	0.5	–	0.22	0.5	Ω

1. T_{low} = −40°C for NCP431AI, NCP431AV
   = 0°C for NCP431AC
   T_{high} = 70°C for NCP431AC
   = 85°C for NCP431AI
   = 125°C for NCP431AV
2. Guaranteed by design
3. The deviation parameter ΔV_{refT} is defined as the difference between the maximum and minimum values obtained over the full operating ambient temperature range that applies.



The average temperature coefficient of the reference input voltage, Vref is defined as:

$$V_{ref}\frac{ppm}{^\circ C} = \frac{\left(\frac{\Delta V_{ref}}{V_{ref@25^\circ C}}\right) \times 10^6}{\Delta T_A} = \frac{\Delta V_{ref} \times 10^6}{\Delta T_A\left(V_{ref@25^\circ C}\right)}$$

αVref can be positive or negative depending on whether Vref Min or Vref Max occurs at the lower ambient temperature.

Example: ΔV_{refT} = 17 mV and slope is positive
V_{ref} = 2.5 V, ΔT_A = 165°C (from −40°C to +125°C)

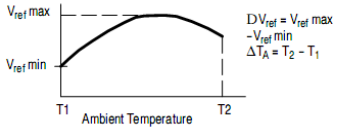
$$\alpha V_{ref} = \frac{0.017 \cdot 10^6}{165 \cdot 2.5} = 41.2 \text{ ppm}/^\circ C$$

4. The dynamic impedance Z_{KA} is defined as: $|Z_{KA}| = (\Delta V_{KA}/\Delta I_K)$. When the device is programmed with two external resistors, R1 and R2, the total dynamic impedance of the circuit is defined as: $|Z_{KA}'| \approx |Z_{KA}| (1 + (R1/R2))$

ELECTRICAL CHARACTERISTICS (T_A = 25°C, unless otherwise noted.)

Symbol	Characteristic	NCP431BC NCP432BC			NCP431BI NCP432BI			NCP431BV NCP432BV			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{ref}	Reference Input Voltage V_{KA} = V_{ref}, I_K = 1 mA T_A = 25°C T_A = T_{low} to T_{high} (Note 5)	 2.4875 2.4875	 2.500 2.500	 2.5125 2.5125	 2.4875 2.4775	 2.500 2.500	 2.5125 2.5125	 2.4875 2.4725	 2.500 2.500	 2.5125 2.5125	V
ΔV_{refT}	Reference Input Voltage Deviation Over Temperature Range (Figure 1, Notes 6, 7) V_{KA}= V_{ref}, I_K = 1 mA	– –	–	– –	– –	5.0	10 1–	– –	10	15 15	mV
$\frac{\Delta V_{ref}}{\Delta V_{AK}}$	Ratio of Change in Reference Input Voltage to Change in Cathode to Anode Voltage I_K = 1 mA (Figure 2), ΔV_{KA} = 10 V to V_{ref} ΔV_{KA} = 36 V to 10 V	 – –	 –2.00 –1.28	 –3.1 –1.9	 – –	 –2.00 –1.28	 –3.1 –1.9	 – –	 –2.00 –1.28	 –3.1 –1.9	mV/V
I_{ref}	Reference Input Current (Figure 2) I_K = 1 mA, R1 = 220 k, R2 = ∞ T_A = –40°C to +125°C	–	81	190	–	81	190	–	81	190	nA
ΔI_{refT}	Reference Input Current Deviation Over Temperature Range (Figure 2, Note 6, 7) I_K = 1 mA, R1 = 10 k, R2 = ∞	–	22	55	–	22	55	–	22	55	nA
I_{min}	Minimum Cathode Current For Regulation V_{KA} = V_{ref} (Figure 1)	–	40	80	–	40	80	–	40	80	μA
I_{off}	Off–State Cathode Current (Figure 3) V_{KA} = 36 V, V_{ref} = 0 V	–	180	1000	–	180	1000	–	180	1000	nA
$\lvert Z_{KA}\rvert$	Dynamic Impedance (Figure 1, Note 7) V_{KA} = V_{ref}, ΔI_K = 1.0 mA to 100 mA f ≤ 1.0 kHz	–	0.22	0.5	–	0.22	0.5	–	0.22	0.5	Ω

5. T_{low} = –40°C for NCP431BI, NCP431BV, NCP432BI, NCP432BV
   = 0°C for NCP431BC, NCP432BC
   T_{high} = 70°C for NCP431BC, NCP432BC
   = 85°C for NCP431BI, NCP432BI
   = 125°C for NCP431BV, NCP432BV
6. Guaranteed by design
7. The deviation parameter ΔV_{refT} is defined as the difference between the maximum and minimum values obtained over the full operating ambient temperature range that applies.



The average temperature coefficient of the reference input voltage, Vref is defined as:

$$V_{ref}\frac{ppm}{^\circ C} = \frac{\left(\frac{\Delta V_{ref}}{V_{ref@25^\circ C}}\right) \times 10^6}{\Delta T_A} = \frac{\Delta V_{ref} \times 10^6}{\Delta T_A\left(V_{ref@25^\circ C}\right)}$$

αVref can be positive or negative depending on whether Vref Min or Vref Max occurs at the lower ambient temperature.

Example: ΔV_{refT} = 17 mV and slope is positive
V_{ref} = 2.5 V, ΔT_A = 165°C (from –40°C to +125°C)

$$\alpha V_{ref} = \frac{0.017 \cdot 10^6}{165 \cdot 2.5} = 41.2\ ppm/^\circ C$$

8. The dynamic impedance Z_{KA} is defined as: $|Z_{KA}| = (\Delta V_{KA}/\Delta I_K)$. When the device is programmed with two external resistors, R1 and R2, the total dynamic impedance of the circuit is defined as: $|Z_{KA}'| \approx |Z_{KA}| (1 + (R1/R2))$

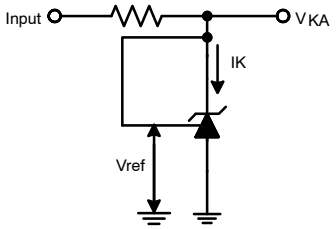


Figure 3. Test Circuit for $V_{KA} = V_{ref}$

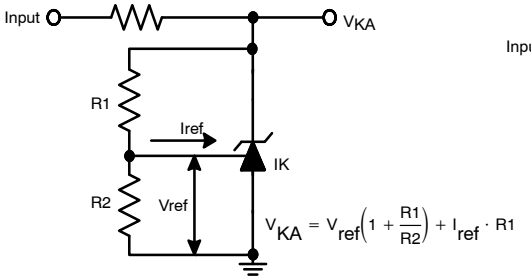


Figure 4. Test Circuit for $V_{KA} > V_{ref}$

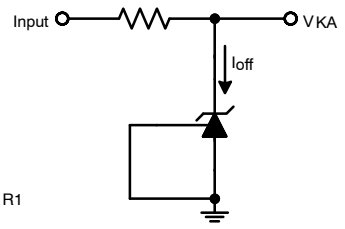


Figure 5. Test Circuit for I_{off}

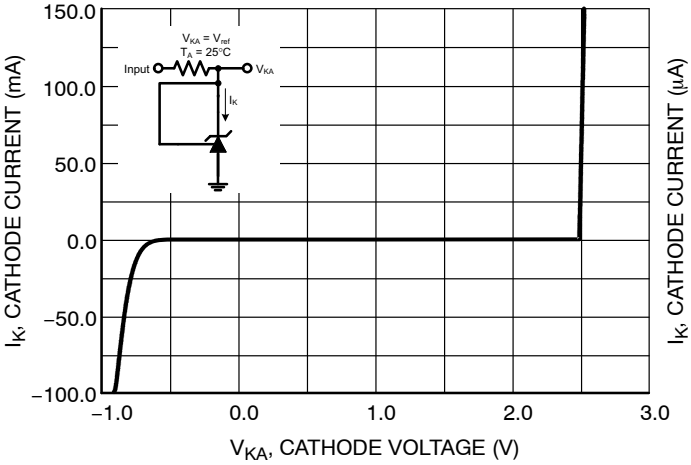


Figure 6. Cathode Current versus Cathode Voltage

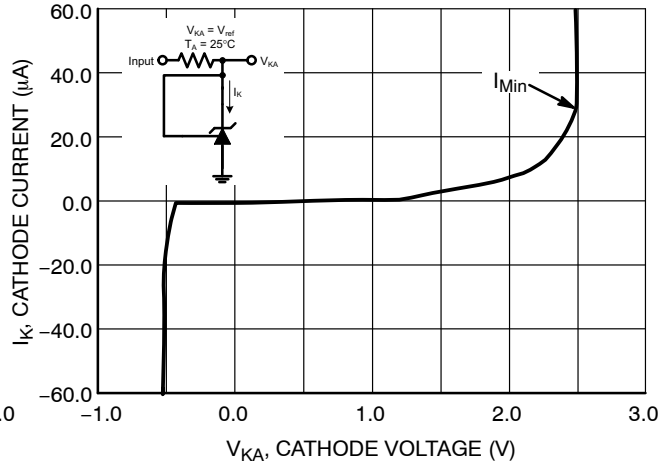


Figure 7. Cathode Current versus Cathode Voltage

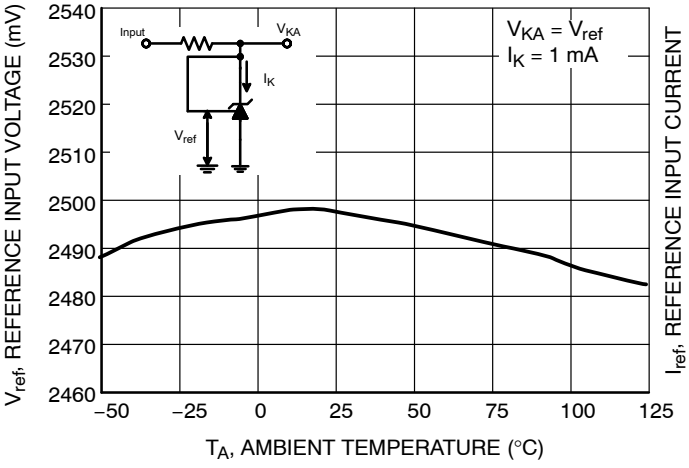


Figure 8. Reference Input Voltage versus Ambient temperature

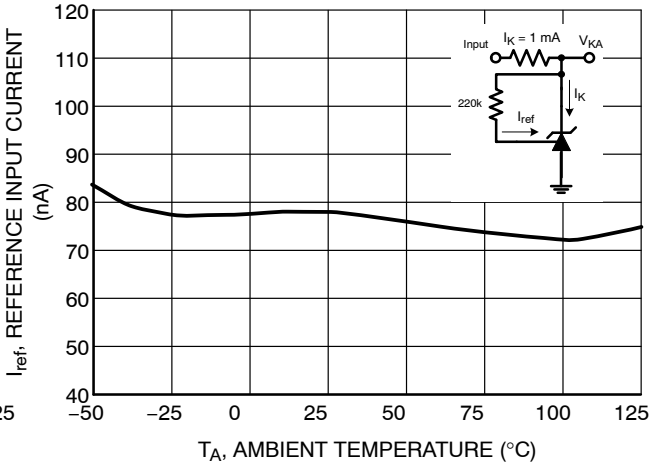


Figure 9. Reference Input Current versus Ambient temperature

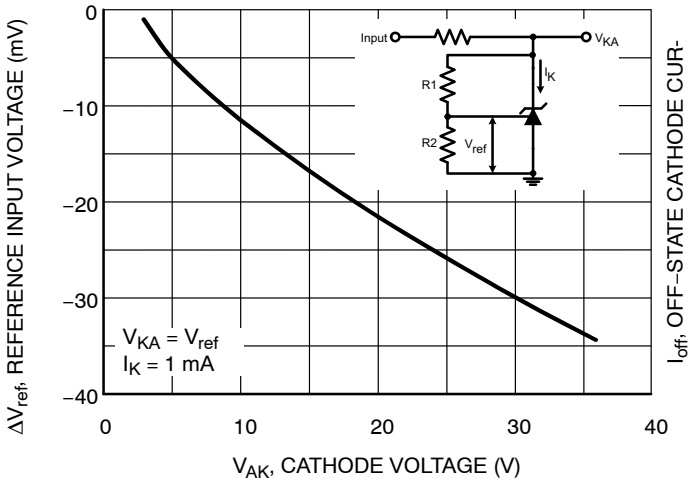


Figure 10. Change in Reference Input Voltage versus Cathode Voltage

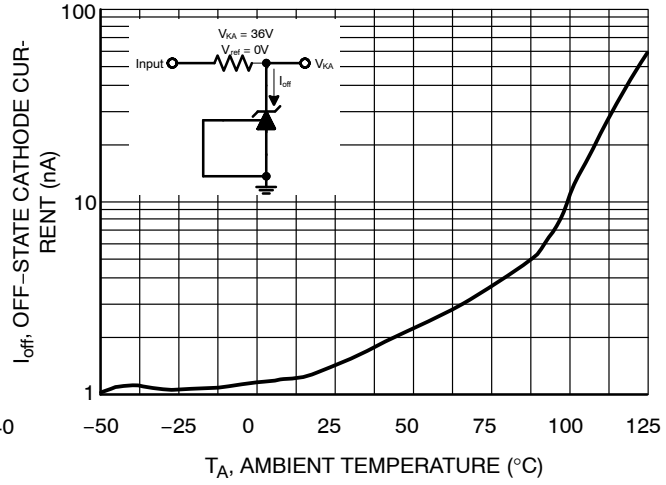


Figure 11. Off−State Cathode Current versus Ambient Temperature

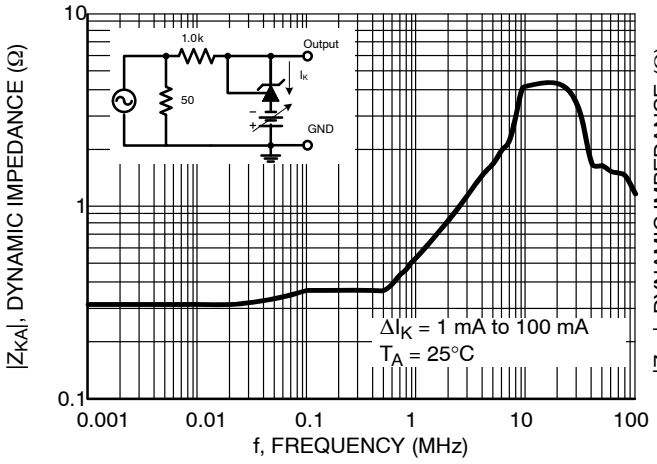


Figure 12. Dynamic Impedance versus Frequency

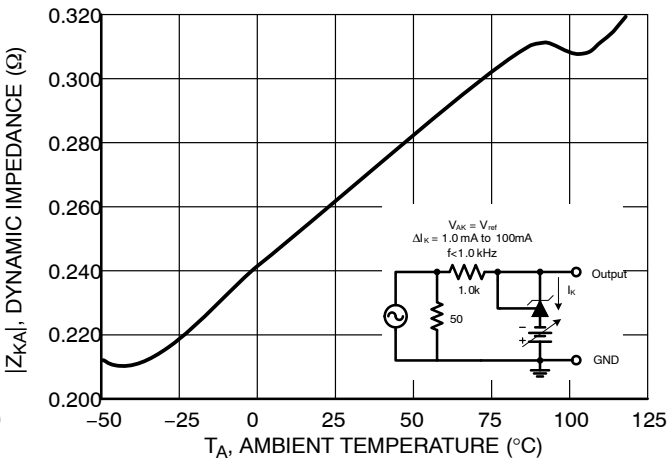


Figure 13. Dynamic Impedance versus Ambient Temperature

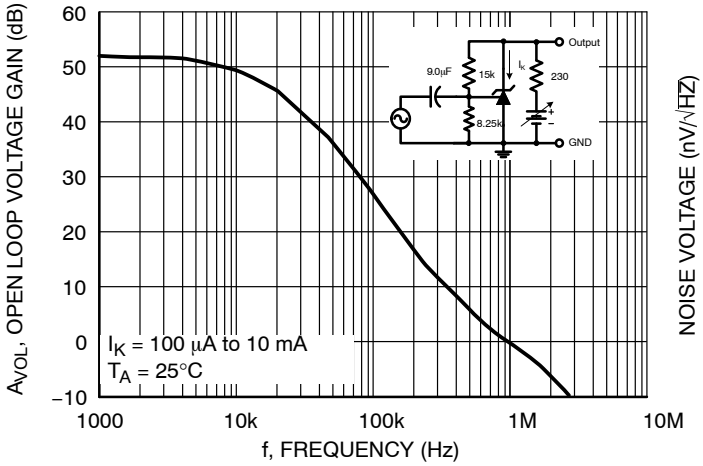


Figure 14. Open−Loop Voltage Gain versus Frequency

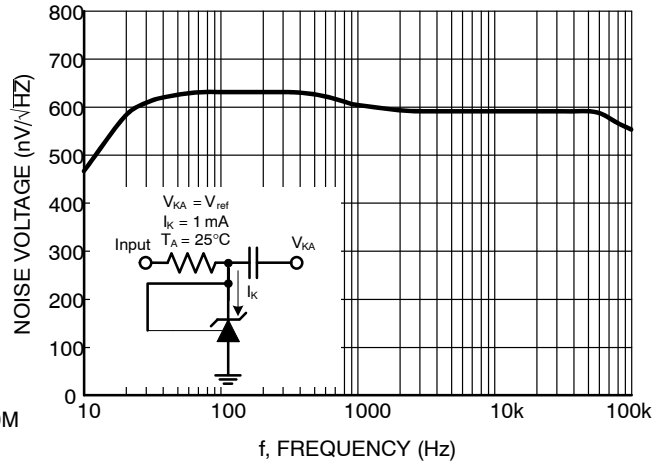


Figure 15. Spectral Noise Density

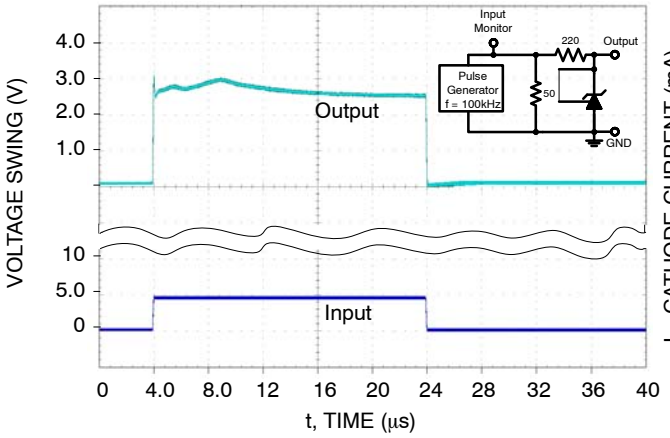


Figure 16. Pulse Response

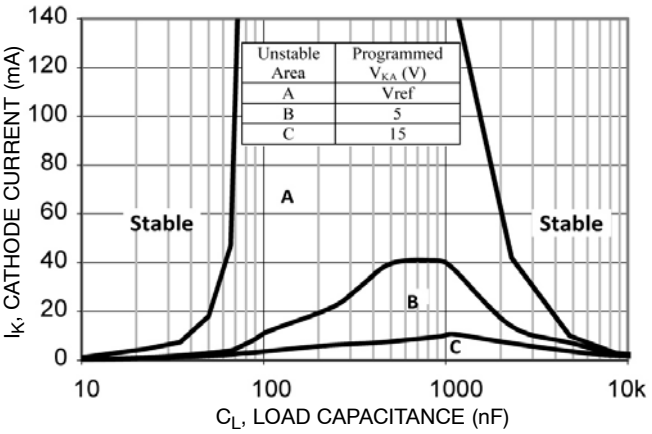


Figure 17. Stability Boundary Conditions

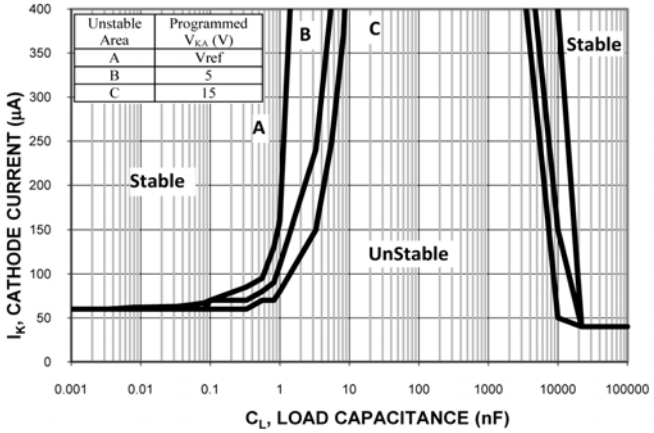


Figure 18. Stability Boundary Conditions for Small Cathode Current

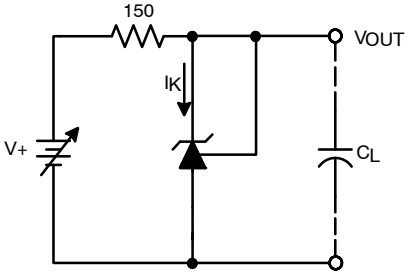


Figure 19. Test Circuit For Curve A of Stability Boundary Conditions

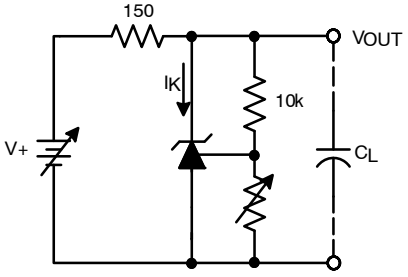


Figure 20. Test Circuit For Curve B And C of Stability Boundary Conditions

TYPICAL APPLICATIONS

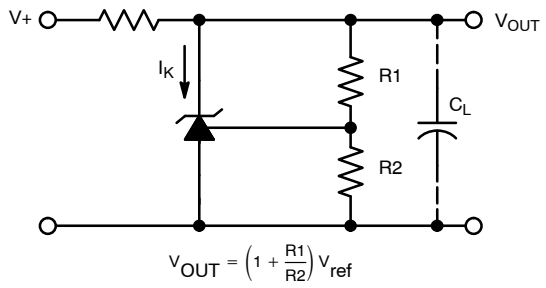


Figure 21. Shunt Regulator

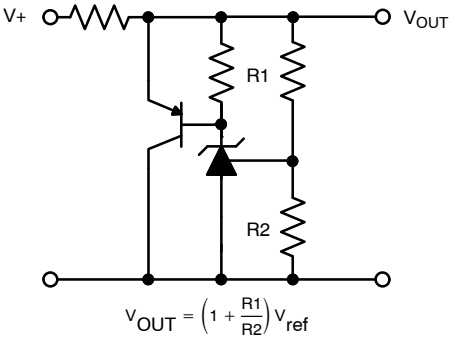


Figure 22. High Current Shunt Regulator

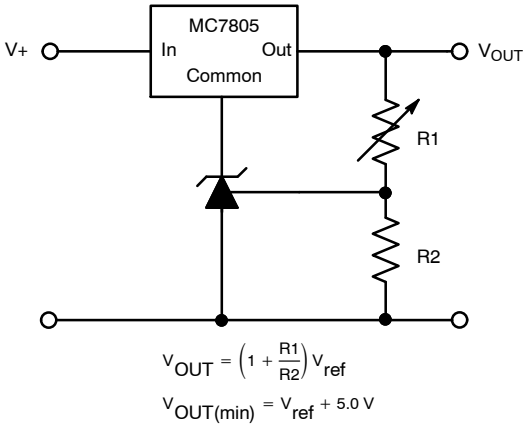


Figure 23. Output Control for a Tree−Terminal Fixed Regulator

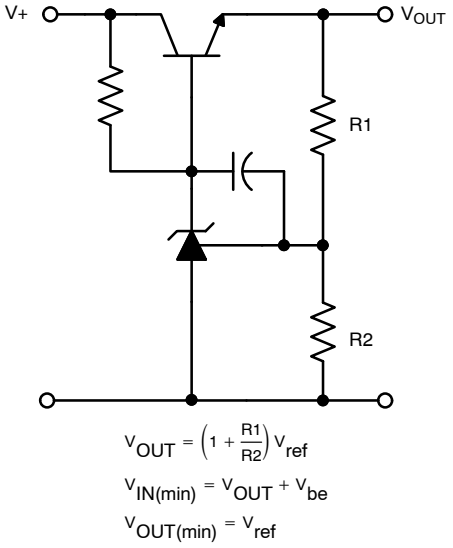


Figure 24. Series Pass Regulator

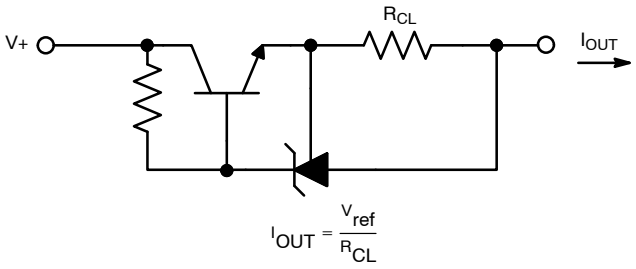


Figure 25. Constant Current Source

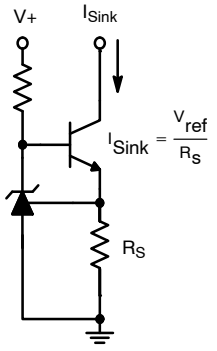


Figure 26. Constant Current Sink

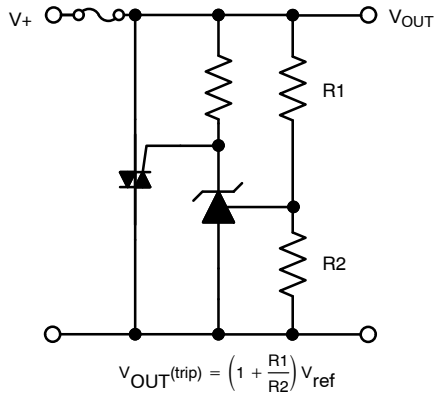


Figure 27. Triac Crowbar

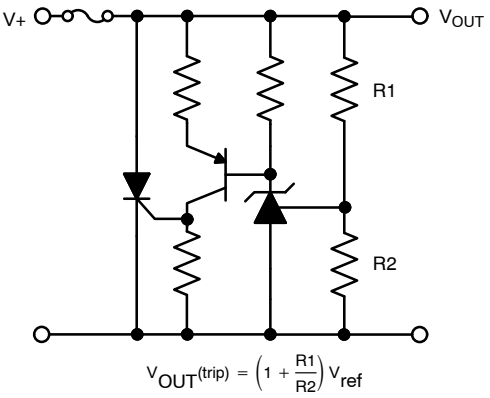


Figure 28. SRC Crowbar

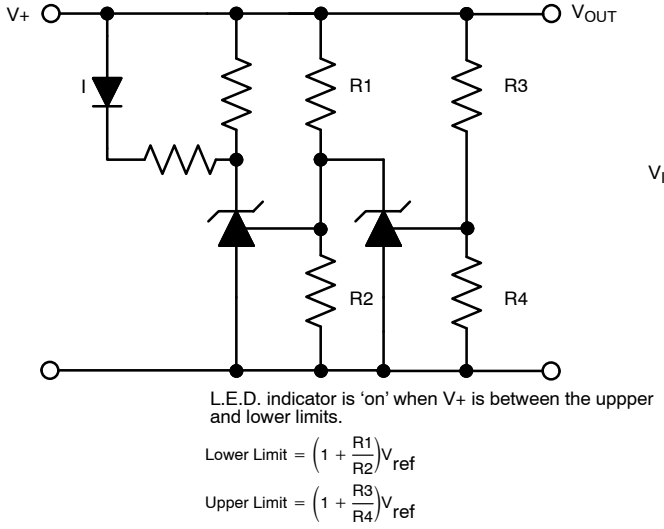
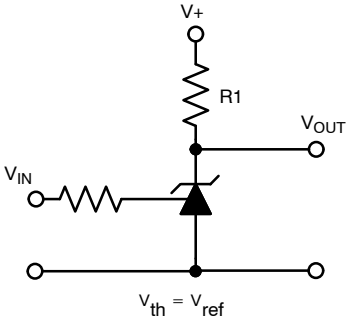


Figure 29. Voltage Monitoring



V_{IN}	V_{OUT}
< V_{ref}	V+
> V_{ref}	≈2.0 V

Figure 30. Single−Supply Comparator with Temperature−Compensated Threshold

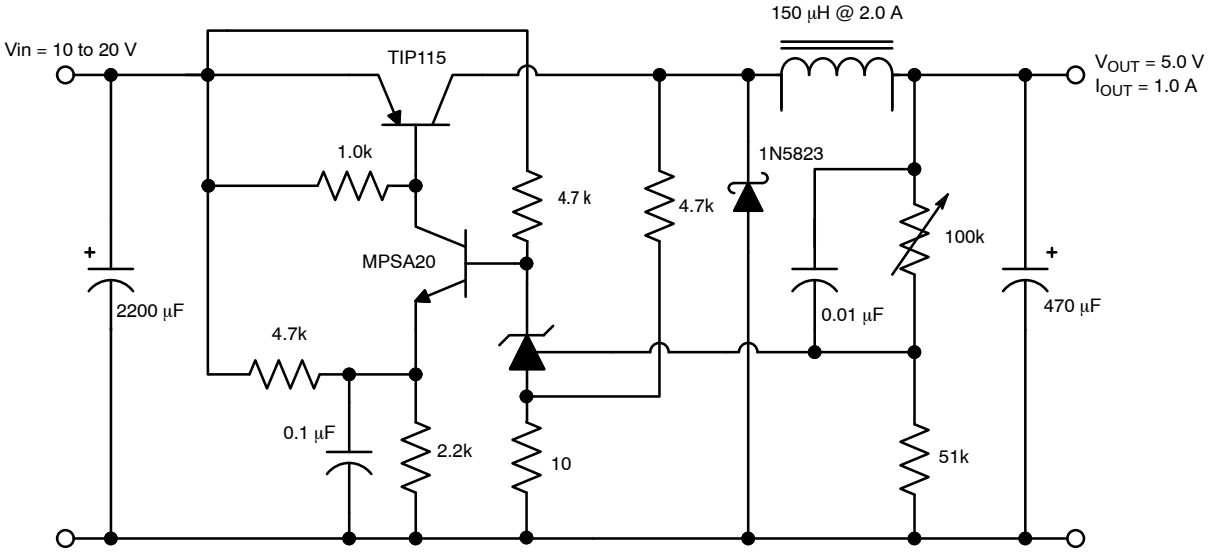


Figure 31. Step−Down Switching Converter

APPLICATIONS INFORMATION

The NCP431/NCP432 is a programmable precision reference which is used in a variety of ways. It serves as a reference voltage in circuits where a non−standard reference voltage is needed. Other uses include feedback control for driving an optocoupler in power supplies, voltage monitor, constant current source, constant current sink and series pass regulator. In each of these applications, it is critical to maintain stability of the device at various operating currents and load capacitances. In some cases the circuit designer can estimate the stabilization capacitance from the stability boundary conditions curve provided in Figure 17. However, these typical curves only provide stability information at specific cathode voltages and at a specific load condition. Additional information is needed to determine the capacitance needed to optimize phase margin or allow for process variation.

A simplified model of the NCP431/NCP432 is shown in Figure 32. When tested for stability boundaries, the load resistance is 150 Ω. The model reference input consists of an input transistor and a dc emitter resistance connected to the device anode. A dependent current source, Gm, develops a current whose amplitude is determined by the difference between the 1.78 V internal reference voltage source and the input transistor emitter voltage. A portion of Gm flows through compensation capacitance, CP2. The voltage across CP2 drives the output dependent current source, Go, which is connected across the device cathode and anode.

Model component values are:
Vref = 1.78 V
Gm = 0.3 + 2.7 exp (−IC/26 mA)
where IC is the device cathode current and Gm is in mhos
Go = 1.25 (Vcp2) μmhos.

Resistor and capacitor typical values are shown on the model. Process tolerances are ±20% for resistors, ±10% for capacitors, and ±40% for transconductances.

An examination of the device model reveals the location of circuit poles and zeroes:

$$P1 = \frac{1}{2\pi R_{GM} C_{P1}} = \frac{1}{2\pi \cdot 1.0M \cdot 20\ pF} = 7.96\ kHz$$

$$P2 = \frac{1}{2\pi R_{P2} C_{P2}} = \frac{1}{2\pi \cdot 10M \cdot 0.265\ pF} = 60\ kHz$$

$$Z1 = \frac{1}{2\pi R_{Z1} C_{P1}} = \frac{1}{2\pi \cdot 15.9k \cdot 20\ pF} = 500\ kHz$$

In addition, there is an external circuit pole defined by the load:

$$P_L = \frac{1}{2\pi R_L C_L}$$

Also, the transfer dc voltage gain of the NCP431 is:

$$G = G_M R_{GM} Go R_L$$

Example 1:
I_C=10 mA, R_L= 230 Ω, C_L= 0. Define the transfer gain.
The DC gain is:

$$G = G_M R_{GM} Go R_L = (2.138)(1.0M)(1.25\mu)(230) = 615 = 56\ dB$$

$$\text{Loop gain} = G\frac{8.25k}{8.25k + 15k} = 218 = 47\ dB$$

The resulting transfer function Bode plot is shown in Figure 33. The asymptotic plot may be expressed as the following equation:

$$Av = 615\frac{\left(1 + \frac{jf}{500\ kHz}\right)}{\left(1 + \frac{jf}{8.0\ kHz}\right)\left(1 + \frac{jf}{60\ kHz}\right)}$$

The Bode plot shows a unity gain crossover frequency of approximately 600 kHz. The phase margin, calculated from the equation, would be 55.9°. This model matches the Open−Loop Bode Plot of Figure 14. The total loop would have a unity gain frequency of about 300 kHz with a phase margin of about 44°.

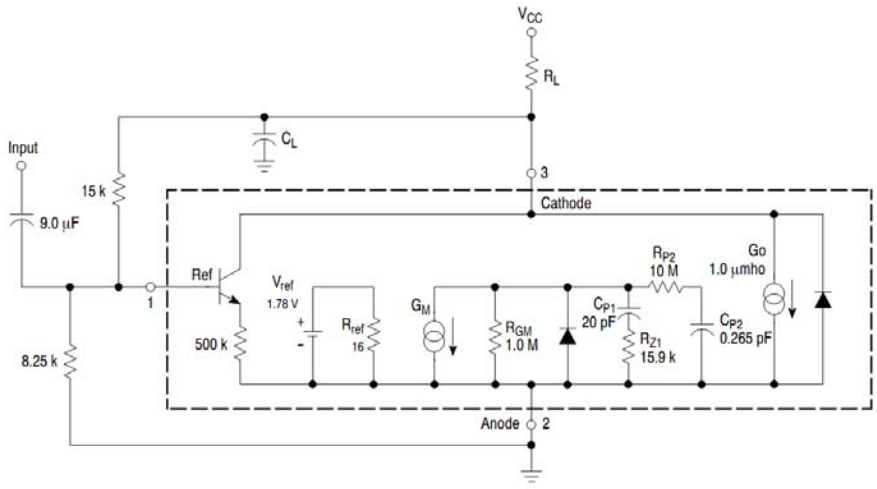


Figure 32. Simplified NCP431/NCP432 Device Model

NCP431/NCP432 OPEN−LOOP VOLTAGE GAIN VERSUS FREQUENCY

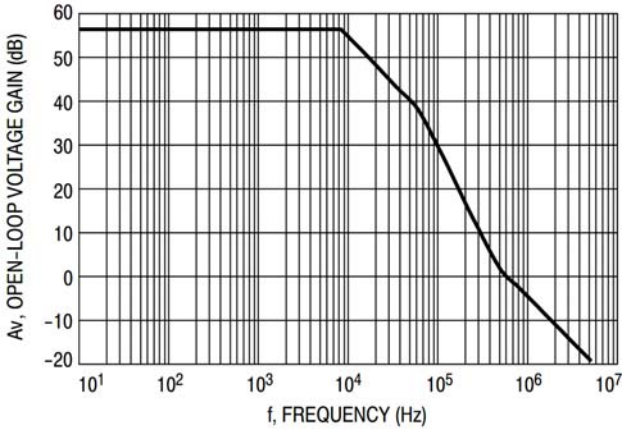


Figure 33. Example 1 Circuit Open Loop Gain Plot

Example 2.
I_C = 7.5 mA, R_L = 2.2 kΩ, C_L = 0.01 μF. Cathode tied to reference input pin. An examination of the data sheet stability boundary curve (Figure 17) shows that this value of load capacitance and cathode current is on the boundary.

Define the transfer gain.
The DC gain is:

$$G = G_M R_{GM} G_o R_L = (2.138)(1.0M)(1.25\mu)(230)$$
$$= 6389 = 76\ dB$$

The resulting open loop Bode plot is shown in Figure 34. The asymptotic plot may be expressed as the following equation:

$$Av = 615 \frac{\left(1 + \frac{jf}{500\ kHz}\right)}{\left(1 + \frac{jf}{8.0\ kHz}\right)\left(1 + \frac{jf}{60\ kHz}\right)\left(1 + \frac{jf}{7.2\ kHz}\right)}$$

Note that the transfer function now has an extra pole formed by the load capacitance and load resistance.

Note that the crossover frequency in this case is about 250 kHz, having a phase margin of about −46°. Therefore, instability of this circuit is likely.

NCP431/NCP432 OPEN−LOOP BODE PLOT WITH LOAD CAP

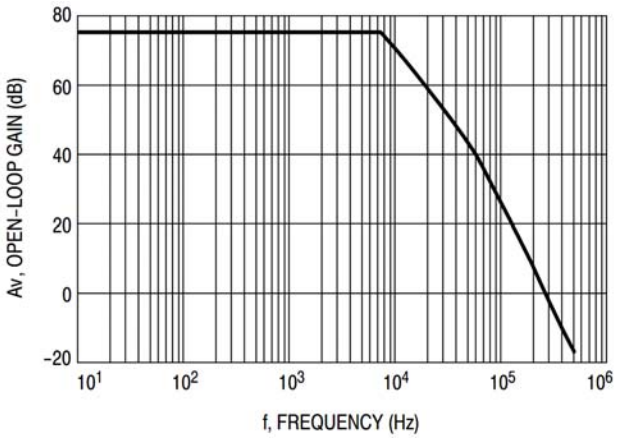


Figure 34. Example 2 Circuit Open Loop Gain Plot

With three poles, this system is unstable. The only hope for stabilizing this circuit is to add a zero. However, that can only be done by adding a series resistance to the output capacitance, which will reduce its effectiveness as a noise filter. Therefore, practically, in reference voltage applications, the best solution appears to be to use a smaller value of capacitance in low noise applications or a very large value to provide noise filtering and a dominant pole rolloff of the system.

The NCP431/NCP432 is often used as a regulator in secondary side of a switch mode power supply (SMPS).

The benefit of this reference is high and stable gain under low bias currents. Figure 35 shows dependence of the gain (dynamic impedance) on the bias current. Value of

minimum cathode current that is needed to assure stable gain is 80 μA maximum.

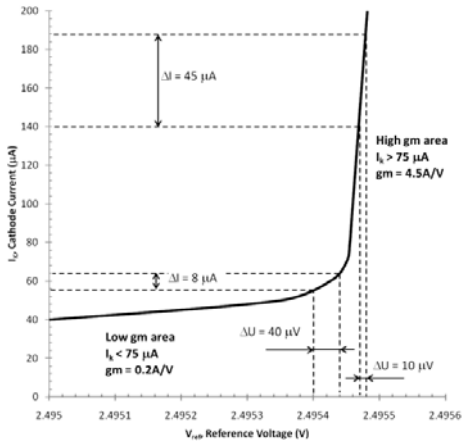


Figure 35. Knee of Reference

Regulator with TL431 or other references in secondary side of a SMPS needs bias resistor to increase cathode current to reach high and stable gain (refer to Figure 36). This bias resistor does not have to be used in regulator with NCP431/NCP432 thanks to its low minimum cathode current.

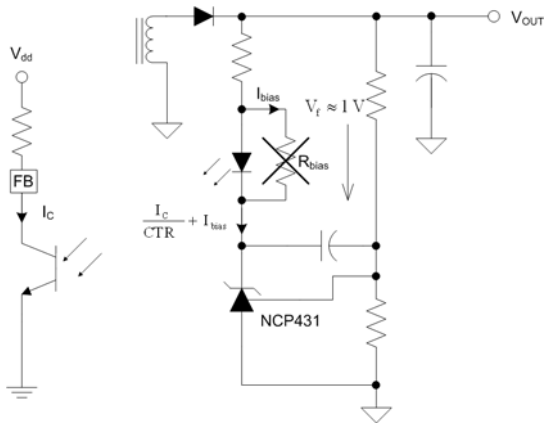
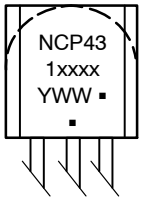


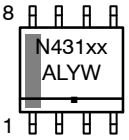
Figure 36. SMPS Secondary Side and Feedback Connection on Primary Side

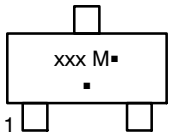
The NCP431/NCP432 operates with very low leakage and reference input current. Sum of these currents is lower than 100 nA. Regulator with the NCP431/NCP432 minimizes parasitic power consumption.

The best way to achieve extremely low no−load consumption in SMPS applications is to use NCP431/NCP432 as regulator on the secondary side. The consumption is reduced by minimum parasitic consumption and very low bias current of NCP431/NCP432.

MARKING DIAGRAMS







xx, xxx, xxx = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
M = Date Code
W, WW = Work Week
▪ = Pb−Free Package

(*Note: Microdot may be in either location)

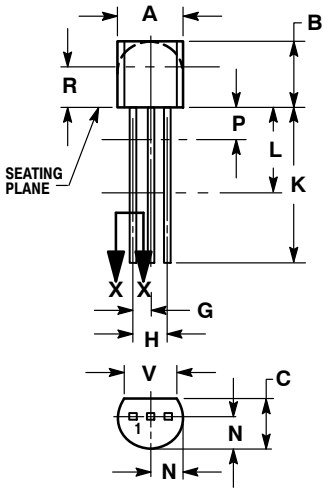
ORDERING INFORMATION

Device	Marking	Tolerance	Operating Temperature Range	Package	Shipping†
NCP431ACDR2G	AC	1%	0°C to 70°C	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCP431ACSNT1G	VRF	1%		SOT−23−3 (Pb−Free)	3000 / Tape & Reel
NCP431BCSNT1G	VRJ	0.5%		SOT−23−3 (Pb−Free)	3000 / Tape & Reel
NCP432BCSNT1G	VRM	0.5%		SOT−23−3 (Pb−Free)	3000 / Tape & Reel
NCP431ACLPRAG	ACLP	1%		TO−92 (TO−226) (Pb−Free)	2000 / Tape & Reel
NCP431AIDR2G	AI	1%	−40°C to 85°C	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCP431AISNT1G	VRG	1%		SOT−23−3 (Pb−Free)	3000 / Tape & Reel
NCP431BISNT1G	VRK	0.5%		SOT−23−3 (Pb−Free)	3000 / Tape & Reel
NCP432BISNT1G	VRN	0.5%		SOT−23−3 (Pb−Free)	3000 / Tape & Reel
NCP431AILPRAG	AILP	1%		TO−92 (TO−226) (Pb−Free)	2000 / Tape & Reel
NCP431AVDR2G	AV	1%	−40°C to 125°C	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCP431AVSNT1G	VRH	1%		SOT−23−3 (Pb−Free)	3000 / Tape & Reel
NCP431AVLPRAG	AVLP	1%		TO−92 (TO−226) (Pb−Free)	2000 / Tape & Reel
NCP431AVLPG	AVLP	1%		TO−92 (TO−226) (Pb−Free)	2000 Units / Bag
NCP431BVSNT1G	VRL	0.5%		SOT−23−3 (Pb−Free)	3000 / Tape & Reel
NCP432BVSNT1G	VRP	0.5%		SOT−23−3 (Pb−Free)	3000 / Tape & Reel

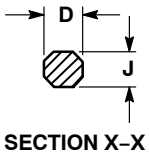
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

TO−92 (TO−226)
CASE 29−11
ISSUE AN



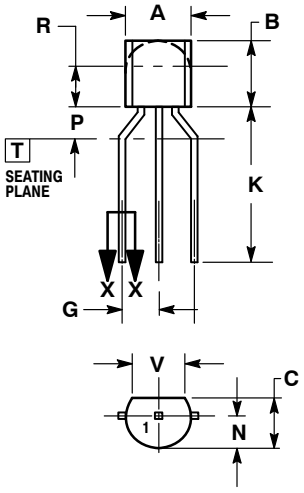
STRAIGHT LEAD



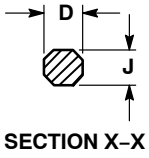
SECTION X−X

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.175	0.205	4.45	5.20
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.021	0.407	0.533
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
K	0.500	---	12.70	---
L	0.250	---	6.35	---
N	0.080	0.105	2.04	2.66
P	---	0.100	---	2.54
R	0.115	---	2.93	---
V	0.135	---	3.43	---



BENT LEAD



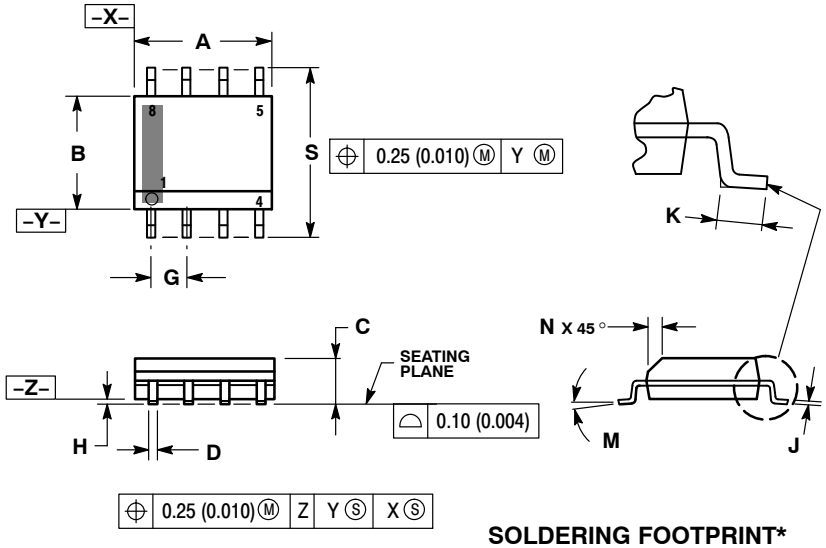
SECTION X−X

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

	MILLIMETERS	
DIM	MIN	MAX
A	4.45	5.20
B	4.32	5.33
C	3.18	4.19
D	0.40	0.54
G	2.40	2.80
J	0.39	0.50
K	12.70	---
N	2.04	2.66
P	1.50	4.00
R	2.93	---
V	3.43	---

PACKAGE DIMENSIONS

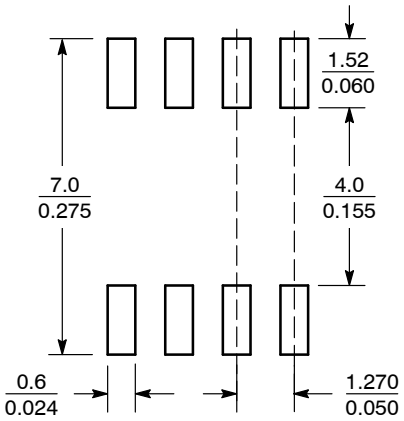
SOIC−8 NB
CASE 751−07
ISSUE AK



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*

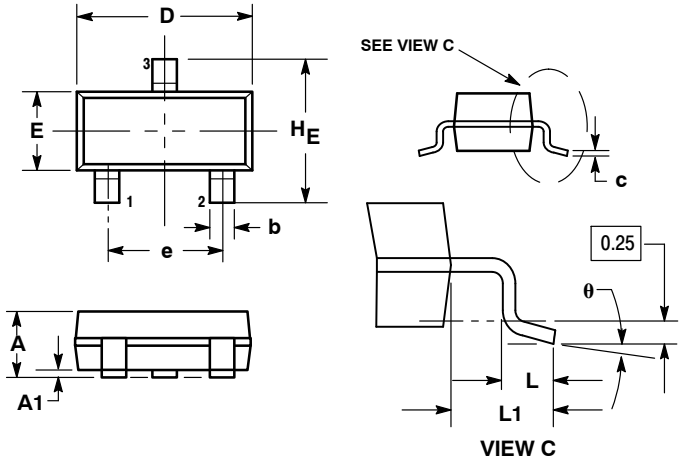


SCALE 6:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

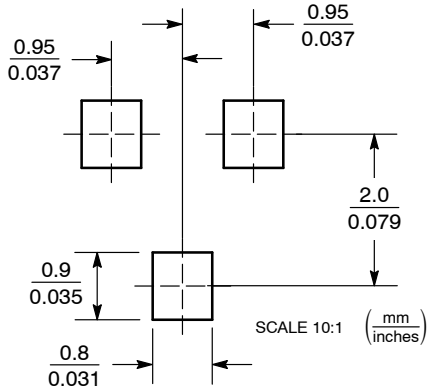
SOT−23 (TO−236)
CASE 318−08
ISSUE AP



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1.00	1.11	0.035	0.040	0.044
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.37	0.44	0.50	0.015	0.018	0.020
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.081
L	0.10	0.20	0.30	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
H_E	2.10	2.40	2.64	0.083	0.094	0.104
θ	0°	−−−	10°	0°	−−−	10°

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

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Phone: 421 33 790 2910
Japan Customer Focus Center
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ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative

NCP431/D