NCP1501

Dual Mode PWM/Linear Buck Converter

The NCP1501 is a dual mode regulator that operates either as a PWM Buck Converter or as a Low Drop Out Linear Regulator. If a synchronization signal is present, the NCP1501 operates as a current mode PWM converter with synchronous rectification. The synchronization signal allows the user to control the location of the spurious frequency noise generated by a PWM converter. Linear mode is active when a synchronization signal is not present. The NCP1501 configuration allows an efficient high power operation and low noise during system sleep modes.

Features

- Synchronous Rectification for Higher Efficiency in PWM Mode
- Linear Mode Operation for Low Noise Output at Low Loads
- Integrated MOSFETs and Feedback Circuits
- Cycle-by-Cycle Peak Current Limit of 800 mA (typ)
- Automatic Switching Between PWM and Linear Mode
- Operating Frequency Range of 500 to 1000 kHz
- Optimized for Ceramic Capacitors and Low Profile Inductors
- Thermal Limit Protection
- Built-in Slope Compensation for Current Mode PWM Converter
- Fixed Output Voltages of 1.05 V, 1.35 V, 1.57 V, 1.8 V
- Shutdown Current Consumption of 0.2 μA
- Internal Soft Start
- Transistor Count: 3500
- Pb-Free Package is Available

Typical Applications

- Cellular Phones
- PDAs
- Pagers
- Supplies for DSP Cores
- Portable Applications

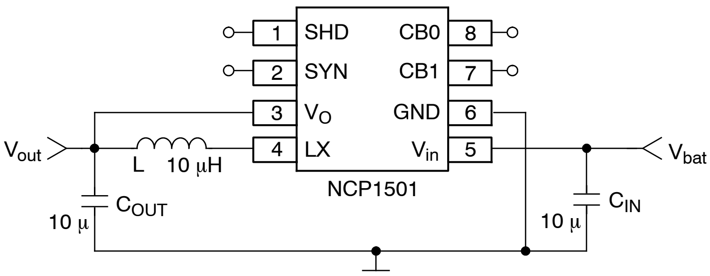

Figure 1. Typical Applications Circuit

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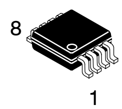
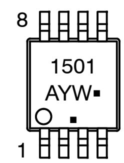
MARKING DIAGRAM

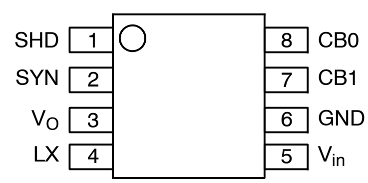


Micro8™ (MSOP-8) DM SUFFIX CASE 846A



A = Assembly Location
Y = Year
W = Work Week
▪ = Pb-Free Package
(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP1501DMR2	Micro8	4000/Tape & Reel
NCP1501DMR2G	Micro8 (Pb-Free)	4000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PIN FUNCTION DESCRIPTIONS

Pin #	Symbol	Pin Description
1	SHD	Enable Pin for the NCP1501. This pin is active high. Internal pull down resistor forces the part off if the pin is not connected on the board.
2	SYN	External Synchronization Signal Pin. The device will operate in PWM mode if a clock signal is present. The pin must be pulled low to enter LDO mode. Internal pull down resistor on pin.
3	V_O	Feedback for the NCP1501. An internal MOSFET is connected across V_O and LX for LDO mode.
4	LX	Connection for the pass devices to the inductor.
5	V_{in}	Input voltage to the NCP1501.
6	GND	Ground Connection for the device.
7	CB1	Voltage Selection Bit. Internal pull up resistor on pin.
8	CB0	Voltage Selection Bit. Internal pull down resistor on pin.

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Maximum Voltage All Pins		V_{max}	5.5	V
Maximum operating Voltage All Pins		V_{max}	5.2	V
Thermal Resistance, Junction-to-Air		$R_{\theta JA}$	240	°C/W
Operating Ambient Temperature Range		T_A	-30 to +85	°C
ESD Withstand Voltage	Human Body Model (Note 1) Machine Model (Note 2)	V_{ESD}	> 2500 > 100	V
Moisture Sensitivity		MSL	Level 1	
Storage Temperature Range		T_{stg}	-55 to +150	°C
Junction Operating Temperature Range		T_J	-30 to +125	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

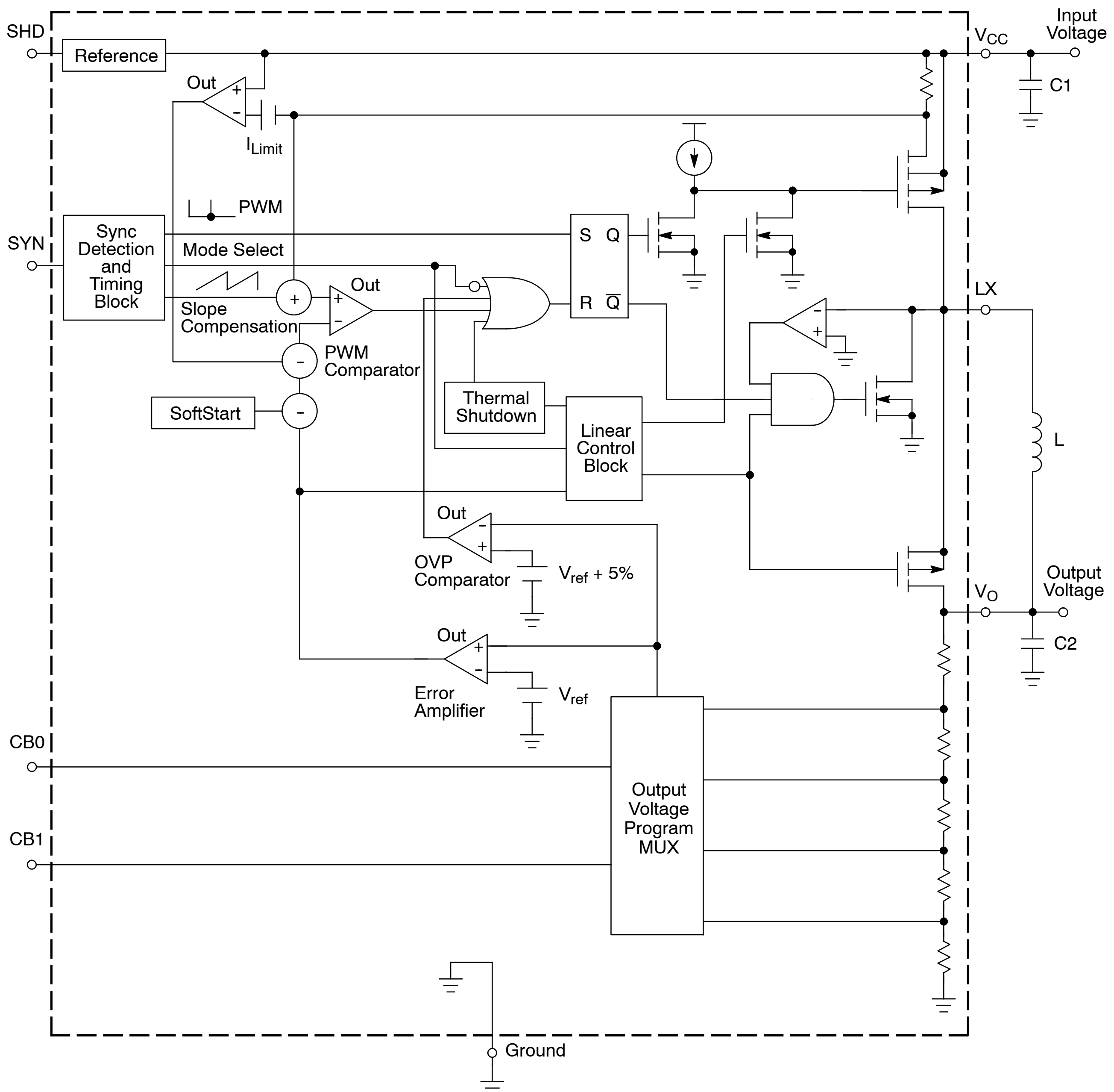
1. Tested to EIA/JESD22-A114-A
2. Tested to EIA/JESD22-A115-A

ELECTRICAL CHARACTERISTICS (V_{in} = 3.6 V, V_O = 1.57 V, T_A = 25°C, F_{syn} = 600 kHz 50% Duty Cycle square wave for PWM mode; T_A = -30 to 85°C for Min/Max values, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
V_{CC} Pin					
Quiescent Current of Switching Mode, I_{out} = 0 mA	Iq PWM	-	124	500	μA
Quiescent Current of LDO Mode, I_{out} = 0 mA	Iq LDO	-	32	65	μA
Quiescent Current, SHD Low	Iq Off	-	0.2	1.0	μA
Input Voltage Range	V_{in}	2.7	-	5.2	V
Sync Pin					
Input Voltage	V_{sync}	-0.3	-	V_{CC}+0.3	V
Frequency Operational Range	F_{sync}	500	-	1000	kHz
Minimum Synchronization Pulse Width	$Dc_{sync(min)}$	-	30	-	%
Maximum Synchronization Pulse Width	$Dc_{sync(max)}$	-	70	-	%
SYNC “H” Voltage Threshold	$V_{sync(H)}$	-	920	1200	mV
SYNC “L” Voltage Threshold	$V_{sync(L)}$	400	830	-	mV
SYNC “H” Input Current, V_{sync} = 3.6 V	$I_{sync(H)}$	-	1.8	-	μA
SYNC “L” Input Current, V_{sync} = 0 V	$I_{sync(L)}$	-0.5	0.005	-	μA

ELECTRICAL CHARACTERISTICS (continued) (V_{in} = 3.6 V, V_O = 1.57 V, T_A = 25°C, F_{syn} = 600 kHz 50% Duty Cycle square wave for PWM mode; T_A = −30 to 85°C for Min/Max values, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Level Selection Pins					
Input Voltage	V_{CB}	−0.3	–	V_{CC}+0.3	V
CB0,1 “H” Voltage Threshold	$V_{CB(H)}$	–	910	1200	mV
CB0,1 “L” Voltage Threshold	$V_{CB(L)}$	400	850	–	mV
CB0,1 “H” Input Current, CBx = 3.6 V	$I_{CB(H)}$	–	1.8	–	μA
CB0,1 “L” Input Current, CBx = 0 V	$I_{CB(L)}$	−0.5	0	–	μA
Shutdown Pin					
Input Voltage	V_{SHD}	−0.3	–	V_{CC}+0.3	V
SHD “H” Voltage Threshold	$V_{SHD(H)}$	–	920	1200	mV
SHD “L” Voltage Threshold	$V_{SHD(L)}$	400	850	–	mV
SHD “H” Input Current, SHD = 3.6 V	$I_{SHD(H)}$	–	1.8	–	μA
SHD “L” Input Current, SHD = 0 V	$I_{SHD(L)}$	−0.5	0	–	μA
Feedback Pin					
Input Voltage	V_{fb}	−0.3	–	V_{CC}+0.3	V
Input Current, V_{fb} = 1.8 V	I_{fb}	–	8.5	–	μA
PWM Mode Characteristics					
Switching P−FET Current Limit	I_{lim}	–	800	–	mA
Duty Cycle	DC	–	–	100	%
Minimum On Time	$T_{on(min)}$	–	100	–	nsec
$R_{DS(on)}$ Switching N−FET P−FET	$R_{DS(on)}$	 – –	 0.7 0.6	 – –	Ohms
Switching P−FET and N−FET Leakage Current	I_{leak}	–	0.01	10	μA
Output Over Voltage Threshold	V_O	–	3.0	–	%
Output Voltage Accuracy, $Vout_{(set)}$ = 1.05 V CB0 = L, CB1 = L $Vout_{(set)}$ = 1.35 V CB0 = L, CB1 = H $Vout_{(set)}$ = 1.57 V CB0 = H, CB1 = H $Vout_{(set)}$ = 1.80 V CB0 = H CB1 = L	V_{out}	1.018 1.309 1.523 1.740	1.050 1.350 1.570 1.800	1.082 1.391 1.617 1.860	V
Load Transient Response, 10 to 100 mA Load Step	V_{out}	–	40	–	mV
Line Transient Response, I_{out} = 100 mA, 3.0 to 3.6 V_{in} Line Step	V_{out}	–	±5	–	mV_{pp}
LDO Mode Characteristics					
$R_{DS(on)}$ LDO FET (Inductor Switch), LX to V_{out}	$R_{DS(on)}$	–	7.0	–	Ohms
Dropout Voltage (Limited by $V_{in(min)}$ = 2.5 V and $V_{out(max)}$ = 1.8 V)	V_{in} − V_{out}	–	0.7	–	V
Output Voltage Accuracy, $Vout_{(set)}$ = 1.05 V CB0 = L, CB1 = L $Vout_{(set)}$ = 1.35 V CB0 = L, CB1 = H $Vout_{(set)}$ = 1.57 V CB0 = H, CB1 = H $Vout_{(set)}$ = 1.80 V CB0 = H CB1 = L	V_{out}	1.018 1.309 1.523 1.740	1.050 1.350 1.570 1.800	1.082 1.391 1.617 1.860	V
Thermal Shutdown					
Thermal Shutdown	TSD	–	160	–	°C
Hysteresis	TSD_{hys}	–	25	–	°C



Component	Value	Manufacturer
C1, C2	10 μF, 6.3 V	TDK, C2012X5R0J106M (0805 size)
L	10 μH	TDK, LLF4017-100 (I_{out} = 300 mA) Coilcraft, LPO4812-103MX (I_{out} = 300 mA) Coilcraft, 0805PS-103M (I_{out} = 150 mA) TDK, NLC252018T-100 (I_{out} = 100 mA)

Figure 2. Typical Circuit with the Internal Schematic

DETAILED OPERATING DESCRIPTION

The Buck regulator is a synchronous rectifier PWM regulator with integrated MOSFETs. This regulator has an LDO function for low power modes to conserve power and lower ripple voltage associated with PFM mode. The NCP1501 does not contain an internal oscillator for the switching mode. The Dual PWM/LDO mode is an exclusive Patent Pending circuit.

The PWM clock is generated via an external clock signal on the Synchronization pin. The operating frequency range for the PWM is 500 kHz to 1000 kHz. The output current of the PWM is typically 100 mA with a guarantee of over 300 mA for the 2.7 to 5.2 input voltage range.

If a synchronization pulse is not present, the NCP1501 changes into the LDO mode. The LDO function assures the user of an extremely low output ripple voltage and greatly reduced quiescent current when the users system is in a sleep mode. Internally to the NCP1501, the Synchronization pin has a pull down resistor to force the part into LDO mode when a clock signal is not present. To place the NCP1501 in LDO mode, the user must set the Synchronization pin low. The LDO mode guarantees an output in excess of 50 mA.

Pins CB0 and CB1 control the output voltage selection. The four voltages are 1.05 V, 1.35 V, 1.57 V, 1.8 V. CB0 contains a pull down resistor and CB1 contains a pull up resistor internal to the NCP1501. The resistors force the output of the converter to 1.35 V if the pins are floating connections to the external circuit.

The Shutdown Pin enables the operation of the device. The Shutdown Pin has an internal pull down resistor to force the NCP1501 into the off mode if this pin is floating due to the external circuit. During Startup, the NCP1501 has a soft start function to limit fast dV/dt and eliminate overshoot on the output.

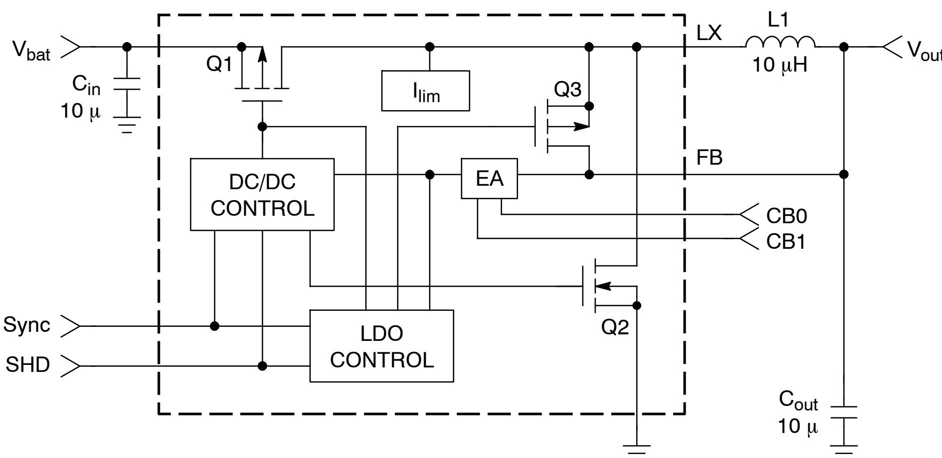


Figure 3. Block Diagram and Circuit Schematic of the NCP1501

The external components required are an input and an output 10 0 µF ceramic capacitor and a 10 µH inductor.

PWM Mode

During normal operation, a synchronization pulse acts as the clock for the DC/DC controller. The rising edge of the clock pulls the gate of Q1 low allowing the inductor to charge. When the current through Q1 reaches either the current limit or feedback voltage reaches its limit, Q1 will turn off and Q2 will turn on. Q2 replaces the free wheeling diode typically associated with Buck Converters. Q2 will turn off when either a rising edge sync pulse is present or all the stored energy is depleted from the inductor. Q3 remains off during this mode.

The output voltage accuracy in the PWM mode is well within 3% of the nominal set value. An over voltage protection circuit is present in the PWM mode to limit the positive voltage spike due to fast load transient conditions. The PWM also has the ability to go to 100% duty cycle for transient conditions and low input to output voltage differentials.

In PWM mode, each switching cycle has a guaranteed on-time of 100 ns. The NCP1501 has two protection circuits that can eliminate the cycle. When tripped, the over voltage protection or the thermal shutdown overrides the gate drive of the high side MOSFET.

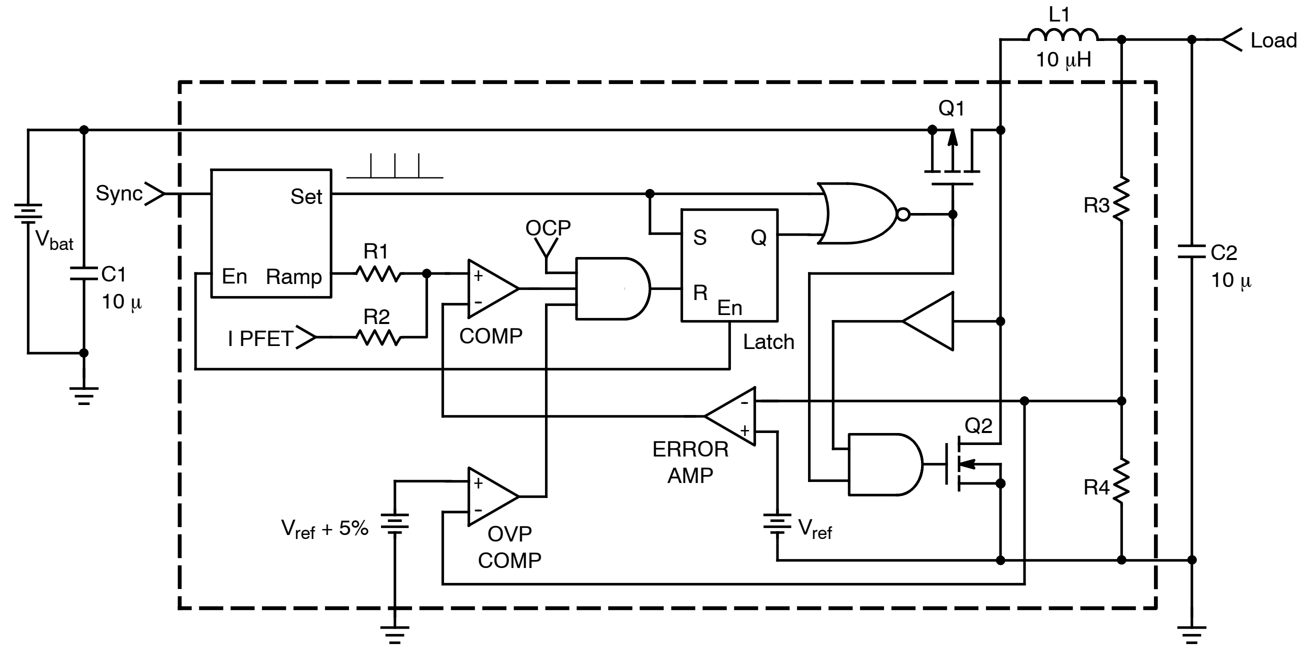


Figure 4. PWM Circuit Schematic

LDO Mode

When the synchronization pulse is not present, the NCP1501 operates as an LDO. The DC/DC Control Circuitry will relinquish control of Q1 and turn off Q2. The LDO Control Circuitry will turn on Q3 as a bypass circuit to the inductor. Q1 is the controlling pass device of the LDO that regulates the input to output voltage dropout. The LDO can source an output current in excess of 50 mA.

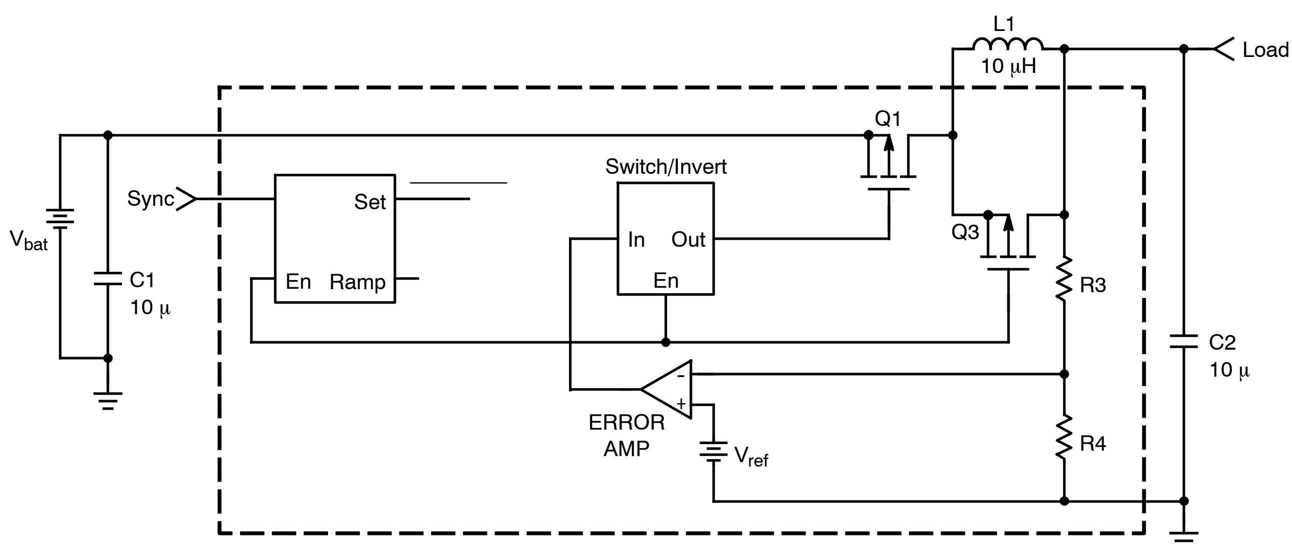


Figure 5. LDO Circuit Schematic

Voltage Output Selection

The output voltage selection is accomplished via two external pins: CB0 and CB1. If CB0 and CB1 pins are left floating by the external circuit, the output voltage will default to 1.35 V. The corresponding voltages are as follows.

CB0	CB1	NCP1501 V_{out} (V)
0	0	1.05
0	1	1.35
1	1	1.57
1	0	1.80

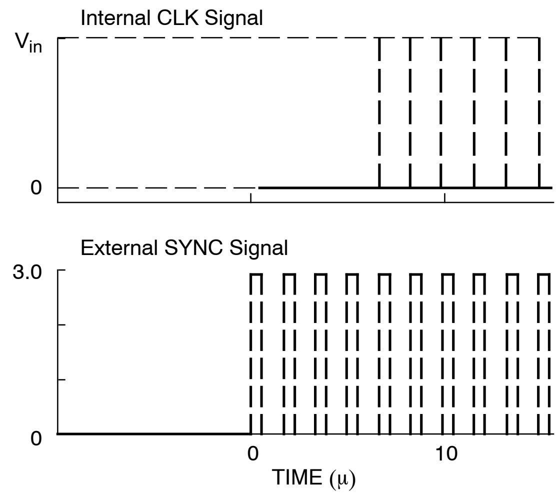


Figure 6. Transition Waveforms from LDO to PWM Mode

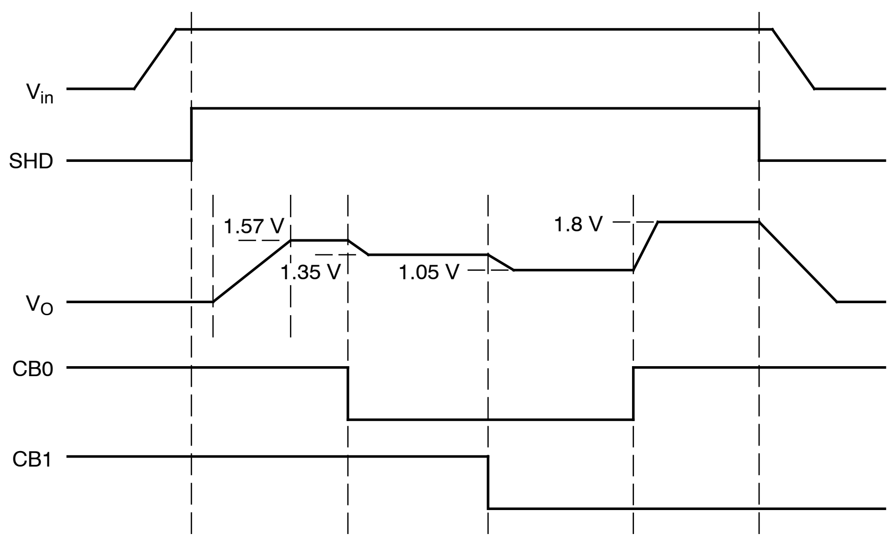


Figure 7. Power Up and Power Down Sequence

Thermal Shutdown

Internal Thermal Shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated, typically at 160°C, the PWM latch is reset and the linear regulator control circuitry is disabled. The thermal shutdown circuit is designed with 25°C of hysteresis. This means that the PWM latch and the regulator control circuitry cannot be re-enabled until the die temperature drops by this amount. This feature is provided to prevent catastrophic failures from accidental device overheating. It is not intended as a substitute for proper heatsinking. The NCP1501 is contained in the Micro-8 package.

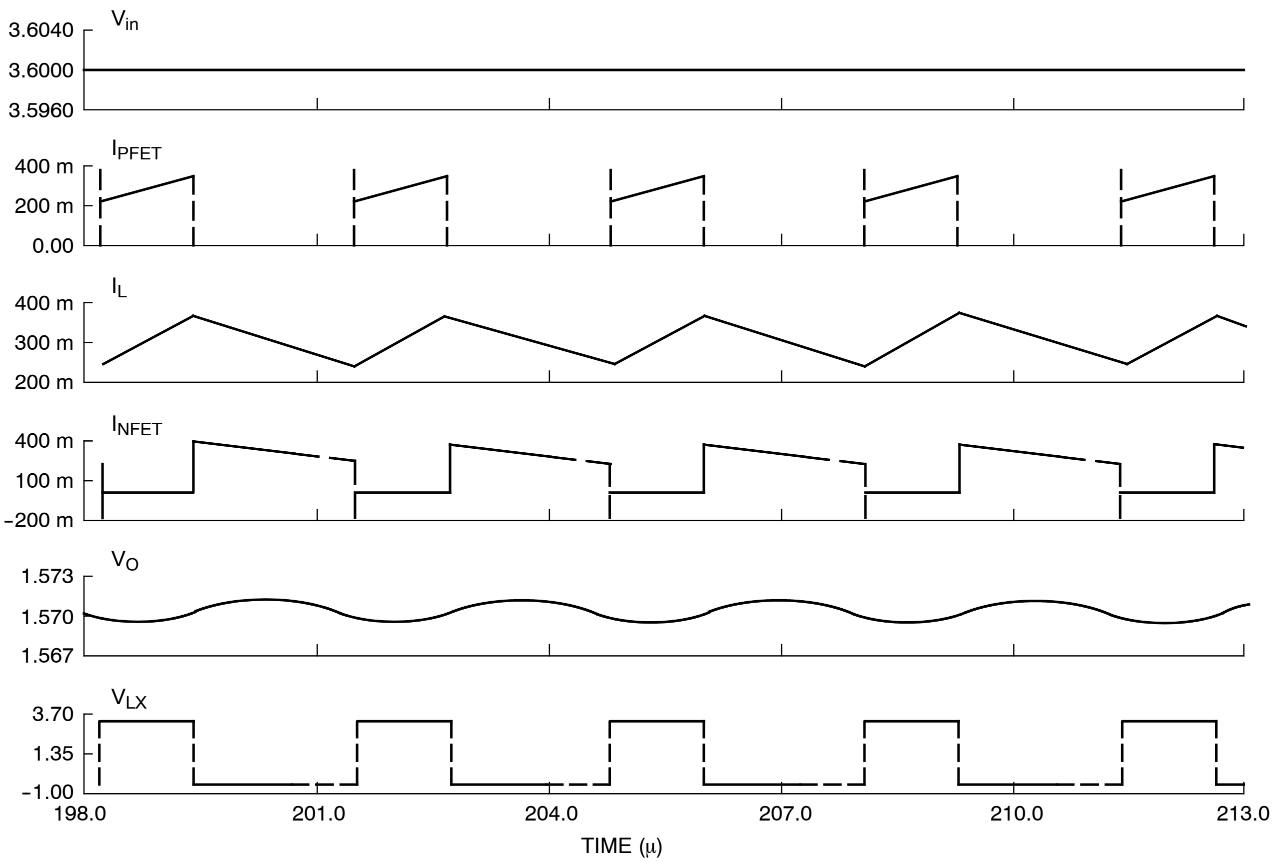


Figure 8. Waveforms During Normal Operation

APPLICATIONS INFORMATION

NCP1501 is a dual mode PWM or LDO step down converter. This dual mode takes advantage of the best of each mode. There are three required external components: an input and output capacitor and an inductor.

The PWM mode allows high efficiency for larger loads. A typical efficiency for an input of 3.6 V and an output of 1.8 V and 100 mA is over 90%. Low R_{DSon} and synchronous rectification contained within the device contributes to the very high efficiency. As with other synchronous rectification devices, the NCP1501 does not require an external diode to supplement the NFET during switching on or off. A synchronization pin allows the user to define the frequency noise spikes of the PWM. The duty cycle of the synchronization signal must be within the range of 30% to 70%. The rising edge of the signal from the synchronization pin acts as the oscillator signal to set the latch and reset the ramp compensation signal. An Over Voltage Protection circuit ensures the output will respond properly to fast transients from large to small loads. The NCP1501 allows the PWM mode to enter a 100% duty cycle for fast load transient conditions and low input to output voltage differentials.

The LDO mode is effective during low load conditions by lowering the quiescent current and reducing the output ripple voltage associated with PWM converters entering PFM mode. NCP1501 enters the LDO mode when a synchronization signal is not present. It is recommended to pull the synchronization signal low for LDO mode.

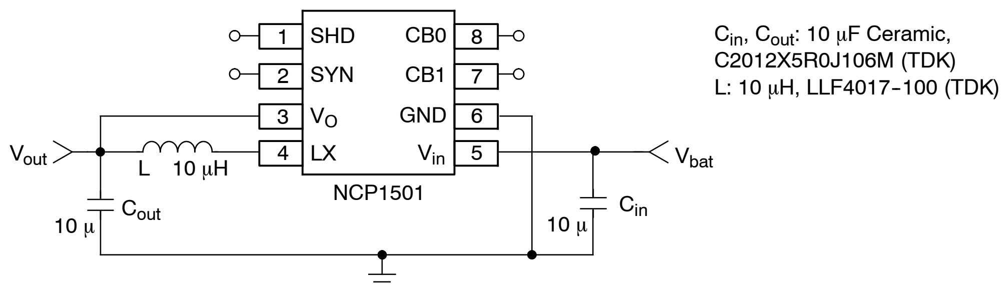


Figure 9. Typical Operating Schematic

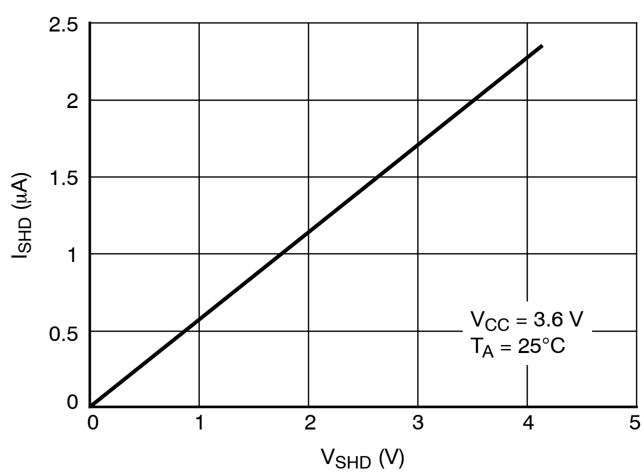


Figure 10. Input Current versus Voltage for the Shutdown Pin

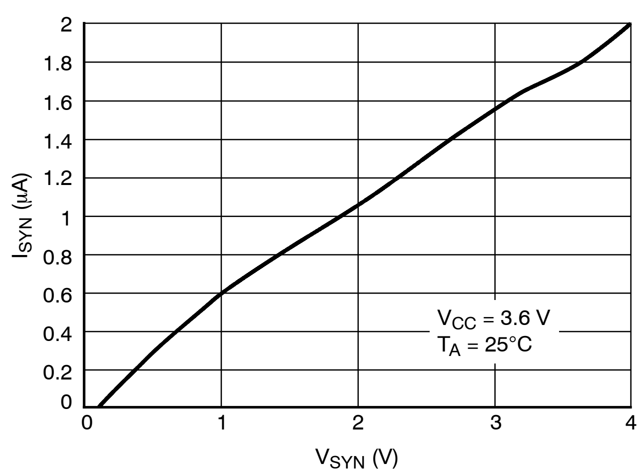


Figure 11. Input Current versus Voltage for the Synchronization Pin

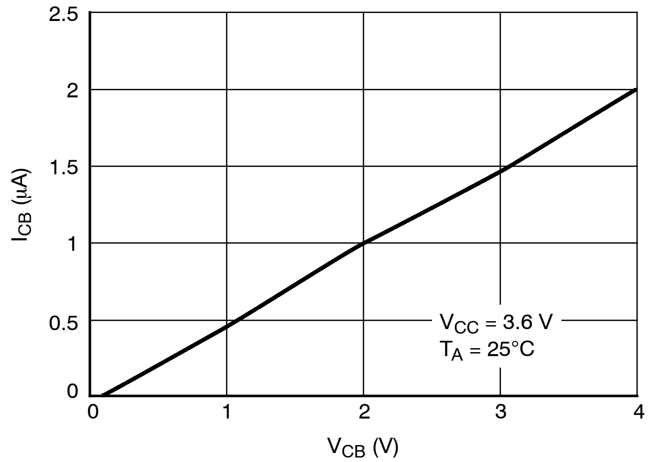


Figure 12. Input Current versus Voltage for the CB Pins

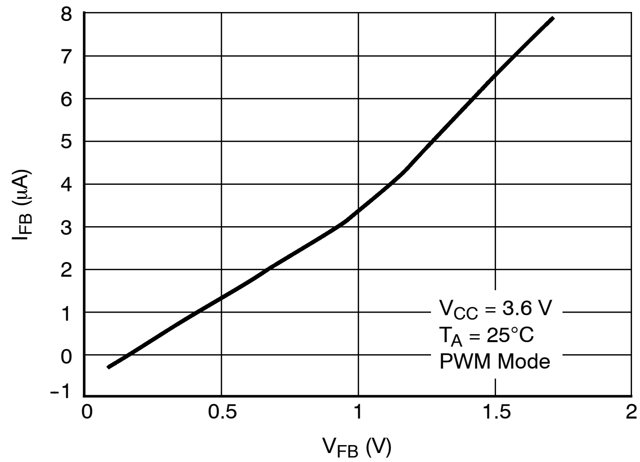


Figure 13. Input Current versus Voltage for the Feedback Pin

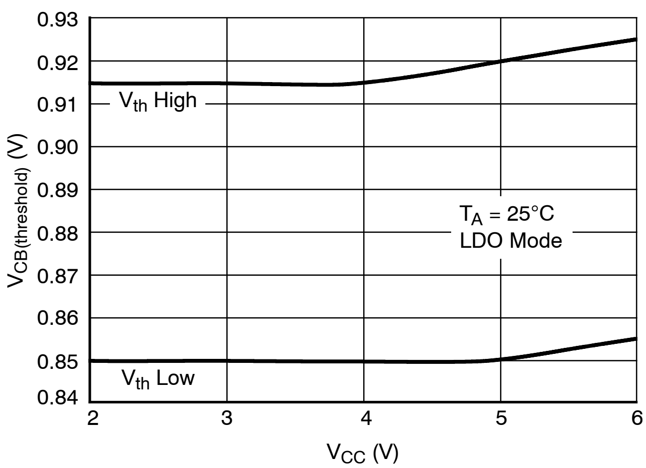


Figure 14. V_{CC} Input Voltage versus CB Threshold

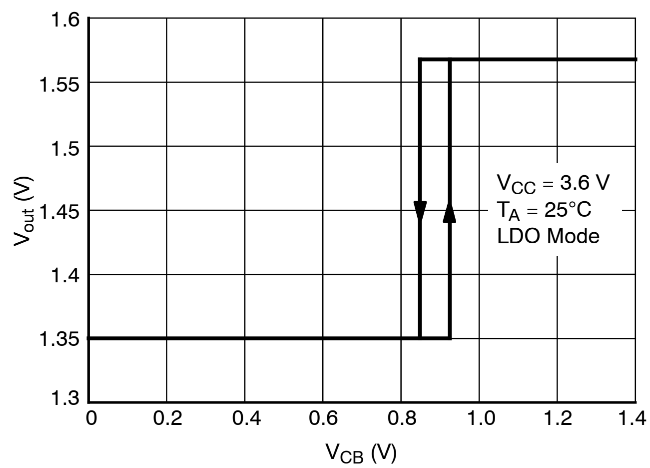


Figure 15. Transition Level of CB Pins

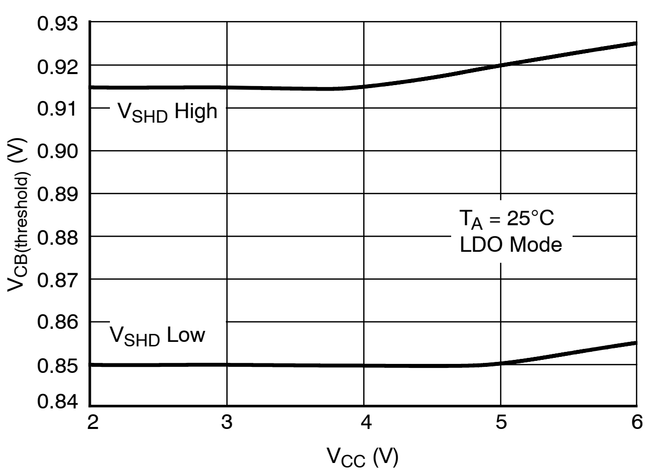


Figure 16. Input Voltage versus Shutdown Voltage

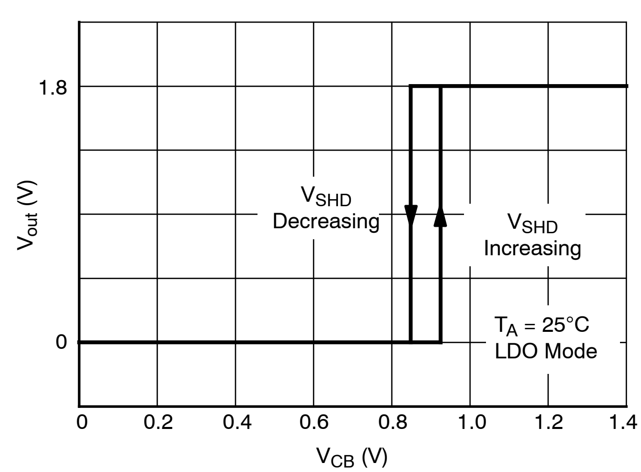


Figure 17. Output Voltage versus Shutdown Pin Voltage

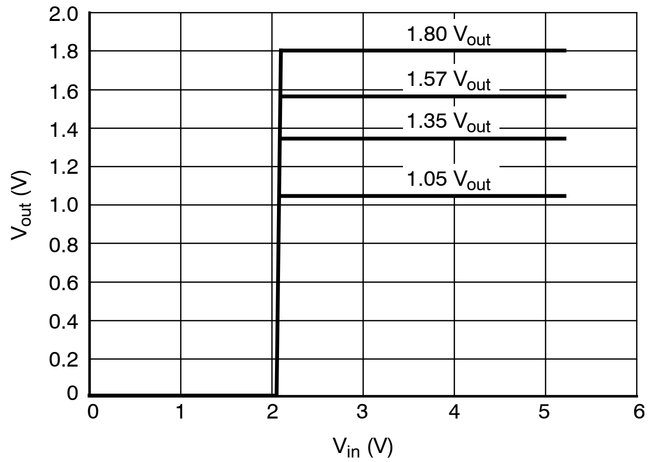


Figure 18. Output Voltage versus PWM Input Voltage

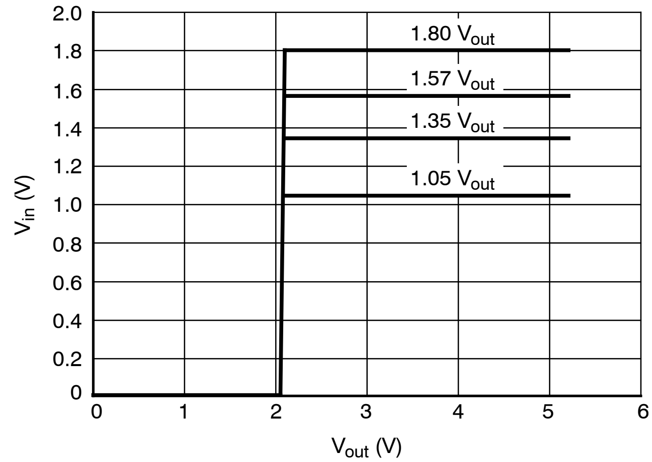


Figure 19. Input Voltage versus Output Voltage

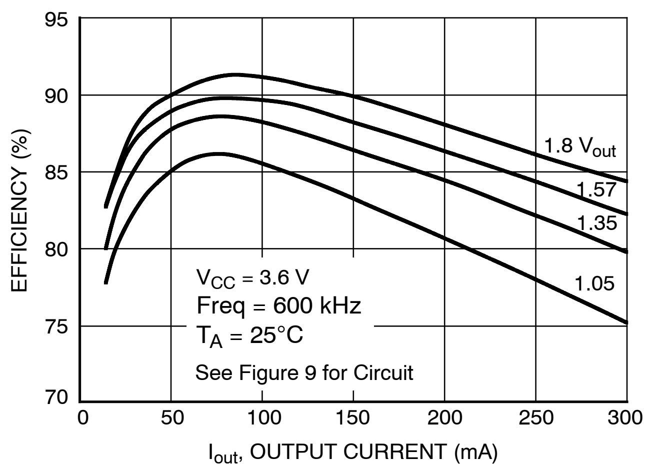


Figure 20. Efficiency versus Output Current

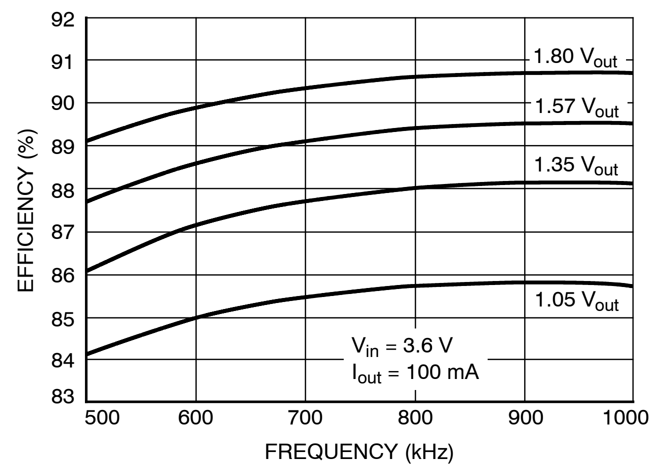


Figure 21. Efficiency versus Frequency

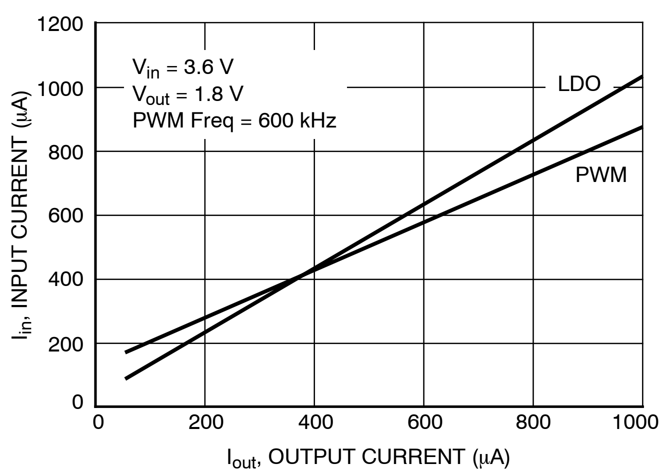


Figure 22. Input Current versus Output Current Comparison for PWM and LDO Mode

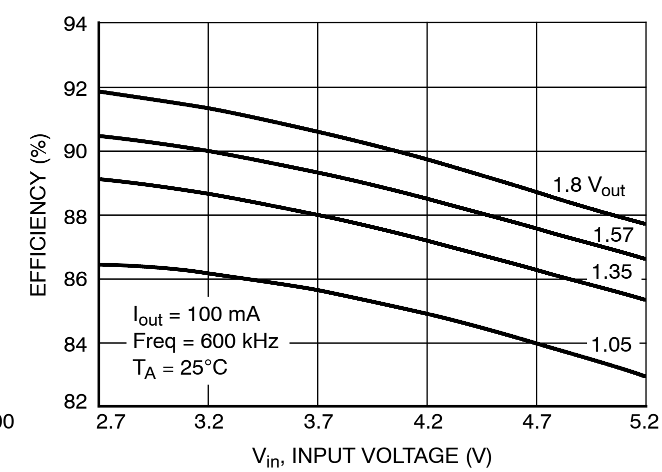


Figure 23. Efficiency versus Input Voltage

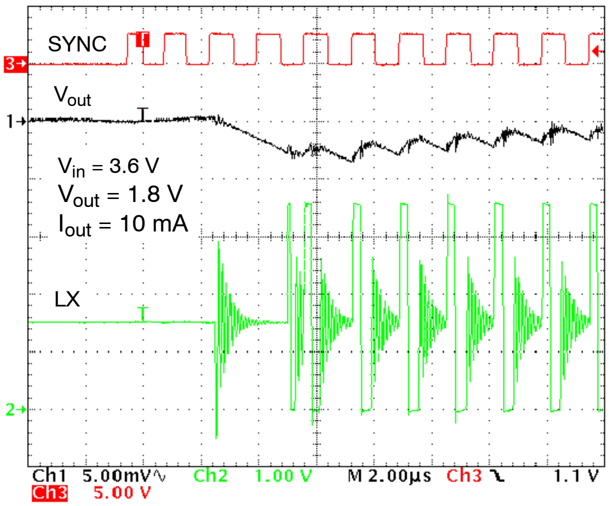


Figure 24. Transition from LDO to PWM Mode

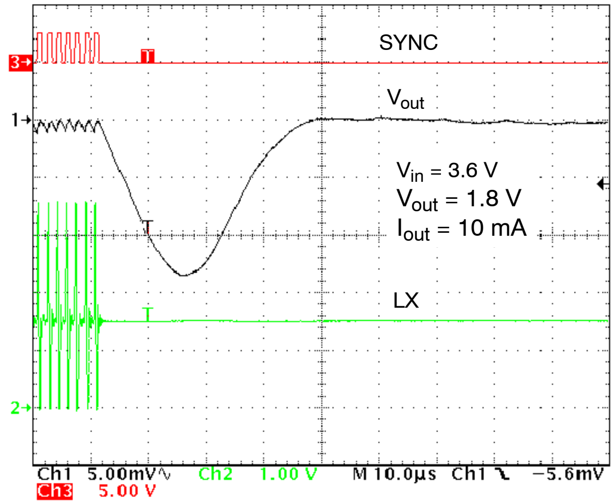


Figure 25. Transition from PWM to LDO Mode

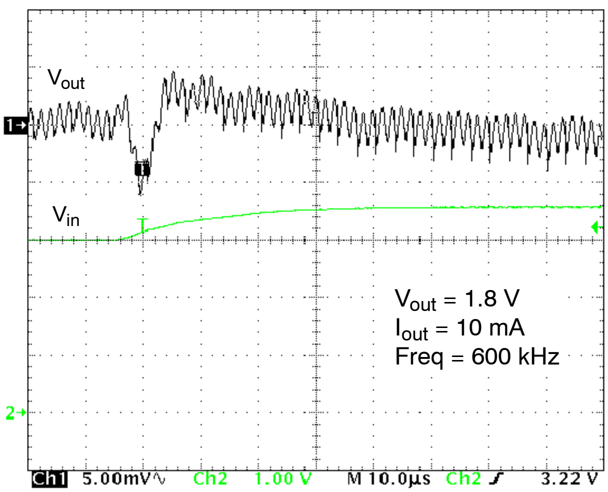


Figure 26. Line Transient from 3.0 to 3.6 V

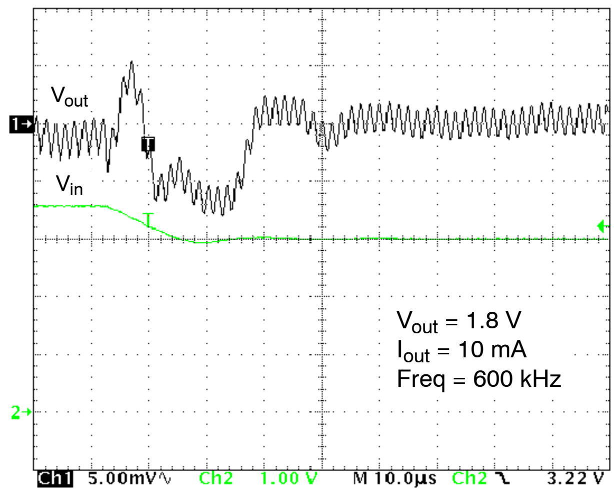


Figure 27. Line Transient from 3.6 to 3.0 V

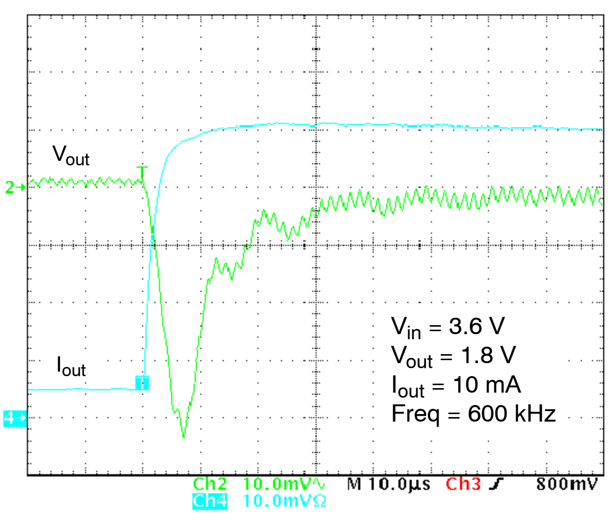


Figure 28. Load Transient from 10 to 100 mA

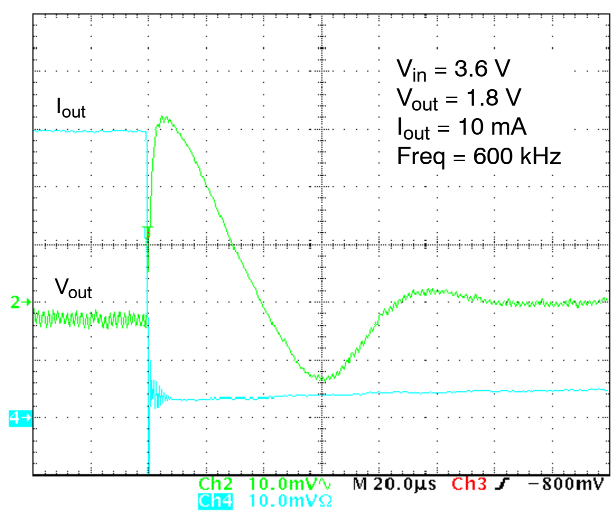


Figure 29. Load Transient from 100 to 10 mA

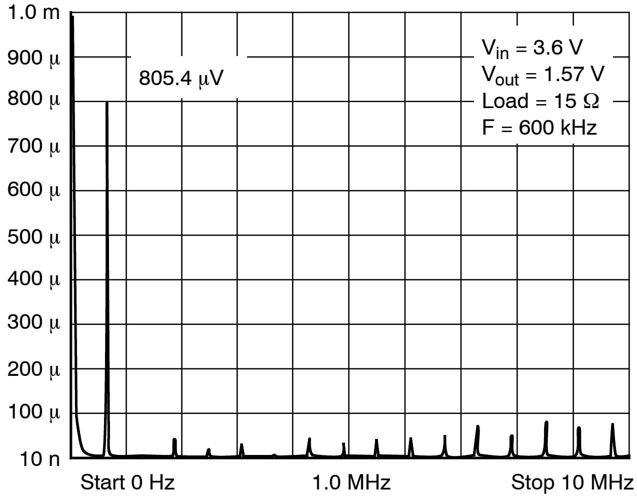


Figure 30. V_{rms} versus Frequency

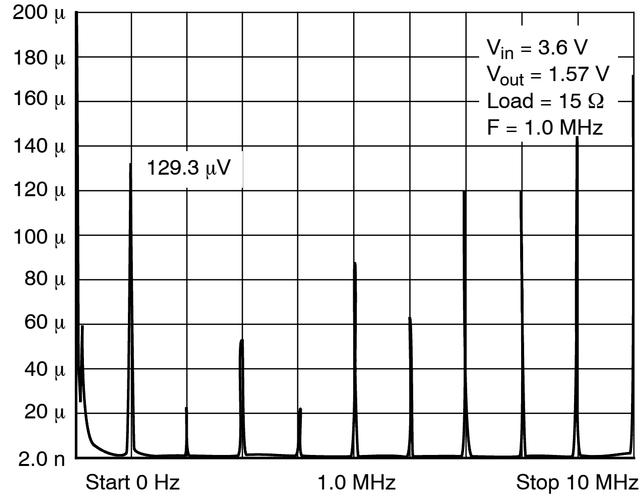


Figure 31. V_{rms} versus Frequency

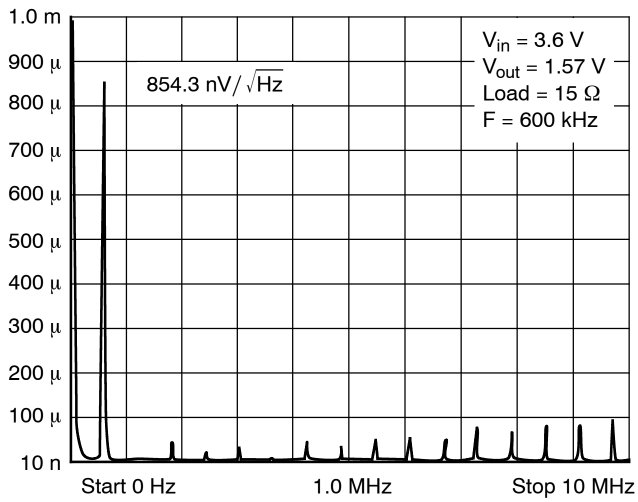


Figure 32. Noise versus Frequency

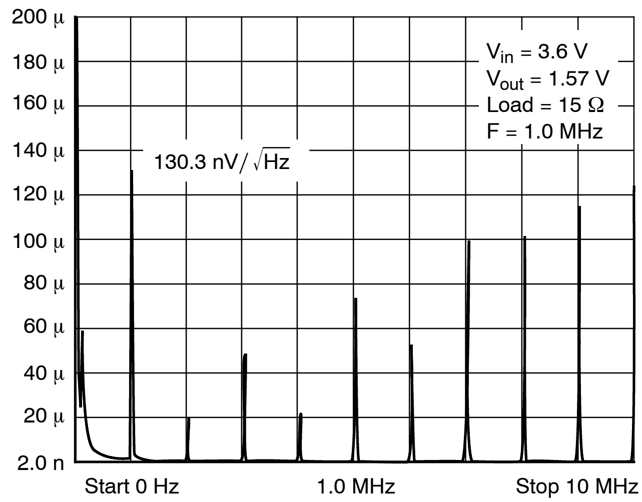
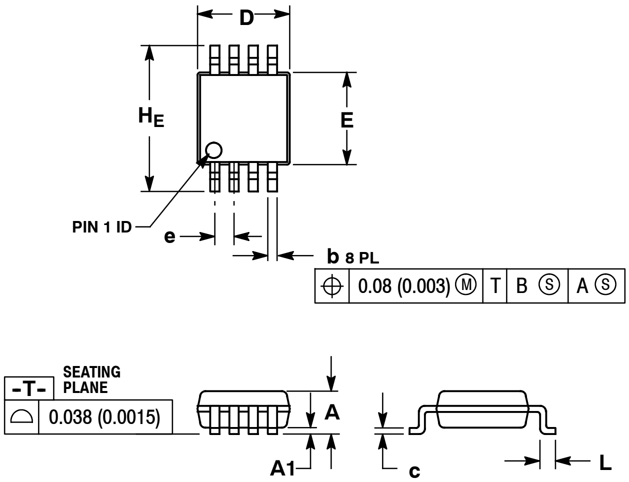


Figure 33. V_{RMS} versus Frequency

PACKAGE DIMENSIONS

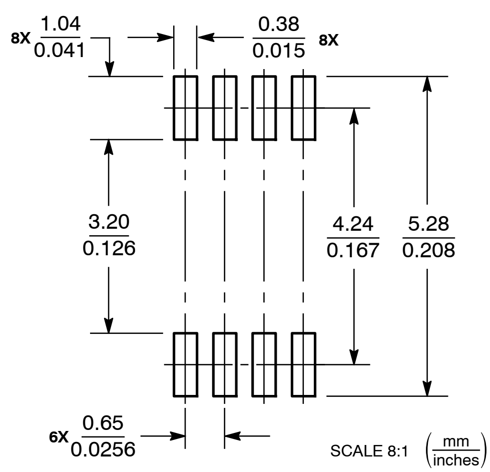
Micro8™
CASE 846A-02
ISSUE H



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. 846A-01 OBSOLETE, NEW STANDARD 846A-02.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	--	--	1.10	--	--	0.043
A1	0.05	0.08	0.15	0.002	0.003	0.006
b	0.25	0.33	0.40	0.010	0.013	0.016
c	0.13	0.18	0.23	0.005	0.007	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
E	2.90	3.00	3.10	0.114	0.118	0.122
e	0.65 BSC			0.026 BSC		
L	0.40	0.55	0.70	0.016	0.021	0.028
HE	4.75	4.90	5.05	0.187	0.193	0.199

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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