

NC7S14 TinyLogic™ HS Inverter with Schmitt Trigger Input

General Description

The NC7S14 is a single high performance CMOS Inverter with Schmitt Trigger input. The circuit design provides hysteresis between the positive-going and negative going input thresholds thereby improving noise margins.

Advanced Silicon Gate CMOS fabrication assures high speed and low power circuit operation over a broad V_{CC} range. ESD protection diodes inherently guard both input and output with respect to the V_{CC} and GND rails.

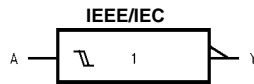
Features

- Space saving SOT23 or SC70 5-lead package
- Schmitt input hysteresis: $> 1V$ typ
- High speed: t_{PD} 4.5 ns typ
- Low quiescent power: $I_{CC} < 1 \mu A$
- Balanced output drive: 2 mA I_{OL} , -2 mA I_{OH}
- Broad V_{CC} operating range: 2V – 6V
- Balanced propagation delays
- Specified for 3V operation

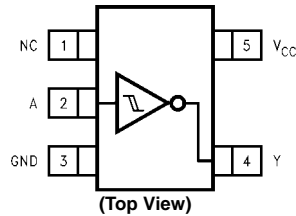
Ordering Code:

Order Number	Package Number	Package Top Mark	Package Description	Supplied As
NC7S14M5	MA05B	7S14	5-Lead, SOT23, JEDEC MO-178, 1.6mm	250 Units on Tape and Reel
NC7S14M5X	MA05B	7S14	5-Lead, SOT23, JEDEC MO-178, 1.6mm	3k Units on Tape and Reel
NC7S14P5	MAA05A	S14	5-Lead SC70, EIAJ SC-88a, 1.25mm Wide	250 Units on Tape and Reel
NC7S14P5X	MAA05A	S14	5-Lead SC70, EIAJ SC-88a, 1.25mm Wide	3k Units on Tape and Reel

Logic Symbol



Connection Diagram



Pin Descriptions

Pin Names	Description
A	Input
Y	Output
NC	No Connect

Function Table

$Y = \bar{A}$

Input	Output
A	Y
L	H
H	L

H = HIGH Logic Level
L = LOW Logic Level

TinyLogic™ is a trademark of Fairchild Semiconductor Corporation.

Absolute Maximum Ratings (Note 1)		Power Dissipation (P_D) @ +85°C	
Supply Voltage (V_{CC})	-0.5V to +7.0V	SOT23-5	200 mW
DC Input Diode Current (I_{IK})		SC70-5	150 mW
@ $V_{IN} \leq -0.5V$	-20 mA	Recommended Operating Conditions (Note 2)	
@ $V_{IN} \geq V_{CC} + 0.5V$	+20 mA	Supply Voltage (V_{CC})	2.0V to 6.0V
DC Input Voltage (V_{IN})	-0.5V to $V_{CC} + 0.5V$	Input Voltage (V_{IN})	0V to V_{CC}
DC Output Diode Current (I_{OK})		Output Voltage (V_{OUT})	0V to V_{CC}
@ $V_{OUT} < -0.5V$	-20 mA	Operating Temperature (T_A)	-40°C to +85°C
@ $V_{OUT} > V_{CC} + 0.5V$	+20 mA	Thermal Resistance (θ_{JA})	
DC Output Voltage (V_{OUT})	-0.5V to $V_{CC} + 0.5V$	SOT23-5	300°C/W
DC Output Source or Sink Current (I_{OUT})	± 12.5 mA	SC70-5	425°C/W
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	± 25 mA	Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of circuits outside the databook specifications.	
Storage Temperature (T_{STG})	-65°C to +150°C	Note 2: Unused inputs must be held HIGH or LOW. They may not float.	
Junction Temperature (T_J)	150°C		
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C		

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = +25^\circ\text{C}$			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units	Conditions		
			Min	Typ	Max	Min	Max				
V_P	Positive Threshold Voltage	2.0	1.0	1.29	1.5	1.0	1.6	V			
		3.0	1.5	1.90	2.2	1.5	2.2				
		4.5	2.3	2.73	3.15	2.3	3.15				
		6.0	3.0	3.56	4.2	3.0	4.2				
V_N	Negative Threshold Voltage	2.0	0.3	0.70	0.9	0.3	0.9	V			
		3.0	0.6	1.05	1.35	0.6	1.35				
		4.5	1.13	1.66	2.0	1.13	2.0				
		6.0	1.5	2.24	2.6	1.5	2.6				
V_H	Hysteresis Voltage	2.0	0.3	0.59	1.0	0.3	1.0	V			
		3.0	0.4	0.85	1.3	0.4	1.3				
		4.5	0.6	1.08	1.4	0.6	1.4				
		6.0	0.8	1.31	1.7	0.8	1.7				
V_{OH}	HIGH Level Output Voltage	2.0	1.90	2.0		1.90		V	$I_{OH} = -20 \mu\text{A}$ $V_{IN} = V_{IL}$		
		3.0	2.90	3.0		2.90					
		4.5	4.40	4.5		4.40					
		6.0	5.90	6.0		5.90					
				3.0	2.68	2.87		2.63	V	$V_{IN} = V_{IL}$ $I_{OH} = -1.3 \text{ mA}$ $I_{OH} = -2 \text{ mA}$ $I_{OH} = -2.6 \text{ mA}$	
				4.5	4.18	4.37		4.13			
				6.0	5.68	5.86		5.63			
V_{OL}	LOW Level Output Voltage	2.0		0.0	0.10		0.10	V	$I_{OH} = 20 \mu\text{A}$ $V_{IN} = V_{IH}$		
		3.0		0.0	0.10		0.10				
		4.5		0.0	0.10		0.10				
		6.0		0.0	0.10		0.10				
				3.0		0.1	0.26		0.33	V	$V_{IN} = V_{IH}$ $I_{OL} = 1.3 \text{ mA}$ $I_{OL} = 2 \text{ mA}$ $I_{OL} = 2.6 \text{ mA}$
				4.5		0.1	0.26		0.33		
				6.0		0.1	0.26		0.33		
I_{IN}	Input Leakage Current	6.0			± 0.1		± 1.0	μA	$V_{IN} = V_{CC}, \text{ GND}$		
I_{CC}	Quiescent Supply Current	6.0			1.0		10.0	μA	$V_{IN} = V_{CC}, \text{ GND}$		

AC Electrical Characteristics

Symbol	Parameter	V _{CC} (V)	T _A = +25°C			T _A = -40°C to +85°C		Units	Conditions	Fig. No.
			Min	Typ	Max	Min	Max			
t _{PLH}	Propagation Delay	5.0		4.5	21			ns	C _L = 15 pF	Figure 1
t _{PHL}		2.0		20	100		125		C _L = 50 pF	Figure 3
		3.0		12	27		35	ns		
		4.5		8.5	20		25			
		6.0		7.5	17		21			
t _{TLH}	Output Transition Time	5.0		3	8			ns	C _L = 15 pF	Figure 1
t _{THL}		2.0		25	125		145		C _L = 50 pF	Figure 3
		3.0		16	35		45	ns		
		4.5		11	25		30			
		6.0		9	21		24			
C _{IN}	Input Capacitance	Open		2	10		10	pF		
C _{PD}	Power Dissipation Capacitance	5.0		7				pF	(Note 3)	Figure 2

Note 3: C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. (See Figure 2.) C_{PD} is related to I_{CCD} dynamic operating current by the expression:
 $I_{CCD} = (C_{PD})(V_{CC})(f_{IN}) + (I_{CCstatic})$.

AC Loading and Waveforms

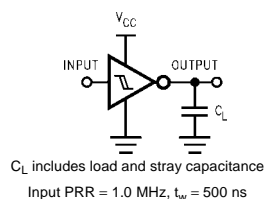


FIGURE 1. AC Test Circuit

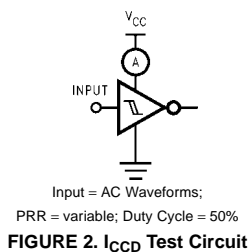


FIGURE 2. I_{CCD} Test Circuit

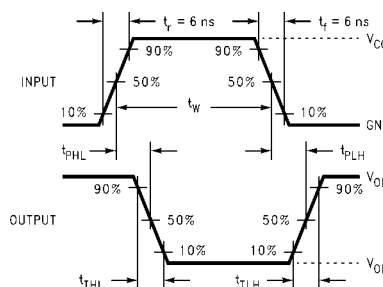


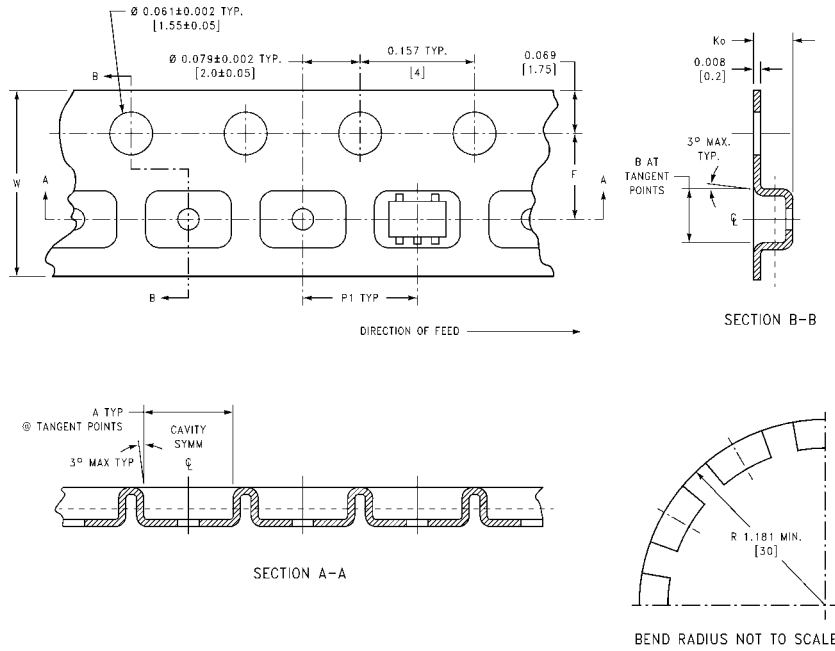
FIGURE 3. AC Waveforms

Tape and Reel Specification

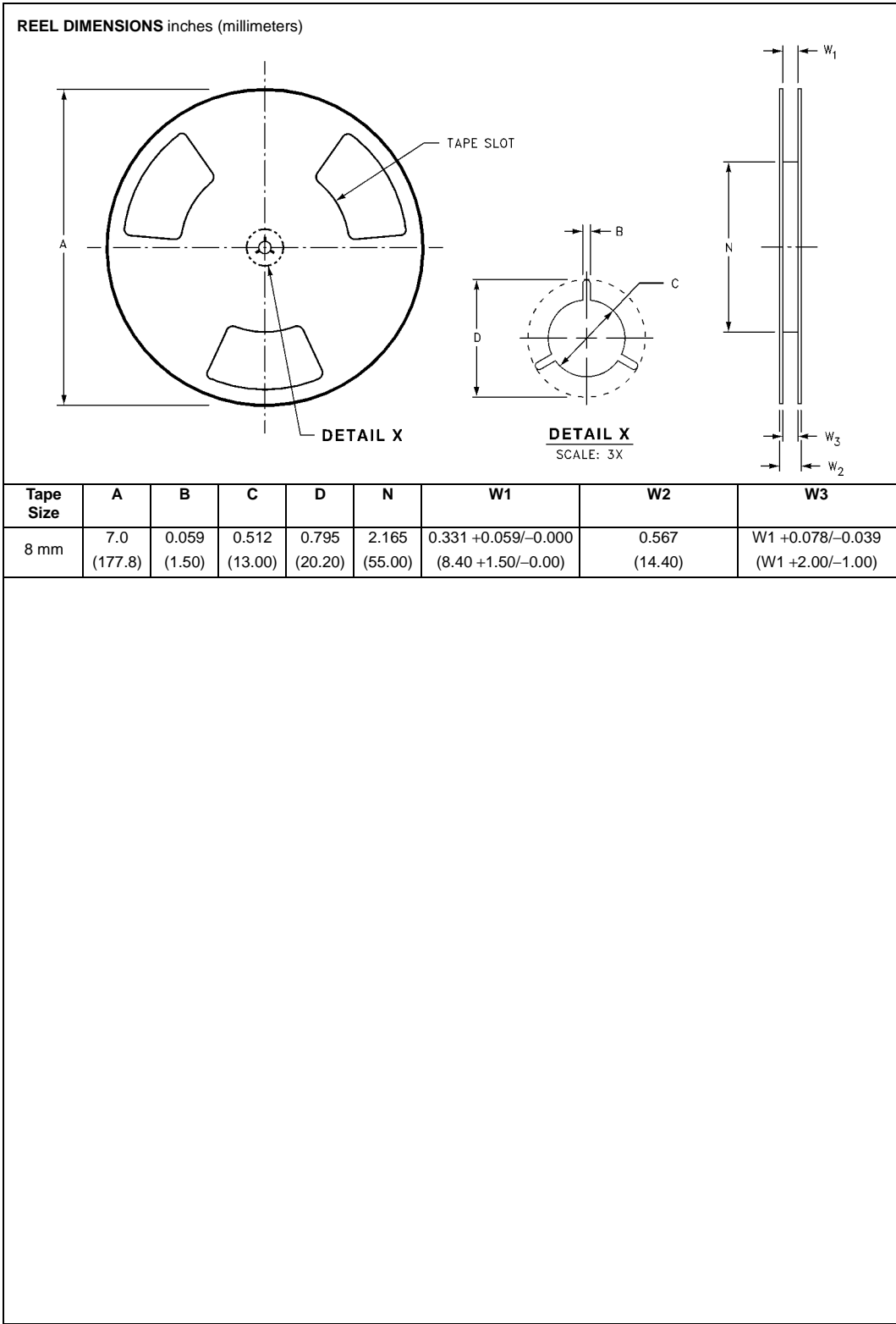
TAPE FORMAT

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
M5, P5	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	250	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed
M5X, P5X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

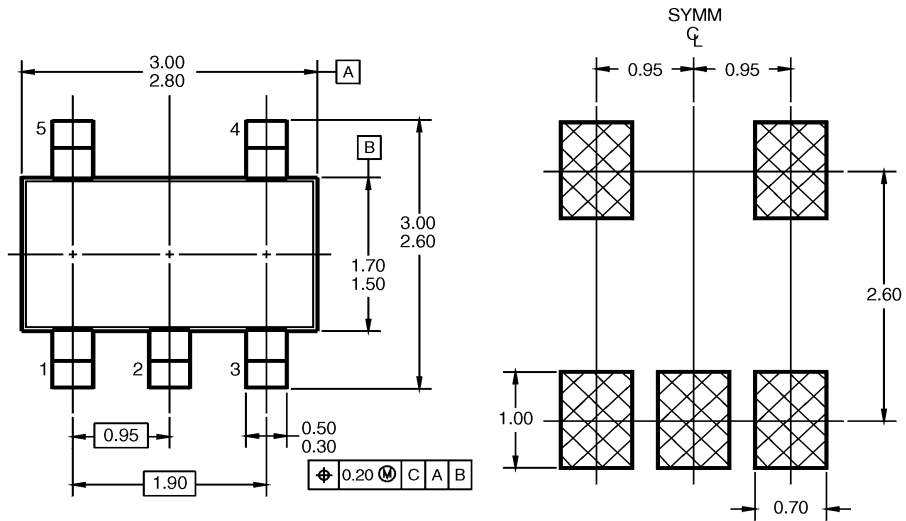
TAPE DIMENSIONS inches (millimeters)



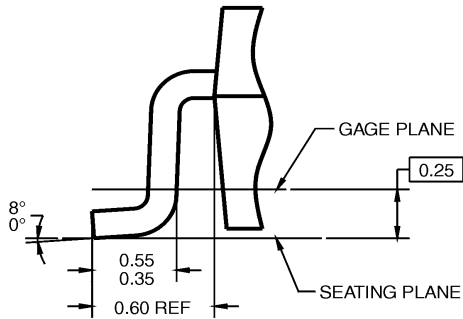
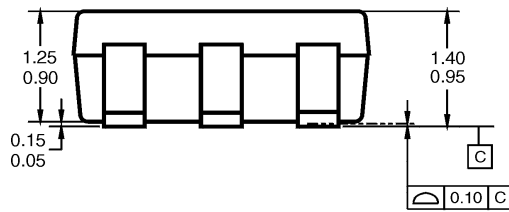
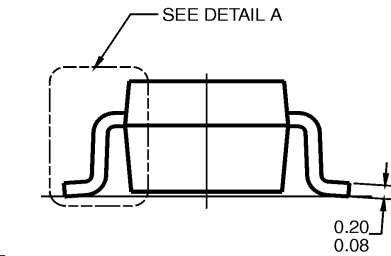
Package	Tape Size	DIM A	DIM B	DIM F	DIM K ₀	DIM P1	DIM W
SC70-5	8 mm	0.093 (2.35)	0.096 (2.45)	0.138 ± 0.004 (3.5 ± 0.10)	0.053 ± 0.004 (1.35 ± 0.10)	0.157 (4)	0.315 ± 0.004 (8 ± 0.1)
SOT23-5	8 mm	0.130 (3.3)	0.130 (3.3)	0.138 ± 0.002 (3.5 ± 0.05)	0.055 ± 0.004 (1.4 ± 0.11)	0.157 (4)	0.315 ± 0.012 (8 ± 0.3)



Physical Dimensions inches (millimeters) unless otherwise noted



LAND PATTERN RECOMMENDATION



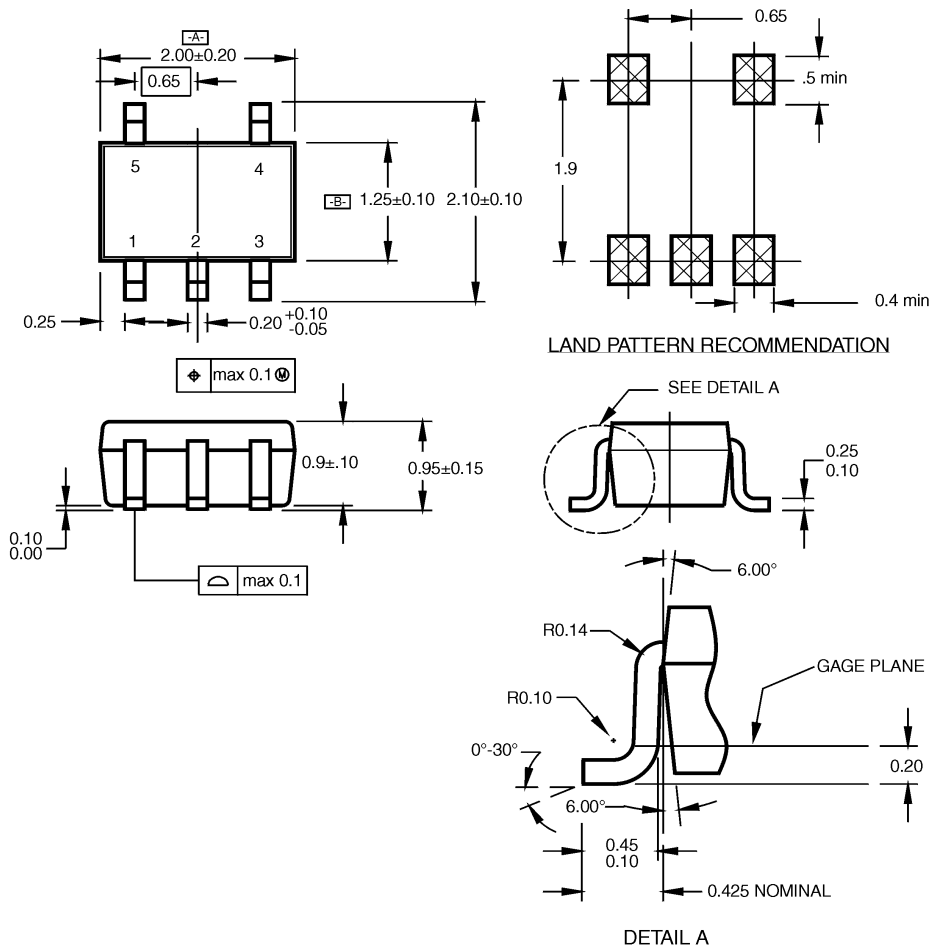
- NOTES: UNLESS OTHERWISE SPECIFIED
- A) THIS PACKAGE CONFORMS TO JEDEC MO-178, ISSUE B, VARIATION AA, DATED JANUARY 1999.
 - B) ALL DIMENSIONS ARE IN MILLIMETERS.

MA05BRevC

DETAIL A

**5-Lead SOT23, JEDEC MO-178, 1.6mm
Package Number MA05B**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**5-Lead SC70, EIAJ SC-88a, 1.25mm Wide
Package Number MAA05A**

NOTES:

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com