# NB3L83948C

# 2.5 V / 3.3 V Differential and LVTTL/LVCMOS 2:1 MUX to 1:12 LVCMOS Fanout

ON Semiconductor®

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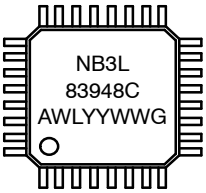
LQFP−32
FA SUFFIX
CASE 873A

**MARKING DIAGRAMS***




| | |
|---|---|
| A | = Assembly Location |
| WL | = Wafer Lot |
| YY | = Year |
| WW | = Work Week |
| G | = Pb−Free Package |

(*Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

### Description

The NB3L83948C is a pure 2.5 V / 3.3 V ($V_{DD}$ = $V_{DDO}$) or mixed mode 3.3 V Core ($V_{DD}$) / 2.5 V Output ($V_{DDO}$) clock distribution buffer with the capability to select either a differential LVPECL / LVDS / LVHSTL / SSTL / HCSL or single ended LVCMOS / LVTTL compatible input clock, such as a Primary or a Test Clock. All other control inputs (CLK_SEL, CLK_EN, and OE) are LVTTL/LVCMOS level compatible.

The NB3L83948C provides an enable input, CLK_EN pin, which synchronously enables or disables the clock outputs while in the LOW state. Since this input is internally synchronized to the input clock, changing only when the input is LOW, potential output glitching or runt pulse generation is eliminated.

The 12 LVCMOS output pins drive 50 Ω series or parallel terminated transmission lines. The outputs can also be disabled to a high impedance (tri−stated) via the OE input, or enabled when High.

Fit, Form, and Function compatible with ICS83948I−147, ICS83948I−01, CY29948AXI, and MPC9448/9448L

### Features

- 2.5 V / 3.3V ($V_{DD}$ = $V_{DDO}$) or 3.3 V $V_{DD}$ / 2.5 V $V_{DDO}$ Operation:
  2.5 ±5%, 2.375 to 2.625 V
  3.3 ±5%; 3.135 to 3.465 V
- 350 MHz Clock Support
- Accepts LVPECL, LVDS, LVHSTL, SSTL, HCSL, or LVCMOS Clock Inputs
- LVCMOS Compatible Control Inputs
- 12 LVCMOS Clock Outputs
- Synchronous Clock Select
- Output Enable to High Z State Control
- 100 ps Max. Skew Between Outputs
- Industrial Temp. Range −40°C to +85°C
- 32−pin LQFP Package
- These are Pb−Free Devices

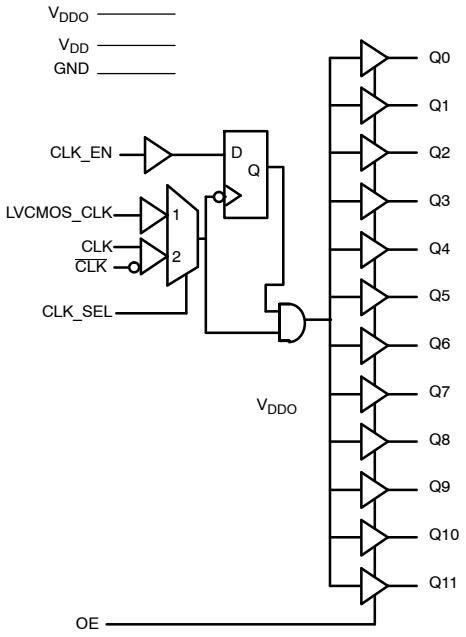



**Figure 1. Simplified Logic Diagram**

### ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

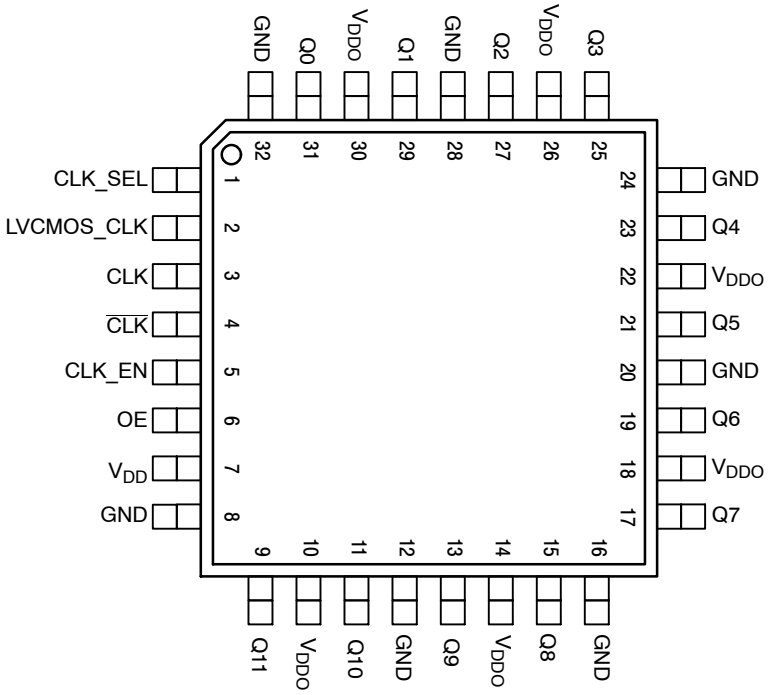



**Figure 2. Pinout Configuration** (Top View)

**Table 1. PIN DESCRIPTION**

| Pin | Name | I/O | Open Default | Description |
|---|---|---|---|---|
| 1 | CLK_SEL | LVTTL/LVCMOS Input | Pullup | Clock Select Input. When LOW, the CLK/$\overline{CLK}$ differential inputs are selected. When HIGH, LVCMOS_CLK is selected. |
| 2 | LVCMOS_CLK | LVTTL/LVCMOS Input | Pullup | Single ended Test Clock Input |
| 3 | CLK | LVPECL, LVDS, LVHSTL, SSTL, HCSL, or LVCMOS | Pullup | True Clock Input (internal) |
| 4 | $\overline{CLK}$ | LVPECL, LVDS, LVHSTL, SSTL, HCSL, or LVCMOS | Pulldown | Invert Clock Input |
| 5 | CLK_EN | LVTTL/LVCMOS Input | Pullup | Synchronous Clock Enable Input. When HIGH, outputs are enabled. When LOW, outputs are disabled (LOW). |
| 6 | OE | LVTTL/LVCMOS Input | Pullup | Output High Z State control. When HIGH, the outputs are active and enabled. When LOW, the outputs are high impedance disabled. |
| 7 | $V_{DD}$ | POWER | | $V_{DD}$ Positive Supply pin for core logic. All $V_{DD}$, $V_{DDO}$, and GND pins must be externally connected to a power supply to guarantee proper operation. Bypass with 0.01 μF cap to GND. |
| 8, 12, 16, 20, 24, 28, 32 | GND | GND | | GND Supply Ground. All $V_{DD}$, $V_{DDO}$ and GND pins must be externally connected to power supply to guarantee proper operation. |
| 9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29, 31 | Q[11:0] | LVCMOS Output | | Clock Output Pins |
| 10, 14, 18, 22, 26, 30 | $V_{DDO}$ | POWER | | $V_{DDO}$ Positive Supply pins. All $V_{DD}$, $V_{DDO}$, and GND pins must be externally connected to a power supply to guarantee proper operation. Bypass each supply pin with 0.01 μF to GND. |

**Table 2. CLOCK SELECT FUNCTION TABLE**

| Control Input | Clock | |
|---|---|---|
| **CLK_SEL** | **CLK, $\overline{CLK}$** | **LVCMOS_CLK** |
| 0 | Selected | De−Selected |
| 1 | De−Selected | Selected |

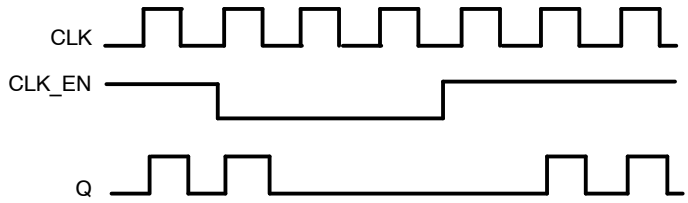



**Figure 3. CLK_EN Control Timing Diagram**

The CLK_EN control input synchronously enables or disables the outputs as shown in Figure 3. This control latches on the falling edge of the selected input CLK. When CLK_EN is LOW, the outputs are disabled in a LOW state. When CLK_EN is HIGH, the outputs are enabled as shown. CLK_EN to CLK Set up and Hold times must be satisfied.

**Table 3. ATTRIBUTES** (Note 1)

| Characteristics | | Value |
|---|---|---|
| Internal Input Pullup and Pulldown Resistor | | 50 kΩ |
| ESD Protection | Human Body Model<br>Machine Model | > 1.5 kV<br>> 200 V |
| Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1) | | Level 1 |
| Flammability Rating<br>Oxygen Index | | UL−94 code V−0 A 1/8”<br>28 to 34 |
| Transistor Count | | 275 Devices |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test | | |

1. For additional information, see Application Note AND8003/D.

**Table 4. MAXIMUM RATINGS** (Note 2)

| Symbol | Parameter | Condition | Rating | Unit |
|---|---|---|---|---|
| $V_{DD}/V_{DDO}$ | Positive Power Supply | GND = 0 V | 4.6 | V |
| $V_I$ | Input Voltage | | $-0.3 \le V_I \le V_{DD} + 0.3$ | V |
| $T_A$ | Operating Temperature Range, Industrial | | −40 to ≤ +85 | °C |
| $T_{stg}$ | Storage Temperature Range | | −65 to +150 | °C |
| $\theta_{JA}$ | Thermal Resistance (Junction−to−Ambient) | 0 lfpm<br>500 lfpm | 80<br>55 | °C/W<br>°C/W |
| $\theta_{JC}$ | Thermal Resistance (Junction−to−Case) | (Note 3) | 12−17 | °C/W |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

2. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and not valid simultaneously. If stress limits are exceeded device functional operation is not implied, damage may occur and reliability may be affected.
3. JEDEC standard multilayer board − 2S2P (2 signal, 2 power).

**Table 5. DC CHARACTERISTICS** $V_{DD}$ = $V_{DDO}$ = 3.3 ±5% (3.135 to 3.465 V) or 2.5 ±5% (2.375 to 2.625 V); $V_{DD}$ = 3.3 ±5% (3.135 to 3.465 V) and $V_{DDO}$ = 2.5 ±5% (2.375 to 2.625 V) GND = 0 V, $T_A$ = −40°C to +85°C; (Note 4)

| Symbol | Characteristic | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $I_{DD}$ | Quiescent Power Supply Current<br>3.3V $V_{DD}$ = $V_{DDO}$ or 3.3 V $V_{DD}$, 2.5 $V_{DDO}$<br>2.5 V $V_{DD}$ = $V_{DDO}$ | | | <br>55<br>52 | mA |
| $V_{IH}$ | Input HIGH Voltage at 3.465 V $V_{DD}$<br>CLK_SEL; LVCMOS_CLK, CLK_EN, OE | 2.0 | | $V_{DD}$+0.3 | V |
| | Input HIGH Voltage 2.625 $V_{DD}$<br>CLK_SEL; LVCMOS_CLK, CLK_EN, OE | 1.7 | | $V_{DD}$+0.3 | |
| $V_{IL}$ | Input LOW Voltage 3.465 V $V_{DD}$<br>CLK_SEL; LVCMOS_CLK, CLK_EN, OE | −0.3 | | 0.8 | V |
| | Input LOW Voltage 2.625 V $V_{DD}$<br>CLK_SEL; LVCMOS_CLK, CLK_EN, OE | −0.3 | | 0.7 | |
| $I_{IN}$ | Input Current ($V_{IN}$ = $V_{DD}$) | | | 300 | μA |
| $V_{OH}$ | Output HIGH Voltage $I_{OH}$ = −24 mA<br>3.3 V ±5% = $V_{DD}$ = $V_{DDO}$ | 2.4 | | | V |
| | Output HIGH Voltage $I_{OH}$ = −15 mA<br>3.3 V ±5% or 2.5 V ±5% = $V_{DD}$; 2.5 V +5% = $V_{DDO}$ | 1.8 | | | |
| $V_{OL}$ | Output LOW Voltage $I_{OL}$ = 24 mA<br>3.3 V ±5% = $V_{DD}$ = $V_{DDO}$ | | | 0.55 | V |
| | Output LOW Voltage $I_{OL}$ = 12 mA<br>3.3 V ±5% = $V_{DD}$ = $V_{DDO}$ | | | 0.3 | |
| | Output LOW Voltage $I_{OL}$ = 15 mA<br>0.3 V ±5% = $V_{DD}$; 2.5 V ±5% = $V_{DDO}$ | | | 0.6 | |
| $V_{CMR}$ | Common Mode Voltage Range (CLK/$\overline{CLK}$)<br>3.3 V ±5% or 2.5 V ±5% = $V_{DD}$ | GND+0.5 | | $V_{DD}$−0.85 | V |
| $V_{PP}$ | Input Voltage (Peak−to−Peak) CLK/$\overline{CLK}$<br>3.3 V ±5% or 2.5 V ±5% = $V_{DD}$ | 0.15 | | 1.3 | V |
| $Z_O$ | Output Impedance | 5 | 7 | 12 | Ω |
| $C_{IN}$ | Input Capacitance | | | 4 | pF |
| $C_{PD}$ | Power Dissipation Capacitance (per Output) | | 25 | | pF |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

4. Parallel terminated 50 Ω to $V_{DDO}$/2. See Figure 5.

**Table 6. AC CHARACTERISTICS** $V_{DD} = V_{DDO} = 3.3 \pm 5\%$ (3.135 to 3.465 V) or $2.5 \pm 5\%$ (2.375 to 2.625 V); $V_{DD} = 3.3 \pm 5\%$ (3.135 to 3.465 V) and $V_{DDO} = 2.5 \pm 5\%$ (2.375 to 2.625 V) GND = 0 V, $T_A = -40°C$ to $+85°C$; (Note 5)

| Symbol | Characteristic | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $F_{max}$ | Maximum Operating Frequency | 350 | | | MHz |
| $t_{PLH}/t_{PHL}$ | Propagation Delay, (crosspoint to $V_{DDO}/2$) $f \leq 350$ MHz | | | | ns |
| | 3.3 V $V_{DD} = V_{DDO}$ or 3.3 V $V_{DD}$, 2.5 V $V_{DDO}$; CLK/$\overline{CLK}$ to Qx | 1.6 | | 3.6 | ns |
| | 3.3 V $V_{DD} = V_{DDO}$ or 3.3 V $V_{DD}$, 2.5 V $V_{DDO}$; 3.3 V LVCMOS_CLK to Qx | 1.0 | | 3.0 | |
| | 2.5 V $V_{DD} = V_{DDO}$ CLK/$\overline{CLK}$ to Qx | 1.6 | | 3.6 | |
| | 2.5 V $V_{DD} = V_{DDO}$ LVCMOS_CLK to Qx | 1.0 | | 3.0 | |
| $t_{PZL}/t_{PZH}$ | Output Enable Time OE to Qx | | | 5 | ns |
| $t_{PLZ}/t_{PHZ}$ | Output Disable Time OE to Qx | | | 5 | ns |
| $tSKEW_{DC}$ | Duty Cycle Skew at $V_{DD}$ / 2 | | | | % |
| | At 150 MHz; 3.3 V $V_{DD} = V_{DDO}$ | 45 | | 55 | |
| | At 200 MHz; 2.5 V $V_{DD} = V_{DDO}$ | 45 | | 55 | |
| | At 150 MHz; 2.5 V $V_{DD} = V_{DDO}$ | 40 | | 60 | |
| $tSKEW_{D-D}$ | Device to Device Skew (similar condition) | | | | ns |
| | CLK/$\overline{CLK}$ to Qx; CLK to Qx | | | 1.0 | |
| $tSKEW_{O-O}$ | Output to Output Skew Within A Device | | 25 | 100 | ps |
| $t_S$ | Set−up Time to CLK tf | | | | ns |
| | CLK_EN to CLK/$\overline{CLK}$ | 1.0 | | | |
| | CLK_EN to CLK | 0.0 | | | |
| $t_H$ | Hold Time to CLK tf | | | | ns |
| | CLK/$\overline{CLK}$ to CLK_EN | 0.0 | | | |
| | CLK to CLK_EN | 1.0 | | | |
| tr/tf | Output rise and fall times | | | | ns |
| | (0.8 V and 2.0 V) 3.3 V $V_{DD} = V_{DDO}$ | | | 1.0 | |
| | (0.6 V and 1.8 V) or 3.3 V $V_{DD}$, 2.5 $V_{DDO}$ | | | 1.0 | |
| | (0.6 V and 1.8 V) 2.5 V $V_{DD} = V_{DDO}$ | | | 1.3 | |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. Outputs loaded with 50 Ω to $V_{TT}$ ($V_{DDO}/2$); see Figure 5. CLOCK input with 50% duty cycle. Measured at CLK/$\overline{CLK}$ crosspoint to Qx $V_{DDO}/2$, CLK $V_{DDO}/2$ to Qx $V_{DDO}/2$; see Figure 4.

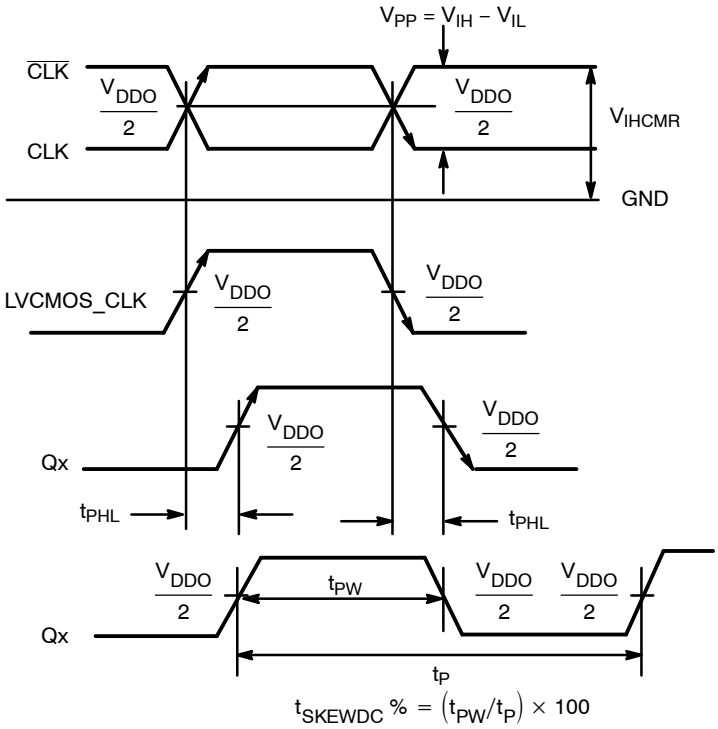



**Figure 4. AC Reference Measurement**

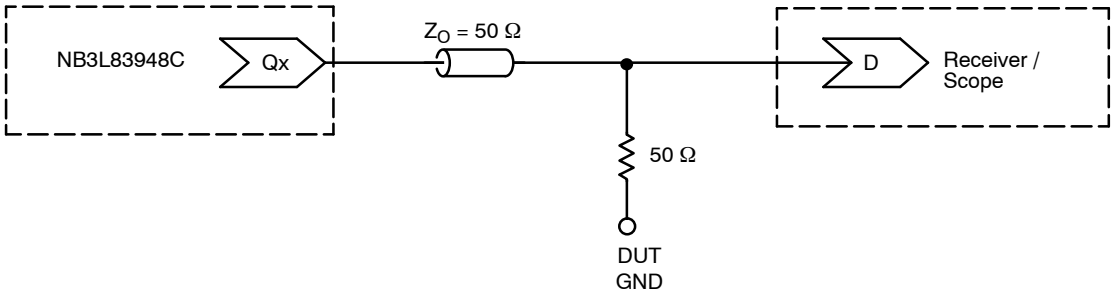



**Figure 5. Typical Termination for Output Driver and Device Evaluation. Supplies may be centered on GND (±1.65 V or ±1.25 V) to permit direct connection into 50 Ω to GND Scope modules**

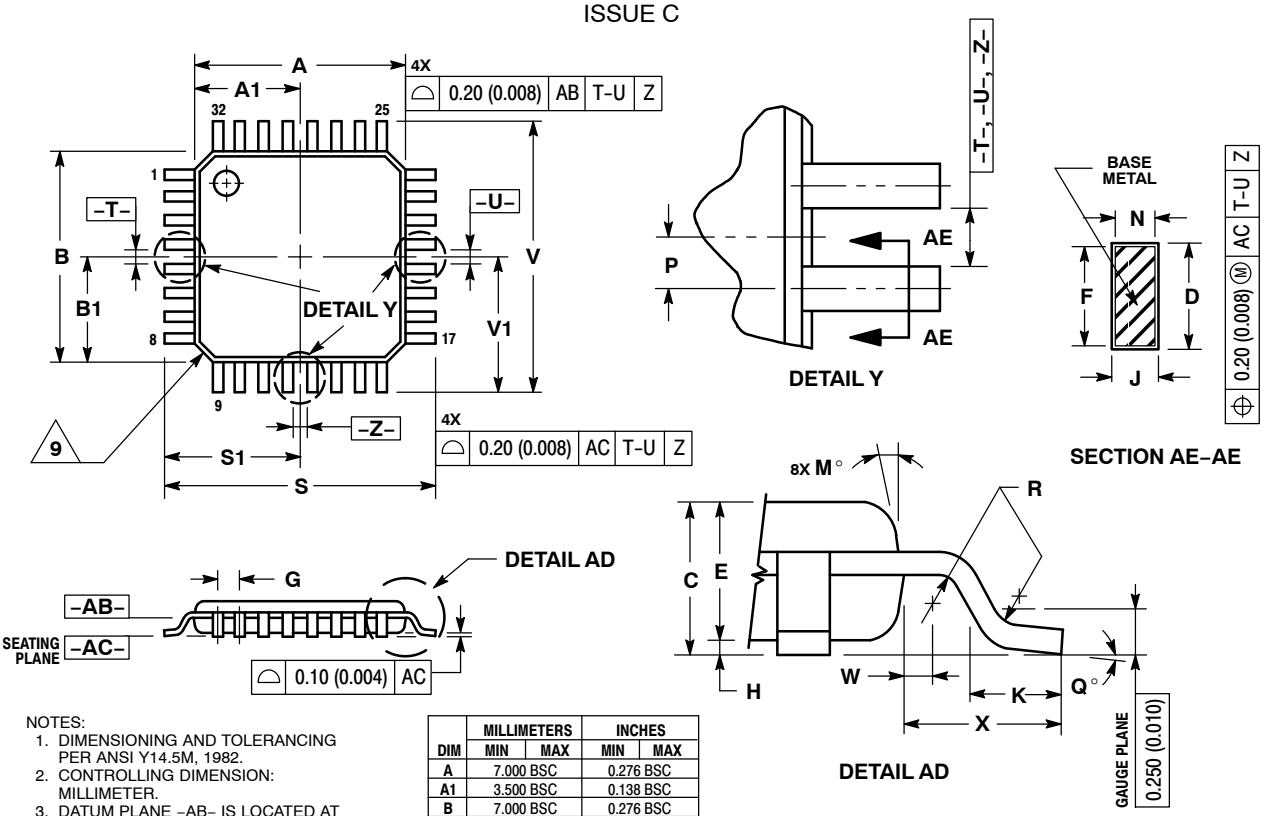
## ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| NB3L83948CFAG | LQFP−32 (Pb−Free) | 250 Units / Tray |
| NB3L83948CFAR2G | LQFP−32 (Pb−Free) | 2000 Units / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## PACKAGE DIMENSIONS

**32 LEAD LQFP**
CASE 873A–02
ISSUE C




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 7.000 BSC | | 0.276 BSC | |
| A1 | 3.500 BSC | | 0.138 BSC | |
| B | 7.000 BSC | | 0.276 BSC | |
| B1 | 3.500 BSC | | 0.138 BSC | |
| C | 1.400 | 1.600 | 0.055 | 0.063 |
| D | 0.300 | 0.450 | 0.012 | 0.018 |
| E | 1.350 | 1.450 | 0.053 | 0.057 |
| F | 0.300 | 0.400 | 0.012 | 0.016 |
| G | 0.800 BSC | | 0.031 BSC | |
| H | 0.050 | 0.150 | 0.002 | 0.006 |
| J | 0.090 | 0.200 | 0.004 | 0.008 |
| K | 0.450 | 0.750 | 0.018 | 0.030 |
| M | 12° REF | | 12° REF | |
| N | 0.090 | 0.160 | 0.004 | 0.006 |
| P | 0.400 BSC | | 0.016 BSC | |
| Q | 1° | 5° | 1° | 5° |
| R | 0.150 | 0.250 | 0.006 | 0.010 |
| S | 9.000 BSC | | 0.354 BSC | |
| S1 | 4.500 BSC | | 0.177 BSC | |
| V | 9.000 BSC | | 0.354 BSC | |
| V1 | 4.500 BSC | | 0.177 BSC | |
| W | 0.200 REF | | 0.008 REF | |
| X | 1.000 REF | | 0.039 REF | |



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