

### DESCRIPTION

These 8-bit shift registers are compatible with most other TTL, DTL, and MSI logic families. All inputs are buffered to lower the drive requirements to one normalized Series 54/74 load, and input clamping diodes minimize switching transients to simplify system design. Maximum input clock frequency is typically 35 megahertz and power dissipation is typically 360 mW.

All Series 54 devices are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . Series 74 devices are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

The bidirectional registers are designed to incorporate virtually all of the features a system designer may want in a shift register. These circuits contain 87 equivalent gates and feature parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

Parallel (Broadside) Load

Shift Right (In the direction  $Q_A$  toward  $Q_H$ )

Shift Left (In the direction  $Q_H$  toward  $Q_A$ )

Inhibit Clock (Do nothing)

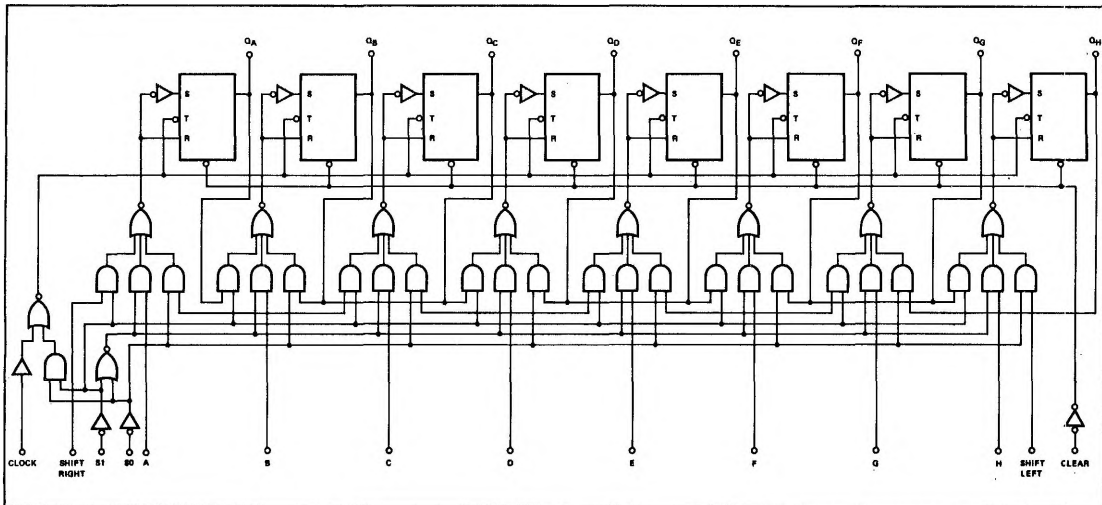
Synchronous parallel loading is accomplished by applying the 8 bits of data and taking both mode control inputs,  $S_0$  and  $S_1$ , high. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when  $S_0$  is high and  $S_1$  is low. Serial data for this mode is entered at the shift-right data input. When  $S_0$  is low and  $S_1$  is high, data shifts left synchronously and new data is entered at the shift-left serial input.

Clocking of the flip-flop is inhibited when both mode control inputs are low. The mode controls should be changed only while the clock input is high.

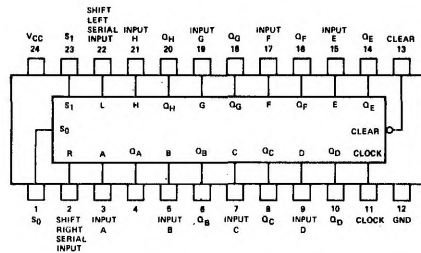
Average power dissipation per gate is typically 4.15 mW.

### LOGIC DIAGRAM



### PIN CONFIGURATIONS

#### N,F,Q PACKAGE



### TRUTH TABLE

OPERATION OF MODE CONTROL		
INPUTS		MODE
$S_1$	$S_0$	
L	L	INHIBIT CLOCK
H	L	SHIFT LEFT
L	H	SHIFT RIGHT
H	H	PARALLEL LOAD

RECOMMENDED OPERATING CONDITIONS

	S54198			N74198			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N:	High logic level			20			20
	Low logic level			10			10
Input Count Frequency, $f_{count}$	0		25	0		25	MHz
Width of Clock or Clear Pulse, $t_w$	20			20			ns
Mode-Control Setup Time, $t_{setup}$	30			30			ns
Data Setup Time, $t_{setup}$	20			20			ns
Hold Time at any Input, $t_{hold}$	0			0			ns
Operating Free-Air Temperature, $T_A$	-55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS*	S54198			N74198			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
$V_{IH}$ High-level input voltage		2			2			V
$V_{IL}$ Low-level input voltage				0.8			0.8	V
$V_I$ Input clamp voltage	$V_{CC} = MAX, I_I = -12mA$			-1.5			-1.5	V
$V_{OH}$ High-level output voltage	$V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = -800\mu A$	2.4			2.4			V
$V_{OL}$ Low-level output voltage	$V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 16mA$			0.4			0.4	V
$I_I$ Input current at maximum input voltage	$V_{CC} = MAX, V_I = 5.5V$			1			1	mA
$I_{IH}$ High-level input current	$V_{CC} = MAX, V_I = 2.4V$			40			40	$\mu A$
$I_{IL}$ Low-level input current	$V_{CC} = MAX, V_I = 0.4V$			-1.6			-1.6	mA
$I_{OS}$ Short-circuit output current†	$V_{CC} = MAX$	-20		-57	-18		-57	mA
$I_{CC}$ Supply current	$V_{CC} = MAX, \text{Table Below}$		72	104		72	116	mA

SWITCHING CHARACTERISTICS,  $V_{CC} = 5V, T_A = 25^\circ C, N = 10$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{max}$ Maximum input count frequency		25	35		MHz
$t_{PHL}$ Propagation delay time, high-to-low-level output from clear	$C_L = 15pF, R_L = 400\Omega$		23	35	ns
$t_{PHL}$ Propagation delay time, high-to-low-level output from clock		8	20	30	ns
$t_{PLH}$ Propagation delay time, low-to-high-level output from clock		8	17	26	ns

\* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

\*\* All typical values are at  $V_{CC} = 5V, T_A = 25^\circ C$ .

† Not more than one output should be shorted at a time.

TEST CONDITIONS FOR  $I_{CC}$  (all outputs are open)

TYPE	APPLY 4.5V	FIRST GROUND, THEN APPLY 4.5V	GROUND
S54198, N74198	Serial input, $S_0, S_1$	Clock	Clear, Inputs A thru H