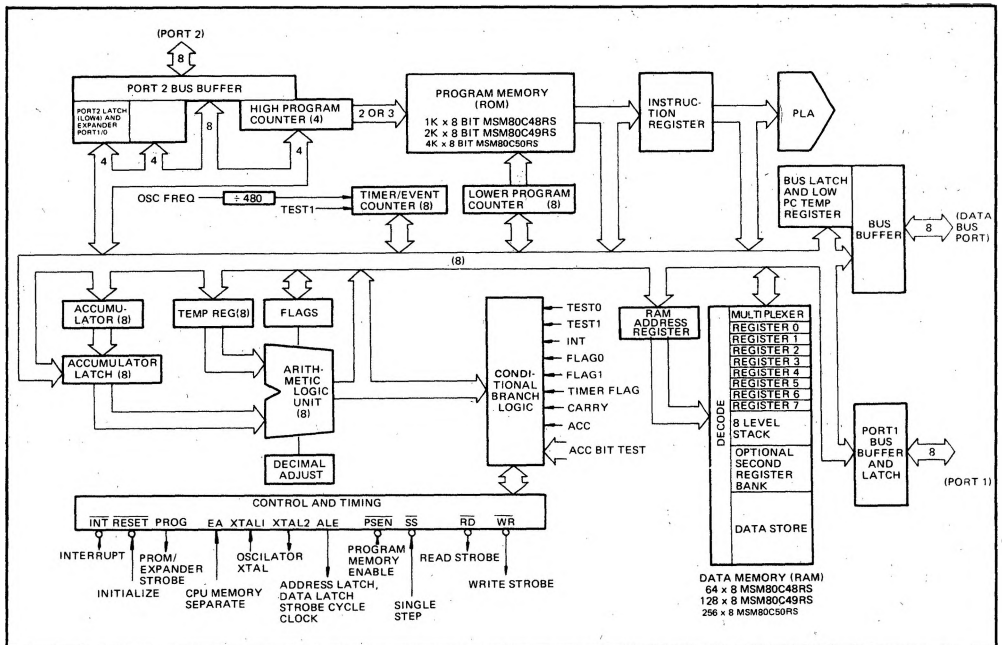
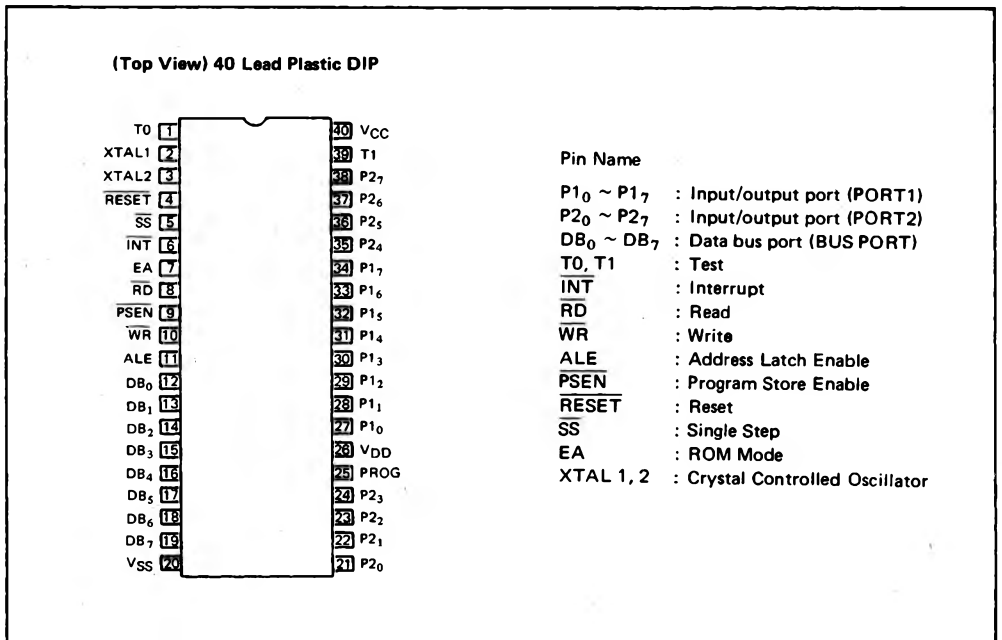


- Lower power consumption enabled by CMOS silicon gate process
- Completely static operation
- Improved power-down feature
- Minimum instruction cycle $1.36 \mu s$ (11 MHz)
@ $V_{CC} = +5V \pm 10\%$
11 MHz version of MSM80C50 (6 MHz < XTAL1.2 < 11 MHz) is under development.
- Every signal input terminal is provided with a Schmitt circuit, except XTAL1 Pin.
- Every signal output terminal is capable of driving a standard TTL, except XTAL2 Pin.
- 111 instructions
- All instructions are usable even during execution of external ROM instructions.
- Operation facility
Addition, logical operations, and decimal adjust
- Program memory (ROM) : $1K \times 8$ bits (MSM80C48)
: $2K \times 8$ bits (MSM80C49)
: $4K \times 8$ bits (MSM80C50)
- Data memory (RAM) : 64×8 bits (MSM80C48)
: 128×8 bits (MSM80C49)
: 256×8 bits (MSM80C50)
- Two sets of working registers
- External and timer interrupts
- Two test inputs
- Built-in 8-bit timer counter
- Extendable external memory and I/O ports
- Input/output ports : Input/output ports
: Data bus input/output
: $8 \text{ bits} \times 2$
: $8 \text{ bits} \times 1$
- Single-step execution function
- Every signal input terminal is provided with a Schmitt circuit, except XTAL 2 Pin
- Every signal output terminal is capable of driving a standard TTL, except X'tal 2 Pin.
- Wide range of operating voltage, from +2.5V to +6V of V_{CC} .
- High noise margin action
- Two kinds of package; 40-pin plastic DIP and 44-pin plastic flat package
- Compatible with Intel's 8048, 8049 and 8050

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

Designation	Input/Output	Function
P1 ₀ ~ P1 ₇ (PORT 1)	Input/Output	8-bit quasi-bidirectional port
P2 ₀ ~ P2 ₇ (PORT 2)	Input/Output	8-bit quasi-bidirectional port The high-order four bits of external program memory addresses can be output from P20-P23, to which the I/O expander MSM82C43RS may also be connected.
DB ₀ ~ DB ₇ (BUS)	Input/Output	Bidirectional port The low-order eight bits of external program memory address can be output from this port, and the addressed instruction is fetched under the control of PSEN signal. Also, the external data memory address is output, and data is read and written synchronously using RD and WR signals. The port can also serve as either a statically latched output port or a non-latching input port.
T0 (Test 0)	Input/Output	The input can be tested with the conditional jump instructions JT0 and JNT0. The execution of the ENT0 CLK instruction causes a clock output to be generated.
T1	Input	The input can be tested with the conditional jump instructions JT1 and JNT1. The execution of a STRT CNT instruction causes an internal counter input to be activated.
INT (Interrupt)	Input	Interrupt input. If interrupt is enabled, INT input initiates an interrupt. Interrupt is disabled after a reset. Also testable with a JN1 instruction. Can be used to terminate the power-down mode. (Active "0" level)
RD (Read)	Output	A signal to read data from external data memory. (Active "0" level)
WR (Write)		A signal to write data to external data memory. (Active "0" level)
ALE Address & Data Latch Clock		This signal is generated in each cycle. It may be used as a clock output. External data memory or external program memory is addressed upon the falling edge. For the external ROM, this signal is used to latch the bus port data upon the ALE signal rise-up after the execution of the OUTL BUS, A instruction.
PSEN Program Store Enable	Output	A signal to fetch an instruction from external program memory (Active "0" level)
RESET	Output	(RESET) input initialize the processor. (Active "0" level) Used to terminate the power-down mode.
SS (Single Step)	Output	A program is executed step by step. This pin can also be used to control internal oscillation when the power-down mode is reset. (Active "0" level)
EA (External Access)	Input	When held at high level, all instructions are fetched from external memory. (Active "1" level)
PROG (Expander Strobe)	Output	This output strobes the MSM82C43RS I/O expander.

PIN DESCRIPTION (CONT.)

Designation	Input/Output	Function
XTAL 1 (Crystal 1)	Input	One side of the crystal input for the internal oscillator. An external source can also be input.
XTAL 2 (Crystal 2)	Output	Other side of Crystal input for internal oscillator.
V _{CC}	—	Power supply terminal
V _{DD}	—	Standby control input. Normally, "1" level. When set to "0" level, oscillation is stopped and processor goes into standby mode.
V _{SS}	—	GND

Note: The required RESET pulse duration is at least two machine cycles under the condition that the power supply and the oscillator have been stabilized.

ADDED FUNCTIONS OF MSM80C48, MSM80C49 AND MSM80C50

The MSM80C48, MSM80C49 and MSM80C50 basically incorporate the capabilities of Intel's 8048, 8049, and 8050 plus the following new functions:

1. Power-Down Mode Enhancements

1.1 Power-down by software

- (1) Clock (See item 4, "Power-down mode", for details.)
 - a. Crystal-controlled oscillator halt (HLTS instruction)
Power requirements can be minimized.
 - b. Clock supply halt (HALT instruction)
Restart is accomplished without oscillator wait.
- (2) I/O ports (See Table 4-1 and 4-2 for details.)
I/O port floating instructions
Power consumption resulting from inputs/outputs can be minimized with FLT and FLTT instructions.
Port floating is cancelled by executing FRES instruction, "0" level at INT pin or "0" level at RESET pin.
- (3) Six types of power-down can be done by a combination of HLTS/HALT and FLT/FLTT instructions.

1.2 Power-down by hardware (See 4.3, Power-down mode by V_{DD} pin utilization for details.)

Crystal-controlled oscillators can be halted by controlling the V_{DD} terminal, thereby floating all I/O ports for minimum power consumption.

2. Additional Instructions (11)

HLTS	MOV A, P2
HALT	MOVP1, @ R3
FLT	MOVP1 P, @ R3
FLTT	DEC @ Rr
FRES	DJNZ @ R, addr
MOV A, P1	

3. Improved Uses of BUS P₀ ~ 7, P1₀ ~ 7, P2₀ ~ 7, and SS terminals

3.1 BUS P₀ ~ 7

The MSM80C48, MSM80C49, and MSM80C50 remove the limitation on the use of OUTL BUS, A instructions during the external ROM access mode by having an independent data latch and external ROM mode address latch in BUS P₀ ~ 7.

Consequently, there is no need to relocate bus port instructions when in the external ROM access mode.

3.2 P1₀ ~ 7 and P2₀ ~ 7

The MSM80C48, MSM80C49 and MSM80C50 are designed to minimize power consumption when P1₀ ~ 7 and P2₀ ~ 7 are used as input/output ports, to maximize the performance of CMOS.

When these ports are used as output ports, the acceleration circuit is actuated only when output data changes from "0" to "1", thus speed-

ing up the rise time of the output signals.

When these ports are used as input ports, the internal pullup resistance becomes approximately 9 kΩ when input data is "1".

The internal pullup resistance rises to approximately 100 kΩ when input data is "0". Thus, a high noise margin can be obtained by selecting the impedance and thus the outflow of current is minimized whenever these ports are used as output or input ports.

3.3 Clock generation control via the SS terminal

When the crystal-controlled oscillator is halted in the HLTS or hardware power-down mode, the SS terminal is pulled down by a resistor of 20 – 50 kΩ, while its internal pullup resistor of 200 – 500 kΩ is isolated from V_{CC}. When the power-down mode is cancelled, the internal resistor of the SS terminal is changed from pull-down to pullup. Consequently, the CPU can be halted for any period of time until the crystal-controlled oscillator resumes normal oscillation when a capacitor is connected to the SS terminal.

4. Power-Down Mode

The MSM80C48, MSM80C49, and MSM80C50 power-down mode can be enabled in 2 different ways—through software by a combination of clock control and port floating instructions, and through hardware by control of the V_{DD} pin.

4.1 Software power-down mode

Power-down mode can be done by a combination of the following instructions.

- (1) HALT (clock supply halt to control circuit)

Instruction
code:

0	0	0	0	0	0	0	1
---	---	---	---	---	---	---	---

Description:

Although crystal-controlled oscillator operation is continued, the clock supply to the CPU control circuit is halted and CPU operations suspended. When cancelling this software mode, restart is accomplished without oscillator wait. Timing charts are outlined in Figs. 4-1 and 4-2.

- (2) HLTS (oscillation stop)

Instruction
code:

1	0	0	0	0	0	1	0
---	---	---	---	---	---	---	---

Description:

The oscillator operation is halted and CPU operations suspended. In cancelling this power down mode, connecting a capacitor to the SS pin enables a reasonable

wait period to be accomplished before normal operation is resumed. [Except in the case of using the RESET pin]
Timing charts are outlined in Figs. 4-3 and 4-4.

(3) FLT (floating P₁₀ ~ 7, P₂₀ ~ 7, and BP₀ ~ 7)

Instruction code:

1 0 1 0 0 0 1 0

Description:

	Internal ROM mode	External ROM mode
P1	Floating	Floating
P2	Floating	P ₂₀ ~ 3 operation P ₂₄ ~ 7 floating
BP	Floating	Operation

Details of IC pin status as a result of executing the FLT instruction are shown in Table 4-1.

(4) FLTT (floating of all output pins)

Instruction code:

1 1 0 0 0 0 1 0

Description:

	Internal ROM mode	External ROM mode
ALE	Floating	Operation
PSEN	Floating	Operation
PROG	Floating	Floating
WR	Floating	Floating
RD	Floating	Floating
TO OUT	Floating	Floating
P1	Floating	Floating
P2	Floating	P ₂₀ ~ 3 operation P ₂₄ ~ 7 floating
BP	Floating	Operation
XTAL	Operation	Operation

Details of IC pin status as a result of executing the FLTT instruction are shown in Table 4-2.

- Example 1: Power-down mode accomplished by stopping oscillation.
○ Setting by execution of HLTS [82H] instruction.
- Example 2: Power-down mode accomplished by stopping the clock supply to the CPU control circuit.
○ Setting by execution of HALT [01H] instruction.
- Example 3: Power-down mode by floating of P₁₀ ~ 7, P₂₀ ~ 7 and BP₀ ~ 7, and subsequent stopping of CPU oscillation.

- Setting by first executing the FLT[A2H] instruction and then the HLTS[82H] instruction.

Example 4: Power-down mode by floating P₁₀ ~ 7, P₂₀ ~ 7 and BP₀ ~ 7, and then stopping the clock supply to the CPU control circuit.

- Setting by first executing the FLT[A2H] instruction, and then the HALT[01H] instruction.

Example 5: Power-down mode by floating all output pins, followed by stopping oscillation.

- Setting by first executing the FLTT[C2H] instruction followed by execution of the HLTS[82H] instruction.

Example 6: Power-down mode by floating all output pins, followed by stopping of the clock supply to the CPU control circuit.

- Setting by first executing the FLTT[C2H] instruction, followed by execution of the HALT[01H] instruction.

4.2 Cancellation of software power-down mode

The power-down mode status outlined above in examples 1 to 6 can be cancelled by using either the interrupt pin or the RESET pin.

- Use of the INT pin during external interrupt enabled mode (i.e. following execution of ENI instruction).
 - The clock generator is activated and the CPU started up when a "0" level is applied to the INT pin. If this "0" level is maintained until at least 2 ALE output signals occur, an external interrupt is generated, and execution proceeds from address 3. If, however, the power-down mode has been done during the interrupt processing routine, execution is resumed just after the power-down instruction.
- Use of the INT pin during external interrupt disabled mode (i.e. following execution of DISI instruction or hardware reset)
 - The clock generator is activated and the CPU started up when a "0" level is applied to the INT pin. If this "0" level is maintained until at least 2 ALE output signals occur, execution is resumed just after the power-down instruction.
- Use of the RESET pin
 - The clock generator is activated and the CPU started up when a "0" level is applied to the RESET pin. If this "0" level is maintained until at least 2 ALE output signals occur, the CPU is reset and execution proceeds from address 0. In case cancellation is done in oscillation stop mode, the "0" level must be input to the RESET PIN until oscillation is stabilized.

Table 4-1 Details of Pin Status Following Execution of FLT Instruction

Pin No.	Pin Name	Internal ROM	External ROM
1P	T0	Active	Active
2P	XTAL1	Active	Active
3P	XTAL2	Active	Active
4P	RESET	Active	Active
5P	SS	200 ~ 500 k Ω pullup	200 ~ 500 k Ω pullup
6P	INT	Active	Active
7P	EA	Active	Active
8P	RD	Active	Active
9P	PSEN	Active	Active
10P	WR	Active	Active
11P	ALE	Active	Active
12P	DB0	Floating	Active
13P	DB1	Floating	Active
14P	DB2	Floating	Active
15P	DB3	Floating	Active
16P	DB4	Floating	Active
17P	DB5	Floating	Active
18P	DB6	Floating	Active
19P	DB7	Floating	Active
20P	VSS	0 [V]	0 [V]
21P	P20	Floating	Active
22P	P21	Floating	Active
23P	P22	Floating	Active
24P	P23	Floating	Active
25P	PROG	Active	Active
26P	VDD	"1" level	"1" level
27P	P10	Floating	Floating
28P	P11	Floating	Floating
29P	P12	Floating	Floating
30P	P13	Floating	Floating
31P	P14	Floating	Floating
32P	P15	Floating	Floating
33P	P16	Floating	Floating
34P	P17	Floating	Floating
35P	P24	Floating	Floating
36P	P25	Floating	Floating
37P	P26	Floating	Floating
38P	P27	Floating	Floating
39P	T1	Active	Active
40P	VCC	+2 to +6 [V]	+2 to +6 [V]

Note: The FLT mode itself is reset by executing the FRES instruction, or supplying "0" level to INT or RESET pin.

Table 4-2 Details of Pin Status Following Execution of FLTT Instruction

Pin No.	Pin Name	Internal ROM	External ROM
1P	T0	Floating if output enabled	Floating if output enabled
2P	XTAL1	Active	Active
3P	XTAL2	Active	Active
4P	RESET	Active	Active
5P	SS	200 to 500 k Ω pullup	200 to 500 k Ω pullup
6P	INT	Active	Active
7P	EA	Active	Active
8P	RD	Floating	Floating
9P	PSEN	Floating	Active
10P	WR	Floating	Floating
11P	ALE	Floating	Active
12P	DB0	Floating	Active
13P	DB1	Floating	Active
14P	DB2	Floating	Active
15P	DB3	Floating	Active
16P	DB4	Floating	Active
17P	DB5	Floating	Active
18P	DB6	Floating	Active
19P	DB7	Floating	Active
20P	VSS	0 [V]	0 [V]
21P	P20	Floating	Active
22P	P21	Floating	Active
23P	P22	Floating	Active
24P	P23	Floating	Active
25P	PROG	Floating	Floating
26P	VDD	"1" level	"1" level
27P	P10	Floating	Floating
28P	P11	Floating	Floating
29P	P12	Floating	Floating
30P	P13	Floating	Floating
31P	P14	Floating	Floating
32P	P15	Floating	Floating
33P	P16	Floating	Floating
34P	P17	Floating	Floating
35P	P24	Floating	Floating
36P	P25	Floating	Floating
37P	P26	Floating	Floating
38P	P27	Floating	Floating
39P	T1	Active	Active
40P	VCC	+2.5 to +6 [V]	+2.5 to +6 [V]

Note: The FLTT mode itself is reset by executing the FRES instruction, or supplying "0" level to INT or RESET pin.

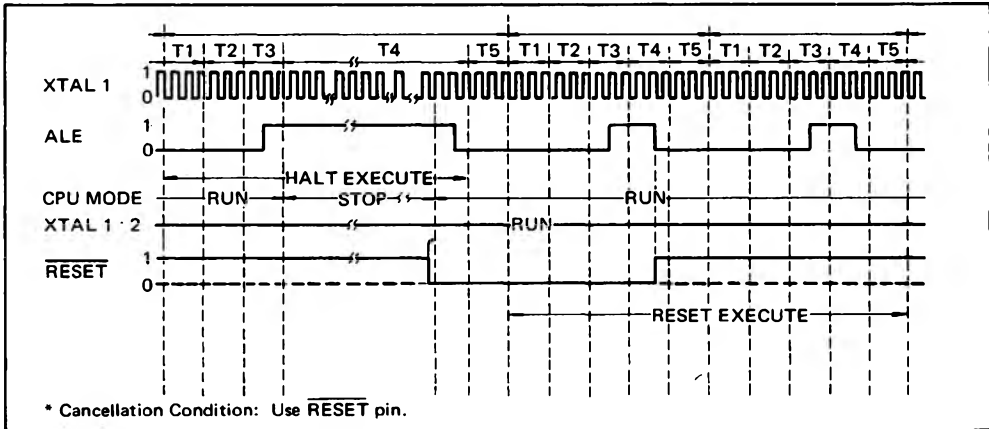


Fig. 4-1 HALT [01H] Instruction Execution Timing Chart

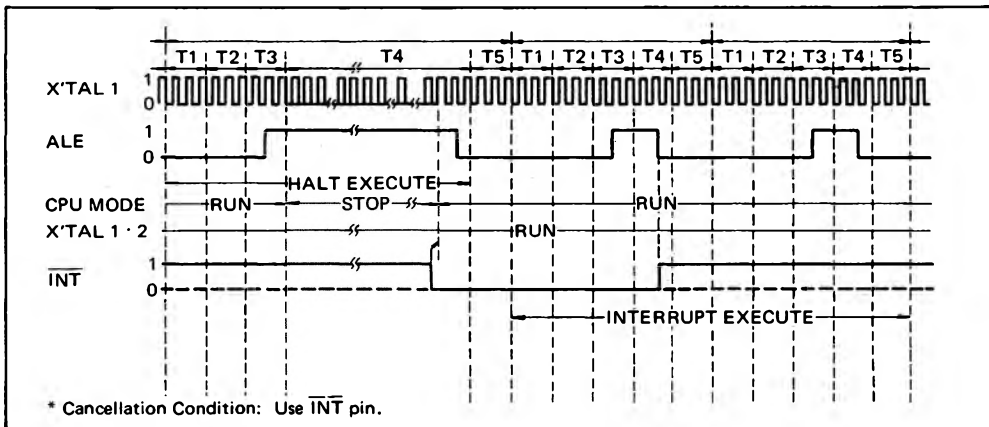


Fig. 4-2 HALT [01H] Instruction Execution Timing Chart

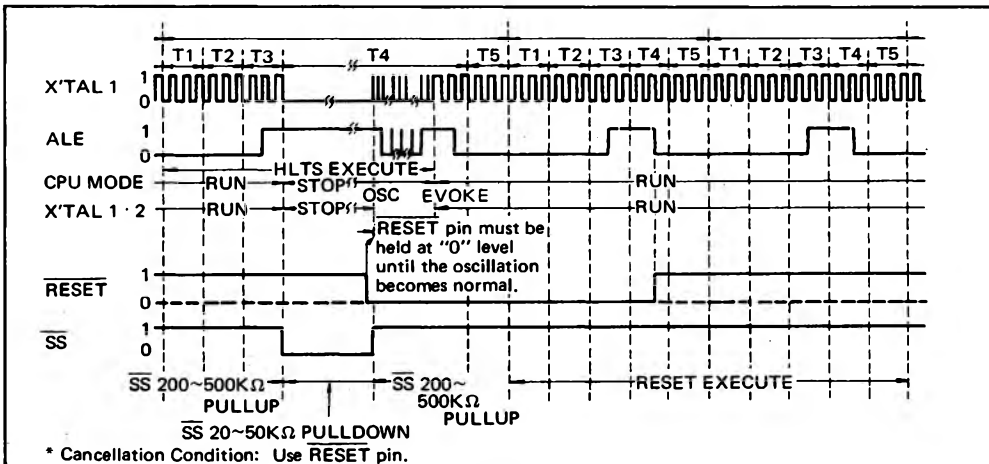


Fig. 4-3 HLTS [82H] Instruction Execution Timing Chart

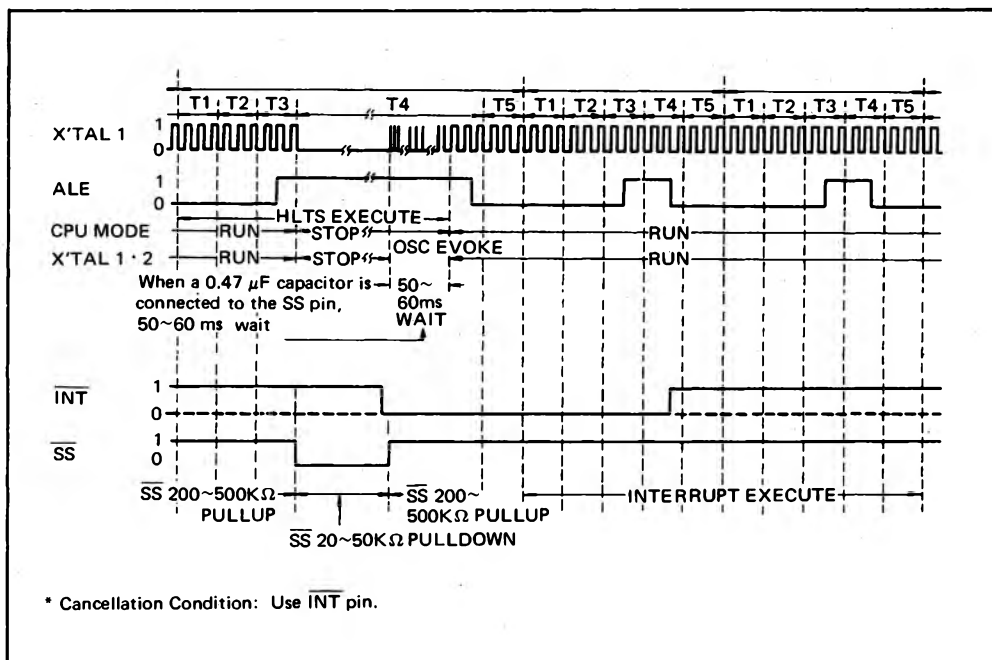


Fig. 4-4 HLTs [82H] Instruction Execution Timing Chart

4.3 Hardware power-down mode

In the MSM80C48, MSM80C49 and MSM80C50, forcing the level at the V_{DD} pin [pin 26] to a "0" during either external ROM or internal ROM mode results in suspension of the oscillator function and subsequent floating (high impedance) of all the I/O pins except the RESET, SS and XTAL 1/2 pins. The CPU is thereby stopped while maintaining internal status. Details of the IC pin status at this time are outlined in Table 4-3.

4.4 Cancellation of hardware power-down mode

- (1) Use of RESET pin
 - The clock generator is activated and the CPU started up when a "1" level is applied to the V_{DD} pin while a "0" level is input to the RESET pin. If this "0" level is kept applied to the RESET pin until oscillation become stable, the CPU will be reset and will start executing from address 0. The timing chart is outlined in Fig. 4-5.
- (2) Use of the INT pin during external interrupt enabled status (i.e. following execution of ENI instruction)
 - The clock generator is activated and the CPU started up when a "1" level is applied to the V_{DD} pin while a "0" level is applied to the INT pin.

If this "0" level is maintained until at least 2 ALE output signals occur, an external interrupt is generated, and execution starts from address 3.

However, if the power-down mode is started during an interrupt processing routine, execution will be continued on the next instruction after the present instruction. The timing chart is outlined in Fig. 4-6.

- (3) Use of the INT pin during external interrupt disabled mode (i.e. following execution of DISI instruction or hardware reset)
 - The clock generator is activated and the CPU started up when a "1" level is applied to the V_{DD} pin while a "0" level is applied to the INT pin. If this "0" level is maintained until at least 2 ALE output signals occur, execution is continued on the next instruction after the present instruction. The timing chart is outlined in Fig. 4-6.
- (4) Use of V_{DD} pin only
 - The clock generator is activated and the CPU started up when a "1" level is applied to the V_{DD} pin while a "1" level is also applied to both the RESET and INT pins. In this case, execution is resumed from the stopped position. The timing chart is outlined in Fig. 4-7.

Table 4-3 Details of Pin Status during Hardware Power-Down Mode

Pin No.	Pin Name	Normal Operation ($V_{DD} = "1"$ level)	Power Down Mode ($V_{DD} = "0"$ level)
1P	T0	Active	Floating if output enabled
2P	XTAL1	Active	Active
3P	XTAL2	Active	Active
4P	RESET	Active	Active
5P	SS	200 to 500 k Ω pullup	20 to 50 k Ω pulldown
6P	INT	Active	Active
7P	EA	Active	Active
8P	RD	Active	Floating
9P	PSEN	Active	Floating
10P	WR	Active	Floating
11P	ALE	Active	Floating
12P	DB0	Active	Floating
13P	DB1	Active	Floating
14P	DB2	Active	Floating
15P	DB3	Active	Floating
16P	DB4	Active	Floating
17P	DB5	Active	Floating
18P	DB6	Active	Floating
19P	DB7	Active	Floating
20P	V _{SS}	0 [V]	0 [V]
21P	P20	Active	Floating
22P	P21	Active	Floating
23P	P22	Active	Floating
24P	P23	Active	Floating
25P	PROG	Active	Floating
26P	V _{DD}	"1" level	"0" level
27P	P10	Active	Floating
28P	P11	Active	Floating
29P	P12	Active	Floating
30P	P13	Active	Floating
31P	P14	Active	Floating
32P	P15	Active	Floating
33P	P16	Active	Floating
34P	P17	Active	Floating
35P	P24	Active	Floating
36P	P25	Active	Floating
37P	P26	Active	Floating
38P	P27	Active	Floating
39P	T1	Active	Active
40P	V _{CC}	+2 to +6 [V]	+2 to +6 [V]

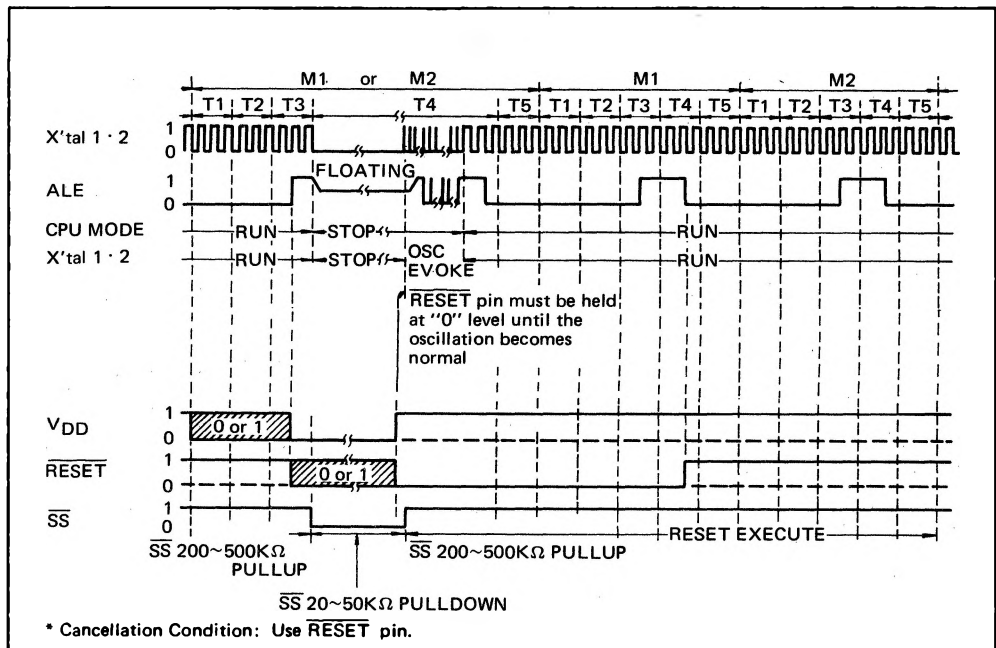


Fig. 4-5 Hardware Power-Down Mode Timing Chart

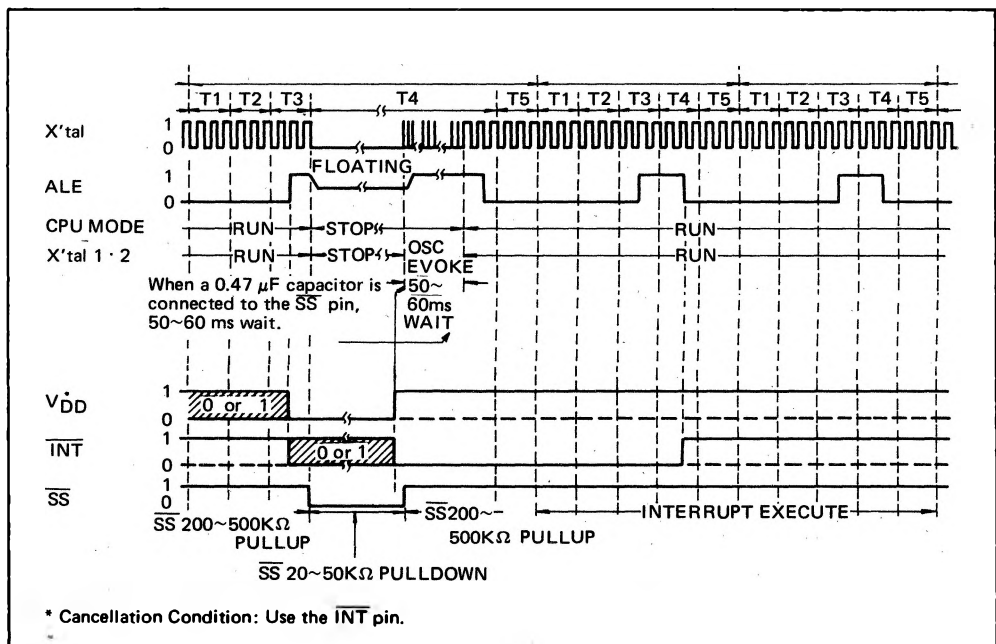


Fig. 4-6 Hardware Power-Down Mode Timing Chart

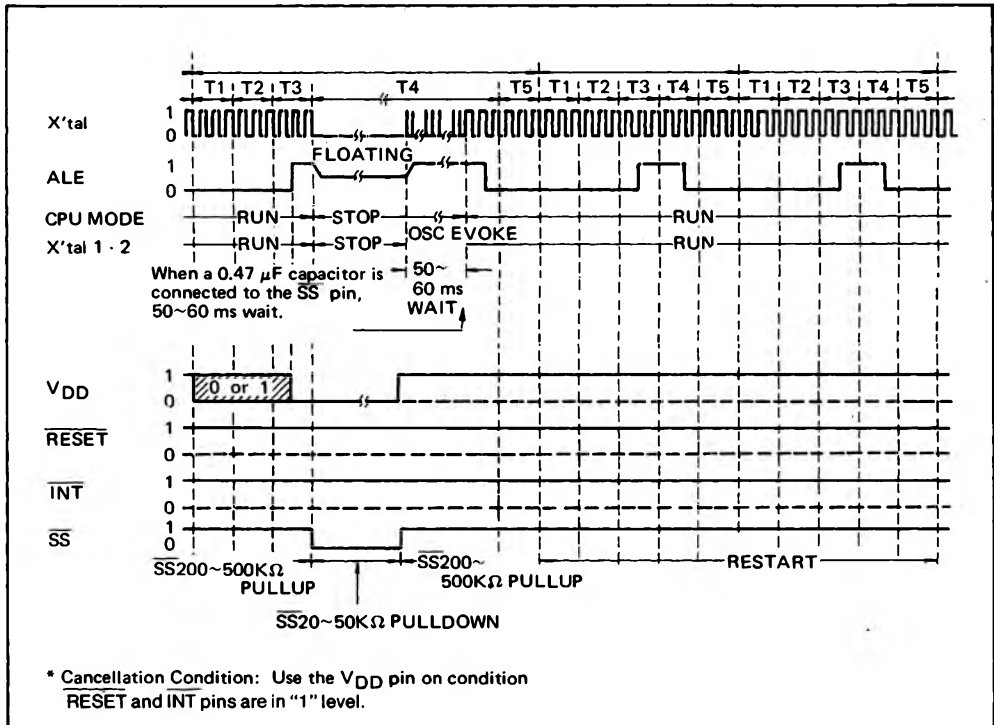


Fig. 4-7 Hardware Power-Down Mode Timing Chart

MSM80C48/MSM80C49/MSM80C50 INSTRUCTION TABLE

H	L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	0 0 0 0	NOP	HALT Added	OUTL BUS A	ADD A, # data	JMP	ENI		DECA	INS A, BUS	INA, P1	INA, P2		MOVD A, Pp			
1	0 0 0 1	INC @R0	INC @R1	JB0 addr	ADDC A, # data	CALL	DISI	JTF addr	INCA	INC Rr							
2	0 0 1 0	XCHA @, R0	XCHA @, R1		MOV A, # data	JMP	ENTONTI	JNT0 addr	CLRA	XCHA, Rr							
3	0 0 1 1	XCHD A, @R0	XCHD A, @R1	JB1 addr		CALL	DIS TCNTI	JT0 addr	CPLA		OUTL P1, A	OUTL P2, A		MOVD Pp, A			
4	0 1 0 0	ORLA @R0	ORLA @R1	MOV A, T	ORLA, # data	JMP	STR CNT	JNT1 addr	SWAP A	ORLA, Rr							
5	0 1 0 1	ANLA @R0	ANLA @R1	JB2 addr	ANLA, # data	CALL	STR T	JT1 addr	DA A	ANLA, Rr							
6	0 1 1 0	ADDA @R0	ADDA @R1	MOV T, A	MOV A, P1 Added	JMP	STOP TCNT		RRC A	ADD A, Rr							
7	0 1 1 1	ADDC A, @R0	ADDC A, @R1	JB3 addr	MOV A, P2 Added	CALL	ENTO CLK	JF1 addr	RR A	ADDC A, Rr							
8	1 0 0 0	MOVX A, @R0	MOVX A, @R1	HLTS Added	RET	JMP	CLR F0	JN1 addr		ORL BUS, # data	ORL P1, # data	ORL P2, # data		ORLD Pp, A			
9	1 0 0 1	MOVX @R0, A	MOVX @R1, A	JB4 addr	RETR	CALL	CLR F0	JNZ addr	CLRC	ANL BUS, # data	ANL P1, # data	ANL P2, # data		ANL D Pp, A			
A	1 0 1 0	MOV @R0, A	MOV @R1, A	FLT Added	MOV P, A @A	JMP	CLR F1		CPL C	MOV Rr, A							
B	1 0 1 1	MOV @R0, # data	MOV @R1, # data	JB5 addr	JMPP @A	CALL	CPL F1	JF0 addr		MOV Rr, # data							
C	1 1 0 0	DEC @R0 Added	DEC @R1 Added	FLTT Added	MOV P1 P, R3 Added	JMP	SEL RB0	JZ addr	MOV A, PSW	DEC Rr							
D	1 1 0 1	XRL A, @R0	XRL A, @R1	JB6 addr	XRLA, # data	CALL	SEL RB1		MOV PSW, A	XRLA, Rr							
E	1 1 1 0	DJNZ @R0 Added	DJNZ @R1 Added	FRES Added	MOV P3 A, @A	JMP	SEL MB0	JNC addr	RL A	DJNZ Rr							
F	1 1 1 1	MOV A, @R0	MOV A, @R1	JB7 addr	MOV P1, R3 Added	CALL	SEL MB1	JC addr	RLCA	MOV A, Rr							

EXPLANATION OF INSTRUCTION SYMBOLS

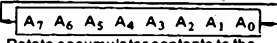
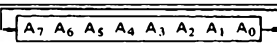
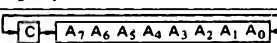
Symbols are listed below.

A	: Accumulator	PC	: Program counter
AC	: Auxiliary carry	Pp	: Port indicator (p = 4 ~ 7)
addr	: 12-bit program memory address or its part	PSW	: Program status word
Bb	: Bit indicator (b = 0 ~ 7)	Rr	: Register indicator (r = 0 ~ 7)
BS	: Bank switch	SP	: Stack pointer
BUS	: BUS PORT	T	: Timer
C	: Carry	TF	: Timer flag
CLK	: Clock	T0, T1	: Test pins T0 and T1
CNT	: Counter	X	: External RAM
D	: 4-bit data	#	: Symbol denoting immediate data
data	: 8-bit numerical value	@	: Symbol denoting indirect address
DBF	: Memory data bank flip-flop	(X)	: Denotes contents of X
F0, F1	: F0 flag and F1 flag	((X))	: Denotes contents addressed by X
I	: Interrupt	←	: Transference

LIST OF INSTRUCTIONS

Classification	Mnemonic	Instruction Code								Hexa-decimal	Byte	Cycle	Description
		D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀				
Accumulator operation instructions	ADD A, Rr	0	1	1	0	1	r ₂	r ₁	r ₀	68~6F	1	1	(AC), (C), (A) ← (A) + (Rr)
	ADD A, @Rr	0	1	1	0	0	0	0	r ₀	60~61	1	1	(AC), (C), (A) ← (A) + ((Rr))
	ADD A, #data	0	0	0	0	0	0	1	1	03 Byte 2	2	2	(AC), (C), (A) ← (A) + data
	ADDC A, Rr	0	1	1	1	1	r ₂	r ₁	r ₀	78~7F	1	1	(AC), (C), (A) ← (A) + (Rr) + (C)
	ADDC A, @Rr	0	1	1	1	0	0	0	r ₀	70~71	1	1	(AC), (C), (A) ← (A) + ((Rr)) + (C)
	ADDC A, #data	0	0	0	1	0	0	1	1	13 Byte 2	2	2	(AC), (C), (A) ← (A) + data + (C)
	ANL A, Rr	0	1	0	1	1	r ₂	r ₁	r ₀	58~5F	1	1	(A) ← (A) AND (Rr)
	ANL A, @Rr	0	1	0	1	0	0	0	r ₀	50~51	1	1	(A) ← (A) AND ((Rr))
	ANL A, #data	0	1	0	1	0	0	1	1	53 Byte 2	2	2	(A) ← (A) AND data
	ORL A, Rr	0	1	0	0	1	r ₂	r ₁	r ₀	48~4F	1	1	(A) ← (A) OR (Rr)
	ORL A, @Rr	0	1	0	0	0	0	0	r ₀	40~41	1	1	(A) ← (A) OR ((Rr))
	ORL A, #data	0	1	0	0	0	0	1	1	43 Byte 2	2	2	(A) ← (A) OR data
	XRL A, Rr	1	1	0	1	1	r ₂	r ₁	r ₀	D8~DF	1	1	(A) ← (A) XOR (Rr)
	XRL A, @Rr	1	1	0	1	0	0	0	r ₀	D0~D1	1	1	(A) ← (A) XOR ((Rr))
	XRL A, #data	1	1	0	1	0	0	1	1	D3 Byte 2	2	2	(A) ← (A) XOR data
	INC A	0	0	0	1	0	1	1	1	17	1	1	(A) ← (A) + 1
	DEC A	0	0	0	0	0	1	1	1	07	1	1	(A) ← (A) - 1
	CLRA	0	0	1	0	0	1	1	1	27	1	1	(A) ← 0
	CPLA	0	0	1	1	0	1	1	1	37	1	1	(A) ← (A)
	DAA	0	1	0	1	0	1	1	1	57	1	1	Add 6 to bits 0 ~ 3 when contents of accumulator bits 0 ~ 3 exceed 9 or when auxiliary carry (AC) is 1. Then add 6 to bits 4 ~ 7 when the result of adding the carry from the lower 0 ~ 3 exceeds 9, or when carry (C) is 1. Set 1 in the carry flag if an overflow is generated in the end result, or when the carry prior to adjustment is 1.

LIST OF INSTRUCTIONS (CONT.)

Classification	Mnemonic	Instruction Code D ₇ D ₆ D ₅ D ₄ D ₃ D ₂ D ₁ D ₀	Hexa- decimal	Byte	Cycle	Description
Accumulator operation instructions	SWAP A	0 1 0 0 0 1 1 1	47	1	1	(A _{4~7}) ← (A _{0~3})
	RL A	1 1 1 0 0 1 1 1	E7	1	1	 Rotate accumulator contents to the left by 1 bit.
	RLC A	1 1 1 1 0 1 1 1	F7	1	1	 Rotate accumulator contents with carry to the left by 1 bit.
	RR A	0 1 1 1 0 1 1 1	77	1	1	 Rotate accumulator contents to the right by 1 bit.
	RRC A	0 1 1 0 0 1 1 1	67	1	1	 Rotate accumulator contents with carry to the right by 1 bit.
Input/output instructions	INA, P1	0 0 0 0 1 0 0 1	09	1	2	(A) ← (P1)
	INA, P2	0 0 0 0 1 0 1 0	0A	1	2	(A) ← (P2)
	OUTL P1, A	0 0 1 1 1 0 0 1	39	1	2	(P1) ← (A)
	OUTL P2, A	0 0 1 1 1 0 1 0	3A	1	2	(P2) ← (A)
	ANL P1, #data	1 0 0 1 1 0 0 1 d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	99 Byte 2	2	2	(P1) ← (P1) AND data
	ANL P2, #data	1 0 0 1 1 0 1 0 d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	9A Byte 2	2	2	(P2) ← (P2) AND data
	ORL P1, #data	1 0 0 0 1 0 0 1 d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	89 Byte 2	2	2	(P1) ← (P1) OR data
	ORL P2, #data	1 0 0 0 1 0 1 0 d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	8A Byte 2	2	2	(P2) ← (P2) OR data
	INS A, BUS	0 0 0 0 1 0 0 0	08	1	2	(A) ← (BUS)
	OUTL BUS, A	0 0 0 0 0 0 1 0	02	1	2	(BUS) ← (A)
	ANL BUS, #data	1 0 0 1 1 0 0 0 d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	98 Byte 2	2	2	(BUS) ← (BUS) AND data
	ORL BUS, #data	1 0 0 0 1 0 0 0 d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	88 Byte 2	2	2	(BUS) ← (BUS) OR data
	MOVD A, Pp	0 0 0 0 1 1 P ₁ P ₀	0C~0F	1	2	(A _{0~3}) ← (Pp) p=4~7 (A _{4~7}) ← 0
Register operation instructions	MOVD Pp, A	0 0 1 1 1 1 P ₁ P ₀	3C~3F	1	2	(Pp) ← (A _{0~3}) p=4~7
	ANLD Pp, A	1 0 0 1 1 1 P ₁ P ₀	9C~9F	1	2	(Pp) ← (Pp) AND (A _{0~3}) p=4~7
	ORLD Pp, A	1 0 0 0 1 1 P ₁ P ₀	8C~8F	1	2	(Pp) ← (Pp) OR (A _{0~3}) p=4~7
	INC Rr	0 0 0 1 1 r ₂ r ₁ r ₀	18~1F	1	1	(Rr) ← (Rr) + 1
	INC @Rr	0 0 0 1 0 0 0 r ₀	10~11	1	1	((Rr)) ← ((Rr)) + 1
Branching instructions	DEC Rr	1 1 0 0 1 r ₂ r ₁ r ₀	C8~CF	1	1	(Rr) ← (Rr) - 1
	DEC @Rr	1 1 0 0 0 0 0 r ₀	C0~C1	1	1	((Rr)) ← ((Rr)) - 1
	JMP addr	a ₁₀ a ₉ a ₈ 0 0 1 0 0 a ₇ a ₆ a ₅ a ₄ a ₃ a ₂ a ₁ a ₀	44~E4 Byte 2	2	2	(PC _{8~10}) ← addr 8~10 (PC _{0~7}) ← addr 0~7 (PC ₁₁) ← DBF
	JMPP @A	1 0 1 1 0 0 1 1	B3	1	2	(PC _{0~7}) ← ((A))

LIST OF INSTRUCTIONS (CONT.)

Classification	Mnemonic	Instruction Code D ₇ D ₆ D ₅ D ₄ D ₃ D ₂ D ₁ D ₀	Hexa- decimal	Byte	Cycle	Description
Branching instructions	DJNZ Rr, addr	1 1 1 0 1 r ₂ r ₁ r ₀ a ₇ a ₆ a ₅ a ₄ a ₃ a ₂ a ₁ a ₀	E8~EF Byte 2	2	2	(Rr) $\rightarrow$ (Rr) - 1 (PC _{0~7}) $\rightarrow$ addr if (Rr) = 0 (PC) $\rightarrow$ (PC) + 2 if (Rr) = 0
	DJNZ @Rr, addr	1 1 1 0 0 0 0 r ₀ a ₇ a ₆ a ₅ a ₄ a ₃ a ₂ a ₁ a ₀	E0~E1 Byte 2	2	2	((Rr)) $\rightarrow$ ((Rr)) - 1 (PC _{0~7}) $\rightarrow$ addr if ((Rr)) = 0 (PC) $\rightarrow$ (PC) + 2 if ((Rr)) = 0
	JC addr	1 1 1 1 0 1 1 0 a ₇ a ₆ a ₅ a ₄ a ₃ a ₂ a ₁ a ₀	F6 Byte 2	2	2	(PC _{0~7}) $\rightarrow$ addr if C = 1 (PC) $\rightarrow$ (PC) + 2 if C = 0
	JNC addr	1 1 1 0 0 1 1 0 a ₇ a ₆ a ₅ a ₄ a ₃ a ₂ a ₁ a ₀	E6 Byte 2	2	2	(PC _{0~7}) $\rightarrow$ addr if C = 0 (PC) $\rightarrow$ (PC) + 2 if C = 1
	JZ addr	1 1 0 0 0 1 1 0 a ₇ a ₆ a ₅ a ₄ a ₃ a ₂ a ₁ a ₀	C6 Byte 2	2	2	(PC _{0~7}) $\rightarrow$ addr if A = 0 (PC) $\rightarrow$ (PC) + 2 if A $\neq$ 0
	JNZ addr	1 0 0 1 0 1 1 0 a ₇ a ₆ a ₅ a ₄ a ₃ a ₂ a ₁ a ₀	96 Byte 2	2	2	(PC _{0~7}) $\rightarrow$ addr if A $\neq$ 0 (PC) $\rightarrow$ (PC) + 2 if A = 0
	JT0 addr	0 0 1 1 0 1 1 0 a ₇ a ₆ a ₅ a ₄ a ₃ a ₂ a ₁ a ₀	36 Byte 2	2	2	(PC _{0~7}) $\rightarrow$ addr if T0 = 1 (PC) $\rightarrow$ (PC) + 2 if T0 = 0
	JNT0 addr	0 0 1 0 0 1 1 0 a ₇ a ₆ a ₅ a ₄ a ₃ a ₂ a ₁ a ₀	26 Byte 2	2	2	(PC _{0~7}) $\rightarrow$ addr if T0 = 0 (PC) $\rightarrow$ (PC) + 2 if T0 = 1
	JT1 addr	0 1 0 1 0 1 1 0 a ₇ a ₆ a ₅ a ₄ a ₃ a ₂ a ₁ a ₀	56 Byte 2	2	2	(PC _{0~7}) $\rightarrow$ addr if T1 = 1 (PC) $\rightarrow$ (PC) + 2 if T1 = 0
	JNT1 addr	0 1 0 0 0 1 1 0 a ₇ a ₆ a ₅ a ₄ a ₃ a ₂ a ₁ a ₀	46 Byte 2	2	2	(PC _{0~7}) $\rightarrow$ addr if T1 = 0 (PC) $\rightarrow$ (PC) + 2 if T1 = 1
	JF0 addr	1 0 1 1 0 1 1 0 a ₇ a ₆ a ₅ a ₄ a ₃ a ₂ a ₁ a ₀	B6 Byte 2	2	2	(PC _{0~7}) $\rightarrow$ addr if F0 = 1 (PC) $\rightarrow$ (PC) + 2 if F0 = 0
	JF1 addr	0 1 1 1 0 1 1 0 a ₇ a ₆ a ₅ a ₄ a ₃ a ₂ a ₁ a ₀	76 Byte 2	2	2	(PC _{0~7}) $\rightarrow$ addr if F1 = 1 (PC) $\rightarrow$ (PC) + 2 if F1 = 0
Sub-routine instructions	JTF addr	0 0 0 1 0 1 1 0 a ₇ a ₆ a ₅ a ₄ a ₃ a ₂ a ₁ a ₀	16 Byte 2	2	2	(PC _{0~7}) $\rightarrow$ addr TF if TF = 1 (PC) $\rightarrow$ (PC) + 2 if TF = 0
	JNI addr	1 0 0 0 0 1 1 0 a ₇ a ₆ a ₅ a ₄ a ₃ a ₂ a ₁ a ₀	86 Byte 2	2	2	(PC _{0~7}) $\rightarrow$ addr if INT = 0 (PC) $\rightarrow$ (PC) + 2 if INT = 1
	JBb addr	b ₂ b ₁ b ₀ 1 0 0 1 0 a ₇ a ₆ a ₅ a ₄ a ₃ a ₂ a ₁ a ₀	12~F2 Byte 2	2	2	(PC _{0~7}) $\rightarrow$ addr if Bb = 1 (PC) $\rightarrow$ (PC) + 2 if Bb = 0
	CALL addr	a ₁₀ a ₉ a ₈ 1 0 1 0 0 a ₇ a ₆ a ₅ a ₄ a ₃ a ₂ a ₁ a ₀	14~F4 Byte 2	2	2	((SP)) $\rightarrow$ (PC) + 2, (PSW _{4~7}) (PC _{0~10}) $\rightarrow$ addr8~10 (PC _{0~7}) $\rightarrow$ addr0~7 (PC ₁₁) $\rightarrow$ DBF (SP) $\rightarrow$ (SP) + 1
Flag operation instructions	RET	1 0 0 0 0 0 1 1	83	1	2	(SP) $\rightarrow$ (SP) - 1 (PC) $\rightarrow$ ((SP))
	RETR	1 0 0 1 0 0 1 1	93	1	2	(SP) $\rightarrow$ (SP) - 1 (PC) $\rightarrow$ ((SP)) (PSW _{4~7}) $\rightarrow$ ((SP)) INT END
	CLRC	1 0 0 1 0 1 1 1	97	1	1	(C) $\rightarrow$ 0
	CPLC	1 0 1 0 0 1 1 1	A7	1	1	(C) $\rightarrow$ (C)
	CLRF0	1 0 0 0 0 1 0 1	85	1	1	(F0) $\rightarrow$ 0
	CPLF0	1 0 0 1 0 1 0 1	95	1	1	(F0) $\rightarrow$ (F0)
Data transfer instructions	CLRF1	1 0 1 0 0 1 0 1	A5	1	1	(F1) $\rightarrow$ 0
	CPLF1	1 0 1 1 0 1 0 1	B5	1	1	(F1) $\rightarrow$ (F1)
	MOV A, Rr	1 1 1 1 1 r ₂ r ₁ r ₀	F8~FF Byte 2	1	1	(A) $\rightarrow$ (Rr)
	MOV A, @Rr	1 1 1 1 0 0 0 r ₀	F0~F1	1	1	(A) $\rightarrow$ ((Rr))
	MOVA, #data	0 0 1 0 0 0 1 1 d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	23 Byte 2	2	2	(A) $\rightarrow$ data

LIST OF INSTRUCTIONS (CONT.)

Classi- fication	Mnemonic	Instruction Code D ₇ D ₆ D ₅ D ₄ D ₃ D ₂ D ₁ D ₀	Hexa- decimal	Byte	Cycle	Description
Data transfer instructions	MOV Rr, A	1 0 1 0 1 r ₂ r ₁ r ₀	A8~AF	1	1	(Rr) ←(A)
	MOV @Rr, A	1 0 1 0 0 0 0 r ₀	A0~A1	1	1	((Rr)) ←(A)
	MOV Rr, #data	1 0 1 1 1 r ₂ r ₁ r ₀ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	B8~BF Byte 2	2	2	(Rr) ←data
	MOV @Rr, #data	1 0 1 1 0 0 0 r ₀ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	B0~B1 Byte 2	2	2	((Rr)) ←data
	MOV A, PSW	1 1 0 0 0 1 1 1	C7	1	1	(A) ←(PSW)
	MOV PSW, A	1 1 0 1 0 1 1 1	D7	1	1	(PSW) ←(A)
	XCH A, Rr	0 0 1 0 1 r ₂ r ₁ r ₀	28~2F	1	1	(A) ↔(Rr)
	XCH A, @Rr	0 0 1 0 0 0 0 r ₀	20~21	1	1	(A) ↔((Rr))
	XCHD A, @Rr	0 0 1 1 0 0 0 r ₀	30~31	1	1	(A _{0~3}) ↔((Rr _{0~3}))
	MOVX A, @Rr	1 0 0 0 0 0 0 r ₀	80~81	1	2	(A) ←((Rr)) External RAM
	MOVX @Rr, A	1 0 0 1 0 0 0 r ₀	90~91	1	2	((Rr)) ←(A) External RAM
	MOVP A, @A	1 0 1 0 0 0 1 1	A3	1	2	(A) ←((PC _{0~10} , A))
	MOVP3 A, @A	1 1 1 0 0 0 1 1	E3	1	2	(A) ←((PC ₀₁₁ , A))
	MOVP1 P, @R3	1 1 0 0 0 0 1 1	C3	1	2	(P1) ←(((PC _{0~7}) ←((R3))))
	MOV P1, @R3	1 1 1 1 0 0 1 1	F3	1	2	(P1) ←((R3))
Control instructions	MOV A, P1	0 1 1 0 0 0 1 1	63	1	1	(A) ←(P1) Latch data
	MOV A, P2	0 1 1 1 0 0 1 1	73	1	1	(A) ←(P2) Latch data
	ENTCNTI	0 0 1 0 0 1 0 1	25	1	1	TINT Enable F/F ←1
	DISTCNTI	0 0 1 1 0 1 0 1	35	1	1	TINT Enable F/F ←0
	ENI	0 0 0 0 0 1 0 1	05	1	1	EXINT Enable F/F ←1
	DISI	0 0 0 1 0 1 0 1	15	1	1	EXINT Enable F/F ←0
	SEL RB0	1 1 0 0 0 1 0 1	C5	1	1	(BS) ←0
	SEL RB1	1 1 0 1 0 1 0 1	D5	1	1	(BS) ←1
	SEL MB0	1 1 1 0 0 1 0 1	E5	1	1	(DBF) ←0
	SEL MB1	1 1 1 1 0 1 0 1	F5	1	1	(DBF) ←1
	ENT0CLK	0 1 1 1 0 1 0 1	75	1	1	T0 ←1/3 XTAL 1
	FLT	1 0 1 0 0 0 1 0	A2	1	1	P1, P2, BUS Floating
	FLTT	1 1 0 0 0 0 1 0	C2	1	1	CPU Output Signal Floating
	FRES	1 1 1 0 0 0 1 0	E2	1	1	FLT, FLTT RESET
	HLT	0 0 0 0 0 0 0 1	01	1	1	CPU Control Clock Stop
Timer/counter instructions	HALTS	1 0 0 0 0 0 1 0	82	1	1	XTAL 1/2 Stop
	MOV A, T	0 1 0 0 0 0 1 0	42	1	1	(A) ←(T)
	MOV T, A	0 1 1 0 0 0 1 0	62	1	1	(T) ←(A)
	STRT T	0 1 0 1 0 1 0 1	55	1	1	(T) ←[+32]←[+15]←XTAL
	STRT CNT	0 1 0 0 0 1 0 1	45	1	1	(T) ←T1 Clock
	STOPT CNT	0 1 1 0 0 1 0 1	65	1	1	(T) Count Stop
Other instruc- tion	NOP	0 0 0 0 0 0 0 0	00	1	1	(PC) ←(PC) + 1

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Limits	Unit
Supply Voltage	V_{CC}	$T_a = 25^{\circ}\text{C}$	-0.3 to 7	V
Input Voltage	V_I	$T_a = 25^{\circ}\text{C}$	-0.3 to V_{CC}	V
Storage Temperature	T_{stg}		-55 to +150	$^{\circ}\text{C}$

OPERATING RANGE

Parameter	Symbol	Conditions	Limits	Unit
Supply Voltage	V_{CC}	$f_{osc} = \text{DC} \sim 11 \text{ MHz}^*$	+2.5 to +6	V
RAM Retention Voltage	V_{CC}		+2 to +6	V
Ambient Temperature	T_A		-40 to +85	$^{\circ}\text{C}$
Fan Out	N	MOS load	10	
		TTL load	1	

- * 11 MHz version of MSM80C50 ($6 \text{ MHz} < \text{XTAL1.2} < 11 \text{ MHz}$) is under development.

DC ELECTRICAL CHARACTERISTICS

($V_{CC} = 5V \pm 10\%$, $T_a = -40$ to $+85^\circ\text{C}$)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Measuring Circuit
"L" Input Voltage	V_{IL}		-0.3		0.8	V	1
"H" Input Voltage (1)	V_{IH}		2.2		V_{CC}	V	
"H" Input Voltage (2)	V_{IH}		3.8		V_{CC}	V	
"L" Output Voltage (3)	V_{OL}	$I_{OL} = 2 \text{ mA}$			0.45	V	
"L" Output Voltage (4)	V_{OL}	$I_{OL} = 1.6 \text{ mA}$			0.45	V	
"H" Output Voltage (3)	V_{OH}	$I_{OH} = 400 \mu\text{A}$	2.4			V	
"H" Output Voltage (4)	V_{OH}	$I_{OH} = 50 \mu\text{A}$	2.4			V	
"H" Output Voltage (3)	V_{OH}	$I_{OH} = 20 \mu\text{A}$	4.2			V	
"H" Output Voltage (4)	V_{OH}	$I_{OH} = 10 \mu\text{A}$	4.2			V	
Input Leak Current	I_{IL}	$V_{SS} \leq V_{IN} \leq V_{CC}$			± 10	μA	2
Output Leak Current (5)	I_{OL}	$V_{SS} \leq V_O \leq V_{CC}$			± 10	μA	3
RESET Pull up Resistance	R_R	$V_{IN} \geq V_{IH} / V_{IN} \leq V_{IL}$	20/500		50/750	$k\Omega$	2
SS Pull up Resistance (6)	R_{SS}	Oscillation stop/oscillation	20/200		50/500	$k\Omega$	
P1, P2 Pull up Resistance	$R_{P1, P2}$	$V_{IN} \geq V_{IH} / V_{IN} \leq V_{IL}$	5/75		15/150	$k\Omega$	3
Power Supply Current	I_{CC}	At hardware power down $V_{CC}=2V$ ($T_a = +25^\circ\text{C}$) (7)		1	10	μA	4
		At HLTS execution * $V_{CC}=2V$ ($T_a = +25^\circ\text{C}$) (7)		1	10	μA	
		At HALT (6 MHz)		1.5	3	mA	
		At HALT (11 MHz)		2.5	5	mA	
		At execution (6 MHz)		5	10	mA	
		At execution (11 MHz)		10	20	mA	

Notes: (1) This does not apply to RESET, XTAL1, XTAL2, and V_{DD} .

(2) RESET, XTAL1, XTAL2, V_{DD}

(3) BUS, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE

(4) Other outputs

(5) High-impedance state

(6) This operates as a pull-down resistor when the oscillation is stopped in the HLTS or hardware power-down mode and as a pull-up resistor in other states.

(7) This does not contain flow out current from I/O Ports and Signal pins.

AC CHARACTERISTICS

($V_{CC} = 5V \pm 10\%$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Parameter	Symbol	Limits				Unit
		11 MHz Clock		Variable Clock (0 – 11 MHz)		
		Min.	Max.	Min.	Max.	
Cycle Time	t _{CY}	1.36		1.36		μS
ALE Pulse Width	t _{LL}	150		7/30t _{CY} –165		ns
Address Set up ALE	t _{AL}	70		2/15t _{CY} –110		ns
Address Hold from ALE	t _{LA}	50		1/15t _{CY} –40		ns
Bus Port Latch Data Setup to ALE	t _{BL}	110		5/30t _{CY} –115		ns
Bus Port Latch Data Hold from ALE	t _{LB}	90		3/30t _{CY} –45		ns
Control Pulse Width (PSEN, RD, and WR)	t _{CC}	300		6/15t _{CY} –245		ns
Data Setup before WR	t _{DW}	250		6/15t _{CY} –295		ns
Data Hold after WR	t _{WD}	40		2/15t _{CY} –140		ns
Data Hold after RD	t _{DR}	0	100	0	100	ns
PSEN, RD to Data-in	t _{RD}		200		5/15t _{CY} –250	ns
Address Setup to WR	t _{AW}	200		6/15t _{CY} –345		ns
Address Setup to Data-in	t _{AD}		400		8/15t _{CY} –325	ns
Address Float to RD, PSEN	t _{AFC}	0		0		ns
Port Control Setup to PROG	t _{CP}	100		2/15t _{CY} –80		ns
Port Control Hold from PROG	t _{PC}	60		4/15t _{CY} –300		ns
PROG to P2 Input Valid	t _{PR}	–	650		9/15t _{CY} –165	ns
Output Data Setup	t _{DP}	200		6/15t _{CY} –345		ns
Output Data Hold	t _{PD}	20		3/15t _{CY} –250		ns
Input Data Hold from PROG	t _{PF}	0	150	0	150	ns
PROG Pulse Width	t _{PP}	700		10/15t _{CY} –205		ns
Port 2 I/O Setup to ALE	t _{PL}	150		9/30t _{CY} –255		ns
Port 2 I/O Hold from ALE	t _{LP}	20		3/30t _{CY} –115		ns

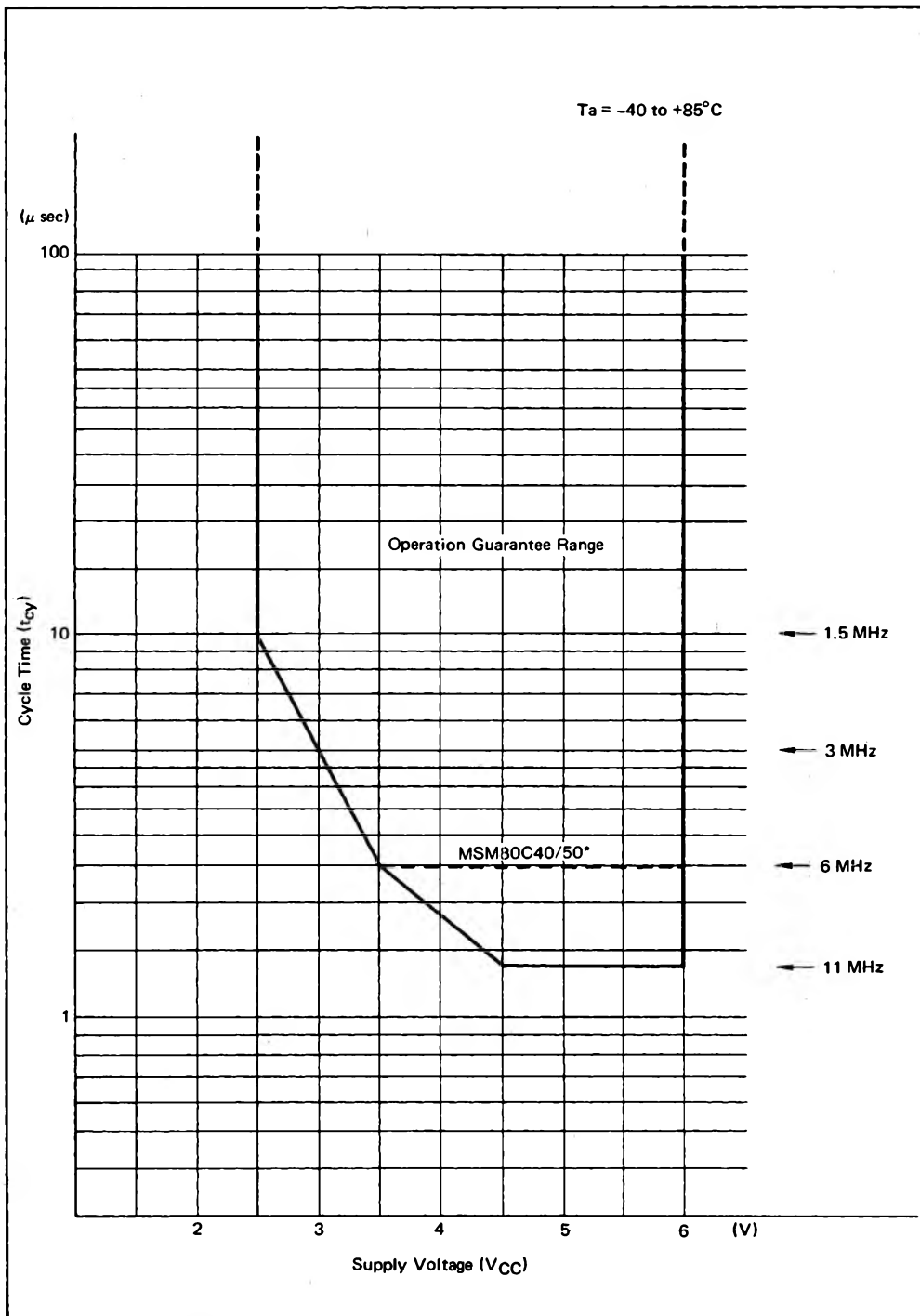
Note: Control output:

Bus output:

$C_L = 80 \text{ pF}$

$C_L = 150 \text{ pF}$ [for 20 pF (t_{WD})]

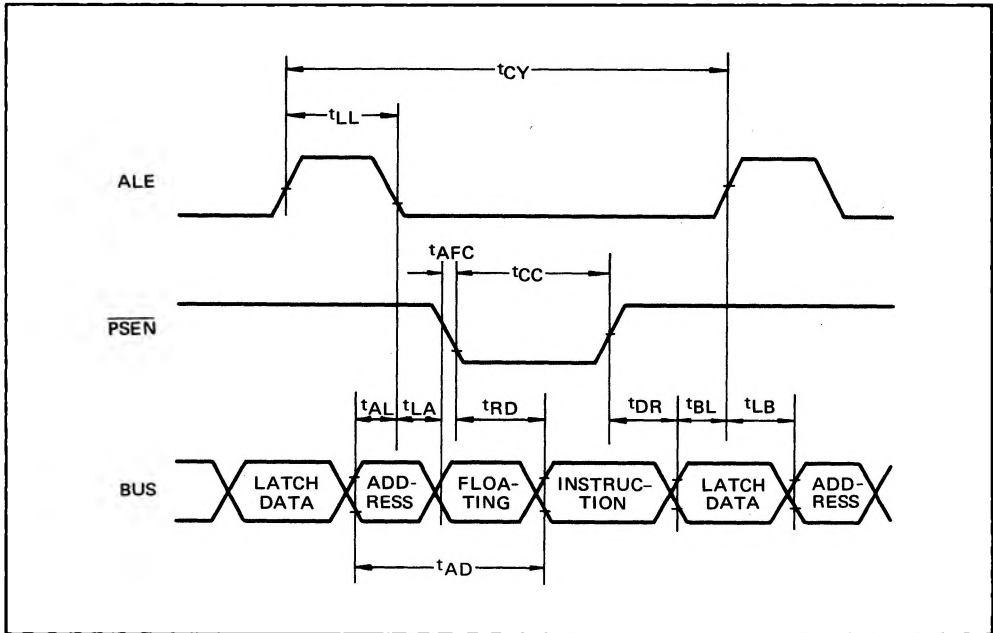
MSM80C49 OPERATION GUARANTEE RANGE



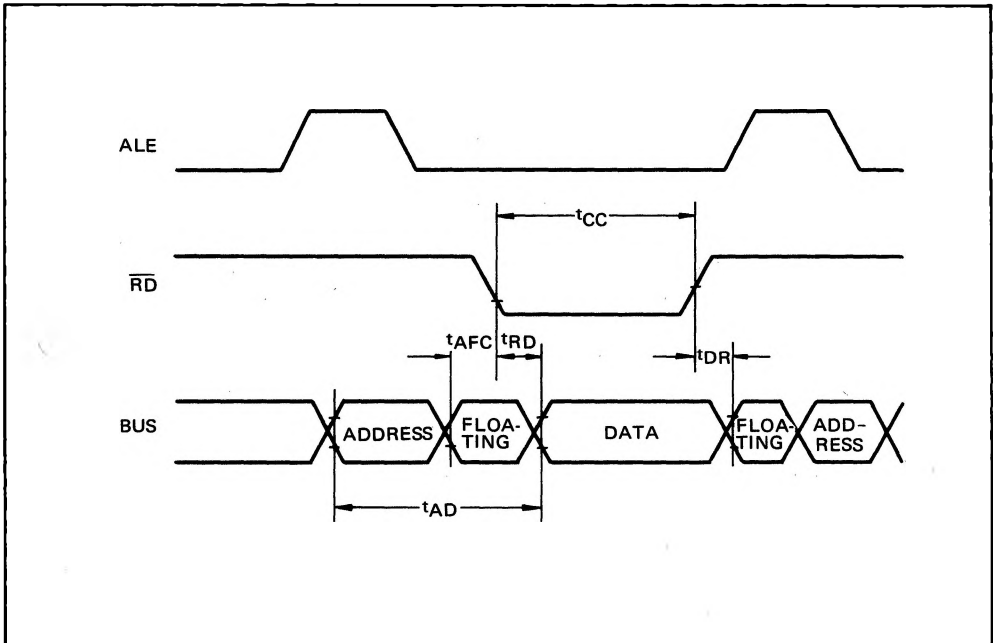
* 11 MHz version of MSM80C40/50 is under development

TIMING CHART

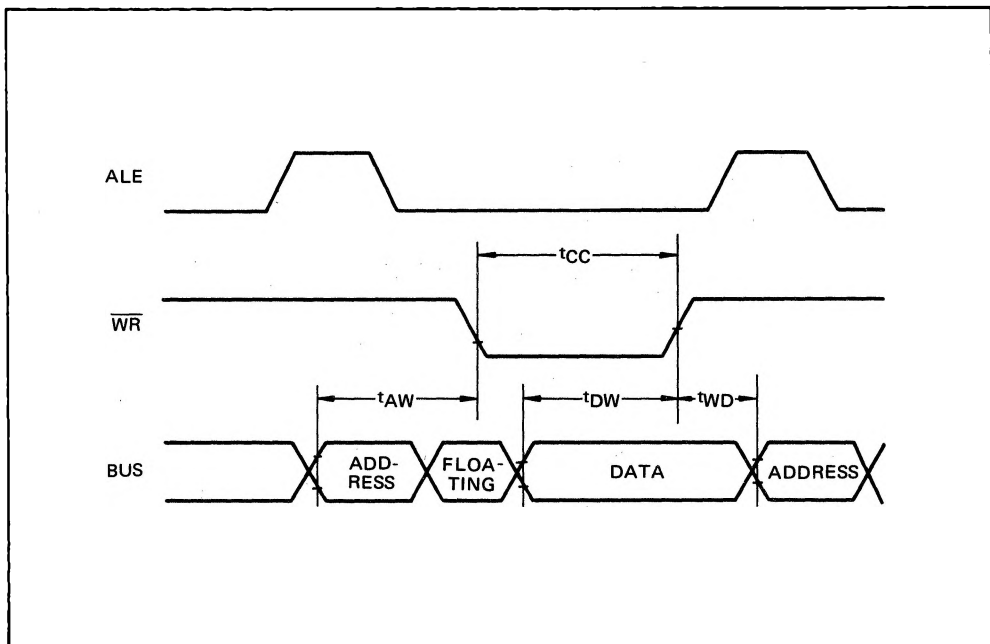
Instruction Fetch (from external program memory)



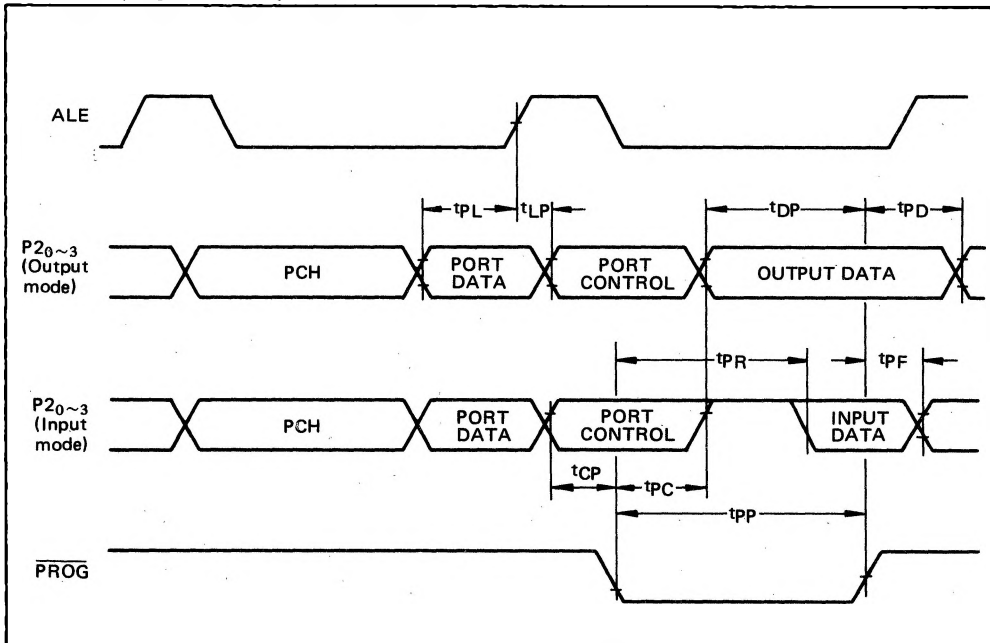
Read (from external data memory)



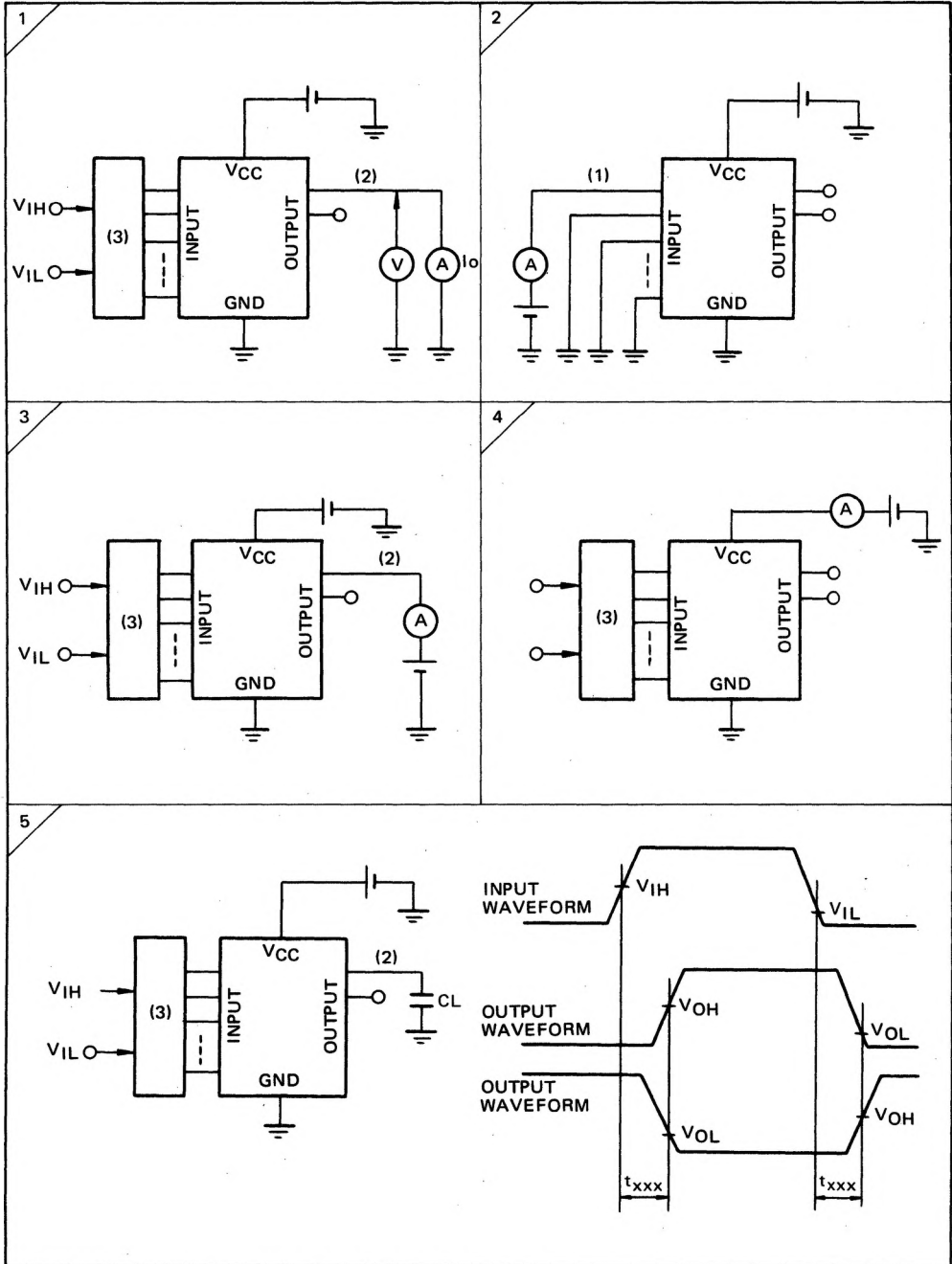
Write (to external memory)



4 low-order bits input/output of port 2 when expanded I/O is used
(in external program memory access mode)



MEASUREMENT CIRCUIT



Notes: (1) This is repeated for each specified input pin.
 (2) This is repeated for each specified output pin.
 (3) Input logic for setting the specified state.