OKI semiconductor

MSM6502/6512

CMOS 4 BIT SINGLE CHIP MICROCONTROLLER WITH LCD DRIVER

GENERAL DESCRIPTION

The OKI MSM6502/6512 is a low-power, high-performance 4 bit single-chip microcontroller implemented in complementary metal oxide semiconductor technology.

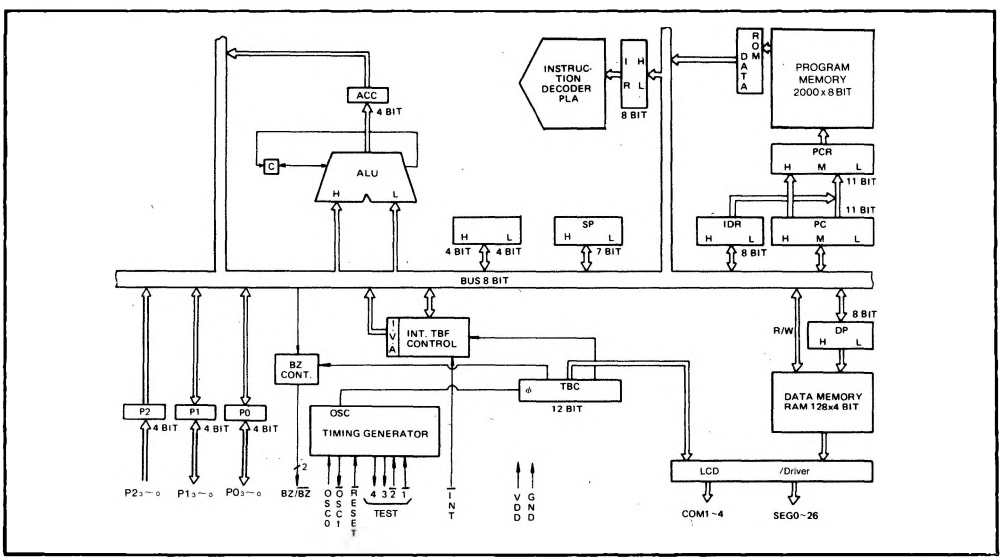
Integrated within this one chip is a 108 (4×27) dot LCD Driver. Also integrated in this chip are 16K bits of mask program ROM, 512 bits of data RAM, Input/Output lines, a programmable timer/counter, and oscillator.

The advantages of the MSM6502/6512 in comparison with the OLMS-40 Series include, among other features, a lower drive voltage, multiplexed interrupts, a larger number of drivable liquid crystal elements, a buzzer output, and larger memories.

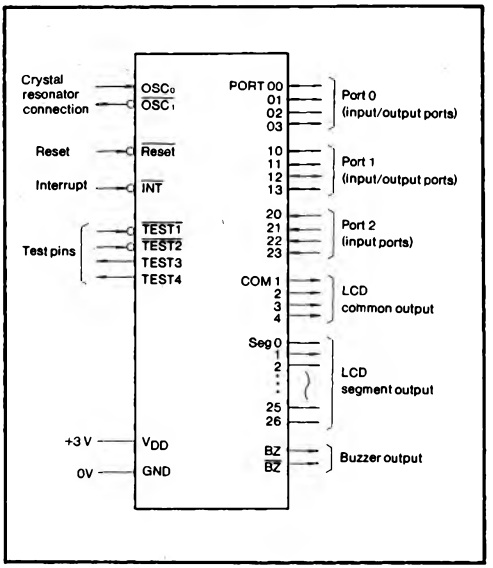
FEATURES

- ROM : 2000 × 8 bit
- RAM : 128 × 4 bit
- Number of Instructions : 68
- Clock Oscillation : Crystal 32.768 kHz
- Cycle Time : 91.5 μs
- Timer Interrupt : Dual (16 & 128 Hz)
- I/O Ports : 4 bit × 2 Port
- Input ports : 4 bit × 1 Port
- LCD Drive : 108 (4×27) picture elements
- Buzzer : 2K/1K/512 Hz/Soft
- Interrupt : Three types (external, two timer types)
- Stack : Nesting RAM stack pointer = 7 bits
- Power down : Halt mode available
- Operating power supply voltage : 2.4V – 3.6V
- Consumption current (V_{DD}=3V, OSC = 32.768 kHz)
  MSM6502 : 45μA (Typical), 30μA (Halt mode)
  MSM6512 : 30μA (Typical), 12μA (Halt mode)
- Package : 56 pin FLAT (Small type)

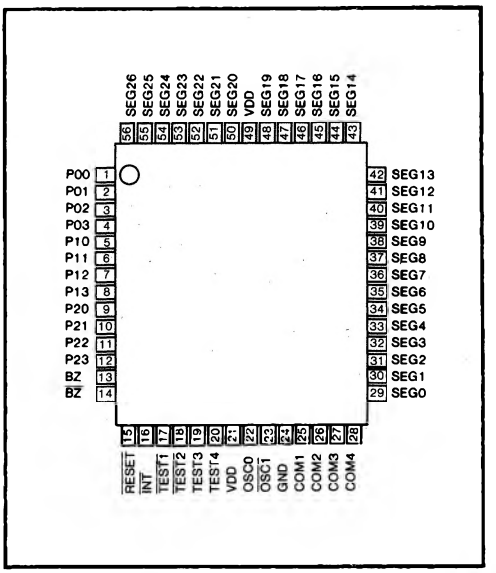
FUNCTIONAL BLOCK DIAGRAM



LOGIC SYMBOL



PIN CONFIGURATION (TOP VIEW)



PIN DESCRIPTION

Designation	Pin No.	Function
GND	24	Circuit GND potential
V_{DD}	21, 49	Main power source
OSC_0	22	Crystal OSC input, internal clock input
$\overline{OSC_1}$	23	Crystal OSC input, internal clock output
P0, P1	1 to 4 5 to 8	Pseudo-bidirectional ports for 4-bits parallel I/O. To input data from these ports, it is necessary to write "1" beforehand. The port to be selected is specified by the L register. The register contents and the corresponding specified ports are listed below. Content of L register / Port Specified 0.8 / P0 1.9 / P1 2.0 AH / P2 3.0 BH / P3 4.0 CH / P4 5.0 DH / P5 6.7.0EH. OFH / No designation Note: P3, P4, P5 are internal ports.
P2	9 to 12	Input ports for 4-bit parallel input with no latching function.
$\overline{INT}$	16	Input pin to request an interrupt from the external circuit. The input flag is set by the fall of the input signal.

Designation	Pin No.	Function
$\overline{\text{RESET}}$	15	The reset mode starts after "0" is input to the $\overline{\text{RESET}}$ pin for more than 2 machine cycles. The reset signal has priority over all of other signals and performs the following operations automatically: (1) Resets all bits of the PC (Program counter) to "0". (2) Sets all bits of the parallel I/O ports (P00 to P13) to "1". (3) Resets the internal resister (H, L, ACC, C, P3, P4, P5). (4) Resets the skip flag. (5) Resets all bits of the time base counter (TBC). (6) Resets the interrupt request flag (IRQF). (7) Resets the interrupt enable flag (EIF). (8) Resets the master interrupt enable flag (MEIF). (9) Sets all bits of the stack pointer (SP) to "1". (10) Initializes the segment and common outputs. (11) Sets all bits of the index register (IDR) to "1". Since the $\overline{\text{RESET}}$ pin is pulled up to V_{DD} by an internal resister (approx. 800 kΩ), it is possible to achieve power ON/reset by connecting it with an external capacitor.
LCD Drive Pins SEG 0 ~ 26 COM 1 ~ 4	29 to 48 50 to 56 25 to 28	A special AC waveform designed to comply with liquid crystal properties is required for liquid crystal drive purpose. The MSM6502B is equipped with a 1/4 duty 1/3 bias liquid crystal drive circuit with four common output ports and 27 segments to enable displays of 108 picture elements. On/off selection of picture element displays involves writing "0" or "1" in the corresponding bits in the RAM 00H to thru 1AH display area, and subsequent automatic hardware controlled display. The frame frequency is 64 Hz.
BZ/$\overline{\text{BZ}}$	13, 14	BZ and $\overline{\text{BZ}}$ are used in the generation of alarms and other sounds. The selectable frequencies include three hardware frequencies (TBC output) 512, 1024, and 2048 Hz, and a software type based on P50 data. These frequencies are selected at P3. When one of the hardware frequencies is selected by P3, output of that frequency is continuous. But selection of the software type results in output of P50 contents to generate a melody by program.

INSTRUCTION LIST

Grouping	Mnemonic	Code	Byte	Cycle	Function
Load	LAI n	8n	1	1	Acc ← n
	LLI n	7n	1	1	L ← n
	LHLI n8	6A n8	2	2	HL ← n8
	LXI n8	69 n8	2	2	X ← n8
	LAM	B0	1	1	Acc ← M<HL>
	LAL	B1	1	1	Acc ← L
	LAH	B2	1	1	Acc ← H
	LMA	B4	1	1	M<HL> ← Acc
	LLA	B5	1	1	L ← Acc
	LHA	B6	1	1	H ← Acc
	LMAD m7	1B m7	2	2	M<m7> ← Acc

INSTRUCTION LIST (CONT.)

Grouping	Mnemonic	Code	Byte	Cycle	Function
Load	LAMD m7	1A m7	2	2	Acc ← M<m7>
	LMT	67	1	2	M<HL+1><HL> ← ROM<X>
	PUSH HL	BC	1	2	STACK ← HL, SP ← SP−2
	PUSH CA	BD	1	2	STACK ← C, Acc, SP ← SP−2
	POP HL	BE	1	2	HL ← STACK, SP ← SP+2
	POP CA	BF	1	2	C, Acc ← STACK, SP ← SP+2
Exchange	XAM	B8	1	1	Acc ⟷ M<HL>
	XAMD m7	1C m7	2	2	Acc ⟷ M<m7>
	XHS	3F	1	1	HL ⟷ SP
Increment and decrement	INA	10	1	1	Acc ← Acc + 1, Skip if Acc=0
	INL	11	1	1	L ← L+1, Skip if L=0
	INM	12	1	1	M<HL> ← M<HL> +1, Skip if M<HL> = 0
	INX	5C	1	1	X ← X + 1
	DCA	14	1	1	Acc ← Acc−1, Skip if Acc=F
	DCL	15	1	1	L ← L − 1 Skip if L=F
	DCM	16	1	1	M<HL> ← M<HL> −1, Skip if M<HL> = F
	DCX	5D	1	1	X ← X − 1
Operation	DSC	60	1	1	C,Acc ← C+Acc+$\overline{M}$<HL>, Adjust if C=0
	DAC	61	1	1	C,Acc ← C+Acc+(M<HL> +6), Adjust if C=0
	ADS	62	1	1	Acc ← Acc+M<HL>, Skip if Cy=1
	ADCS	63	1	1	C,Acc ← C+Acc+M<HL>, Skip if C=1
	AIS n	0n	1	1	Acc ← Acc+n, Skip if Cy=1
	CMA	65	1	1	Acc ← $\overline{Acc}$
	EOR	66	1	1	Acc ← Acc∀M<HL>
	AND	4C	1	1	Acc ← Acc∧M<HL>
	OR	4D	1	1	Acc ← Acc∨M<HL>
	CAM	6B	1	1	Skip if Acc = M<HL>
	CPAL	6C	1	1	Skip if Acc = L
	CAXL	6D	1	1	Skip if Acc = XL
	CAXH	6E	1	1	Skip if Acc = XH
	SC	1F	1	1	C ← "1"
	RC	1E	1	1	C ← "0"
	TC	4E	1	1	Skip if C= "1"

INSTRUCTION LIST (CONT.)

Grouping	Mnemonic	Code	Byte	Cycle	Function
Operation	RAL	18	1	1	(*) ← C ← Acc 3←2←1←0 ← (*)
	RAR	19	1	1	(*) → C → Acc 3→2→1→0 → (*)
Bit Operation	SMB n2	30 ~ 33	1	1	M<HL> bit n2 ← "1"
	SMBD m7, n2	50 (m7) ~ 53 (m7)	2	2	M<m7> bit n2 ← "1"
	SPB n2	20 ~ 23	1	1	P bit n2 ← "1"
	RMB n2	34 ~ 37	1	1	M<HL> bit n2 ← "0"
	RMBD m7, n2	54 (m7) ~ 57 (m7)	2	2	M<m7> bit n2 ← "0"
	RPB n2	24 ~ 27	1	1	P bit n2 ← "0"
	TMB n2	38 ~ 3B	1	1	Skip if M<HL> bit n2 = "1"
	TMBD m7, n2	58 (m7) ~ 5B (m7)	2	2	Skip if M<m7> bit n2 = "1"
	TPB n2	28 ~ 2B	1	1	Skip if P bit n2 = "1"
	TAB n2	2C ~ 2F	1	1	Skip if Acc bit n2 = "1"
	TIRB n2	49 ~ 4B	1	1	if IRQF bit n2="1" Skip & IRQF bit n2 ← "0"
Interrupt	EI	5E	1	1	MEIF ← "1"
	DI	5F	1	1	MEIF ← "0"
Branch	J a11	9000~97CF	2	2	$PC_{10 \sim 0}$ ← a11
	CAL a11	A000~A7CF	2	3	STACK←PC+2, SP←SP-3, $PC_{10 \sim 0}$ ← a11
	JCP a6	C0~FF	1	1	$PC_{5 \sim 0}$ ← a6
	RT	3C	1	2	PC ← STACK, SP←SP+3
	RTS	3D	1	1	PC ← STACK, SP←SP+3, then Skip
Input/ Output	IP	B3	1	1	Acc ← P
	OP	B7	1	1	P ← Acc
CPU Control	HALT	4F	1	1	HLF ← "1"
	NOP	00	1	1	No Operation

ELECTRICAL CHARACTERISTIC

ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Conditions	Limits	Unit
Power Supply Voltage	V_{DD}	Ta = 25°C	−0.3 ~ 7	V
Input Voltage	V_I		−0.3 ~ V_{DD}	V
Output Voltage	Vo		−0.3 ~ V_{DD}	V
Power Dissipation	P_D	Ta = 25°C per package	200	mV
StorageTemperature	Tstg	—	−55 ~ +150	°C

OPERATING RANGE

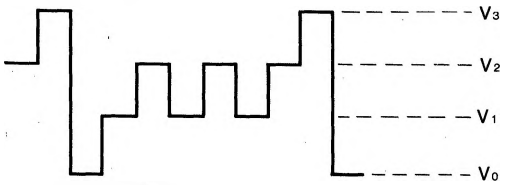
Parameter	Symbol	Conditions	Limits	Unit
Power Supply Voltage	V_{DD}	f(osc)=32.768 kHz	2.4 ~ 3.6	V
Operating Temperature	Top	—	−20 ~ +70	°C

D.C. CHARACTERISTICS

(V_{DD} = 3V, Ta = −20 ~ +70°C)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
"H" Input Voltage	V_{IH}	–		2.6	–	–	V
"L" Input Voltage	V_{IL}	–		–	–	0.4	V
"H" Output Voltage(1)	V_{OH}	I_O = −1.0 mA		2.0	–	–	V
"L" Output Voltage(2)	V_{OL}	I_O = 1.0 mA		–	–	1.0	V
LCD Drive Output Voltage(3)	V_3	MSM6502	I_O = −5 μA	2.8	–	3.0	V
		MSM6512	I_O = −2 μA				
	V_2	MSM6502	I_O = ±2 μA	1.8	–	2.2	V
		MSM6512	I_O = ±0.5 μA				
	V_1	MSM6502	I_O = ±2 μA	0.8	–	1.2	V
		MSM6512	I_O = ±0.5 μA				
	V_0	MSM6502	I_O = 5μA	0.0	–	0.2	V
		MSM6512	I_O = ±2 μA				
OSC_0 Input Current	I_{IH}/I_{IL}	$V_I = V_{DD}/V_I = 0V$		–	–	2/−2	μA
Input Current(4)	I_{IH}/I_{IL}	$V_I = V_{DD}/V_I = 0V$		–	–	1/−10	μA
Input Current(5)	I_{IH}/I_{IL}	$V_I = V_{DD}/V_I = 0V$		–	–	1000/−1	μA
Input Current(6)	I_{IH}/I_{IL}	$V_I = V_{DD}/V_I = 0V$		–	–	1/−40	μA
P0, P1 "H" Output Current	I_{OH}	V_o = 0 V		–	–	−50	μA
Current Consumption	I_{DD}	MSM6502	f(osc) = 32.768 kHz at no load	–	45	70	μA
		MSM6512		–	30	55	
	I_{DDHLT}	MSM6502	f(osc) = 32.768 kHz at HLT execution	–	30	40	μA
		MSM6512		–	12	25	
	I_{DDS}	MSM6502	Statis	–	15	25	μA
		MSM6512		–	5	15	
Oscillation Start Time	T_{OSC}	–		–	–	10	SEC

(1) Applied to BZ, $\overline{BZ}$
(2) Applied to BZ, $\overline{BZ}$, P0, P1
(3) Applied to COMMON, SEGMENT



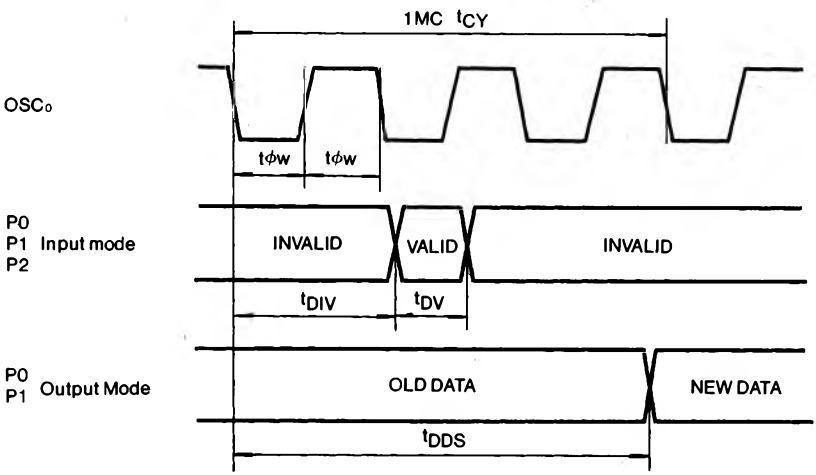
(4) Applied to $\overline{RESET}$, $\overline{INT}$
(5) Applied to P2 (When input is unable)
(6) Applied to P2 (When input is able)

SWITCHING CHARACTERISTIC

(V_{DD} = 3V, Ta = −20 ~ +70°C)

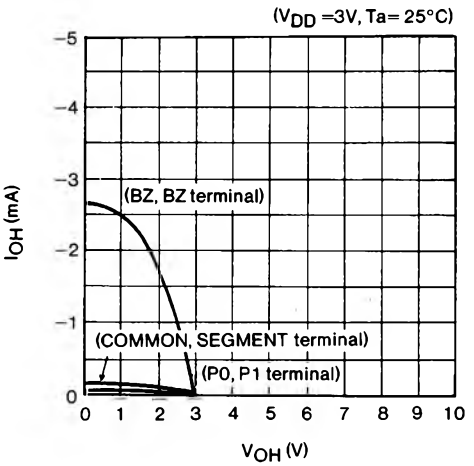
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Clock (OSC_0) Pulse Width	$t\phi W$	–	15	–	–	μS
Cycle Time	t_{CY}	–	(1)	–	–	μS
P0 P1 P2 Data Valid Time	t_{DV}	–	(2)	–	–	μS
P0 P1 P2 Data Invalid Time	t_{DIV}	–	–	–	(3)	μS
P0 P1 Data Delay Time	t_{DDS}	C_L = 50 pF	–	–	(4)	μS

(1) $t_{CY} = 3 \times 1/f(osc)$
(2) $t_{DV} = 1/2 \times 1/f(osc)$
(3) $t_{DIV} = 1 \times 1/f(osc) + 10\mu S$
(4) $t_{DDS} = 5/2 \times 1/f(osc) + 15\mu S$

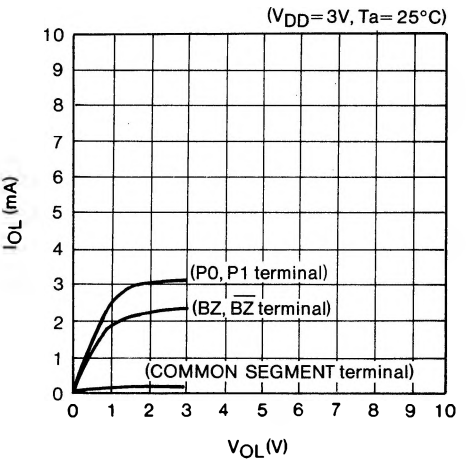


TYPICAL PERFORMANCE CURVES for MSM6502

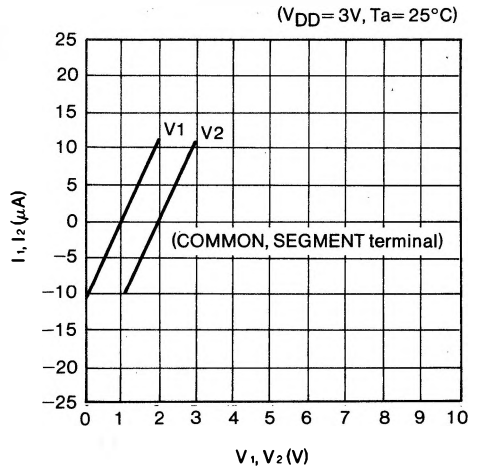
High-level Output Current (I_{OH}) – Output Voltage (V_{OH})



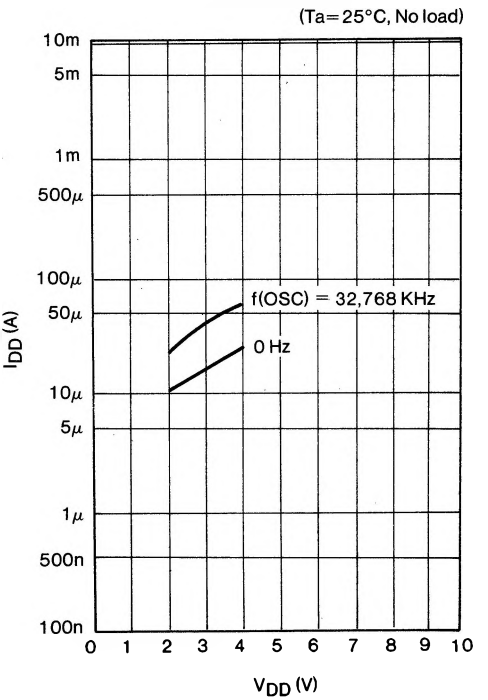
Low-level Output Current (I_{OL}) – Output Voltage (V_{OL})



Middle-level Output Current (I1, I2) – Output Voltage (V1, V2)

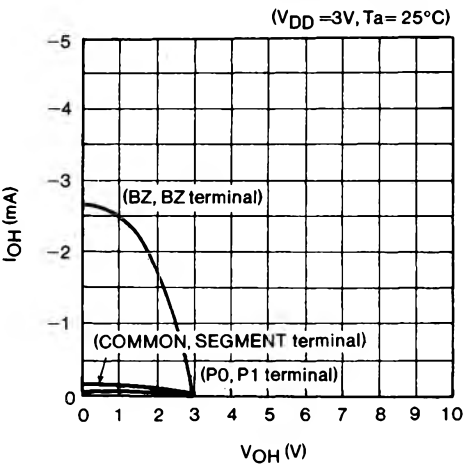


Current Consumption (I_{DD}) – Power Supply Voltage (V_{DD})

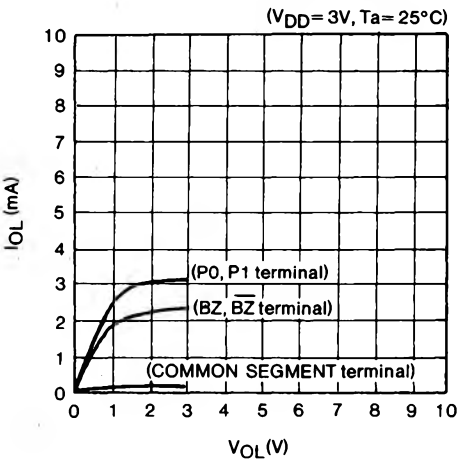


TYPICAL PERFORMANCE CURVES for MSM6512

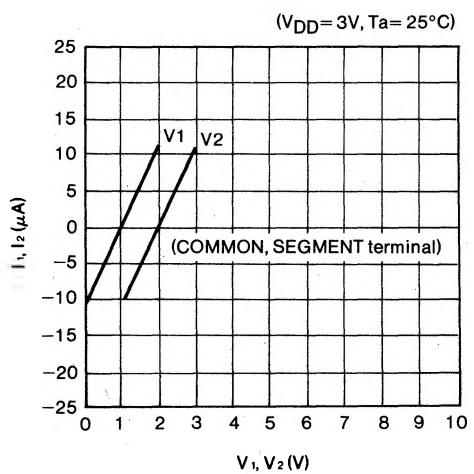
High-level Output Current (I_{OH}) – Output Voltage (V_{OH})



Low-level Output Current (I_{OL}) – Output Voltage (V_{OL})



Middle-level Output Current (I1, I2) – Output Voltage (V1, V2)



Current Consumption (I_{DD}) – Power Supply Voltage (V_{DD})