OKI semiconductor

MSM6442

CMOS 4-BIT SINGLE CHIP MICROCONTROLLER WITH LCD DRIVER

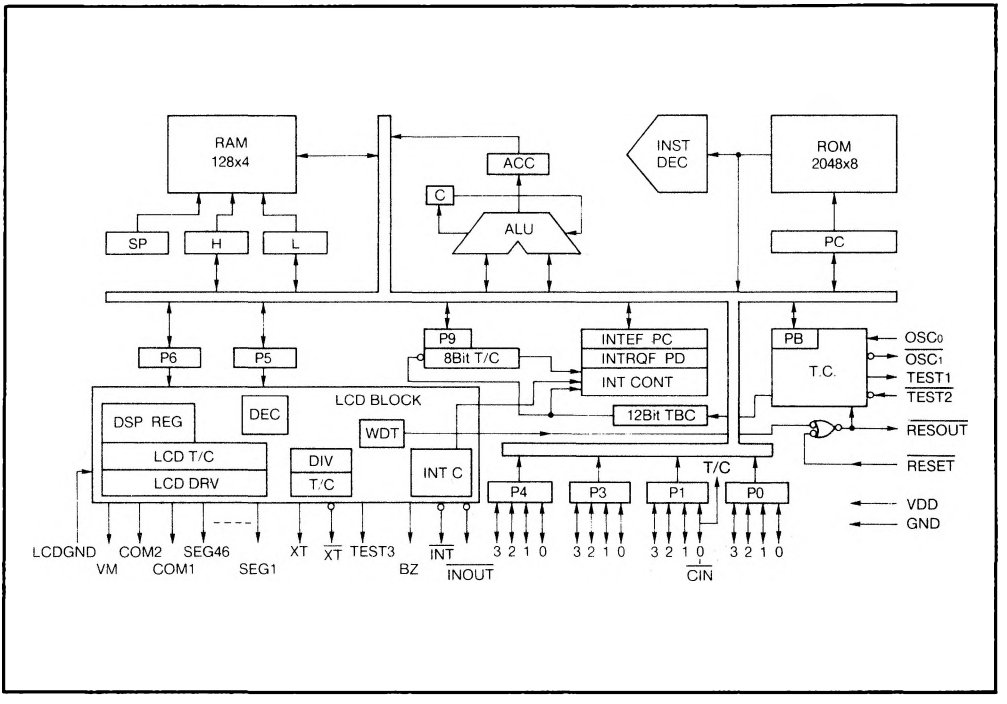
GENERAL DESCRIPTION

The OKI MSM6442 is a low power, high performance single chip device implemented in complementary metal oxide semiconductor technology with 46 segment outputs and 2 commons. Also integrated onto this chip are 16K bits mask program ROM, 512 bits of data RAM, 28 Input/Output lines and oscillator. 71 instructions include binary, BCD, logical operations; bit set, reset, test; subroutine call and return.

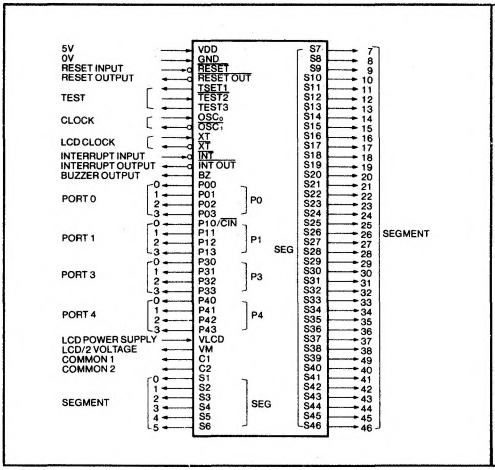
FEATURES

- Low Power Consumption 30mW (typ)
- 2048 × 8 Internal ROM
- 128 × 4 Internal RAM
- Two built-in counters
  12-bit time-base counter
  8-bit programable timer/event counter
- 16 Input/Output Ports and 46 LCD Output Port and 2 Common Output (1/2 Duty, 1/2 Bias)
- LED direct drive available
- Self-contained Oscillator
- 71 Instructions
- 4 Interrupt Levels
- 16 Stack Levels
- −40 to +85°C Operating Temperature
- 4.5 to 5.5V Operating V_{DD} at 4.2 MHz
  3.0 to 6.0V Operating V_{DD} at 1 MHz
- TTL Compatible

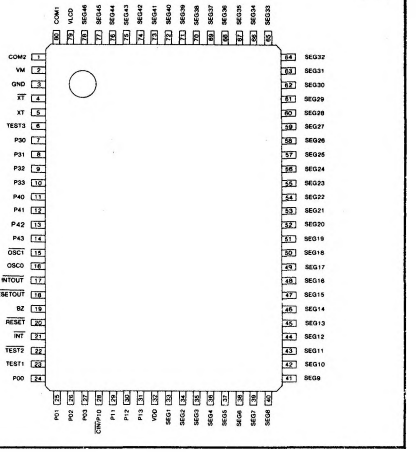
FUNCTIONAL BLOCK DIAGRAM



LOGIC SYMBOL



PIN CONFIGURATION (TOP VIEW)



PIN DESCRIPTION

Terminal	Input/ Output	Function	When reset
P00 ~ P03 P10 ~ P13 P30 ~ P33	Input/ Output	I/O port I/O port (P10 and count input $\overline{CIN}$ are in common) I/O port	"1"
P40 ~ P43	Input/ Output	I/O port	"0"
SEG1 ~ SEG16 SEG17 ~ SEG46	Output*	LCD output port (can be assigned to data output in 4 bit wide) LCD output port	"0"*
COM1 COM2	Output*	LCD common output terminal 1 LCD common output terminal 2	"0"*
$\overline{INT}$	Input	Input port of external interrupt	–
$\overline{INT\ OUT}$	Output	Interrupt output port	"1"
$\overline{RESET}$		Reset input port	–
$\overline{RESET\ OUT}$	Output	Reset output terminal	"1"
BZ	Output	Buzzer pulse output port in 2048 KHz	"0"*
$\overline{OSC_0}$ $\overline{OSC_1}$	Input/ Output	Crystal OSC or ceramic OSC connection Crystal OSC or ceramic OSC connection (System clock)	–
XT $\overline{XT}$	Input/ Output	32.768 kHz crystal oscillator connection (use for LCD control)	–
$\overline{TEST\ 1}$ $\overline{TEST\ 2}$ $\overline{TEST\ 3}$	–	TEST terminal 1 (open) (Connected to V_{DD}) TEST terminal 2 (open) TEST terminal 3 (open)	
V_{DD}	Input	Power supply (5V)	–
V_{LCD} GND	Input	Power supply for LCD	–
VM	Input/ Output	$(V_{DD}-V_{LCD})/2$ supply voltage output or supply voltage input	"0"*
GND	Input	Power supply (0V)	–

*"0" indicates the LCD GND voltage level

ELECTRIC CHARACTERISTICS

• Absolute Maximum Ratings

Parameter	Symbol	Conditions	Limits	Unit
Supply Voltage	V_{DD}	Ta = 25°C	−0.3 ~ 7	V
Input Voltage	V_I		−0.3 ~ V_{DD}	V
Output Voltage	V_O		−0.3 ~ V_{DD}	V
LCD Voltage	LCDGND		V_{DD} − 9 ~ V_{DD}	V
Storage Temperature	Tstg	—	−55 ~ +150	°C

• Operating Conditions

Parameter	Symbol	Conditions	Limits	Unit
Supply Voltage	V_{DD}	f (OSC) ≦ 1MHz	3 ~ 6	V
		f (OSC) ≦ 4.2MHz	4.5 ~ 5.5	V
LCD Voltage	LCDGND	*1	V_{DD} − 8 ~ 0	V
Memory Retension Voltage	V_{DDH}	Oscillation off	2 ~ 6	V
Operating Temperature	Top	—	−40 ~ +85	°C
LCD Clock Oscillation Frequency	f(XT)	*2	32.768	kHz
Fan Out (I/O Port)	N	MOS Load	15	—
		TTL Load	1	—

*1 Voltage applied to LCD is ($_{DD}$−V_{LCD}).

*2 Oscillation Circuit for LCD Clock (XT, $\overline{XT}$ Port) is for Christal Oscillation only.

DC CHARACTERISTICS

(VDD = 5V ±10%, LDCGND = 0V, Ta = −40 ~ +85°C)

Parameter		Symbol	Condition	MIN	TYP	MAX	Unit
"H" Input Voltage	*1. $\overline{INT}$	VIH	—	2.4	—	VDD	V
	*3.		—	3.6	—	VDD	V
"L" Input Voltage	*1. *4	VIL	—	0	—	0.8	V
"H" Output Voltage	*1. $\overline{OSC1}$	VOH	IO = −15μA	4.2	—	—	V
	*2.		IO = −400μA	2.4	—	—	V
	SEG1~SEG46		IO = −10μA	VDD-0.2	—	—	V
	COM1, COM2		IO = −50μA	VDD-0.2	—	—	V
"L" Output Voltage	*1, *2	VOL	IO = 1.6mA	—	—	0.4	V
	$\overline{OSC1}$		IO = 15mA	—	—	0.4	V
	SEG1~SEG46		IO = 10μA	—	—	0.2	V
	COM1, COM2		IO = 50μA	—	—	0.2	V
"M" Output Voltage	COM1, COM2	VOM	IO ±0.5	VDD/2 0.2	—	VDD/2+0.2	V
"H" Input Current	OSC0	IIH	VI= VDD	—	—	15	μA
	XT			—	—	7	μA
	$\overline{INT}$, $\overline{RESET}$			—	—	1	μA
"L" Input Current	OSC0	IIL	VI = 0V	—	—	−15	μA
	XT			—	—	7	μA
	$\overline{INT}$, $\overline{RESET}$			—	—	−30	μA
"H" Output Current	*1	IOH	VO = 2.4V	−0.1	—	—	mA
			VO = 0.4V	—	—	−1.2	mA
Current Consumption —at stop mode —no oscillation		IDDS	VDD = 2V, TA = 25°C No load Display off XT Port is fixed to "L"	—	0.2	10	μA
			Display off XT Port is fixed to "L"	—	1	100	μA
Current Consumption —at stop mode		IDDL	No load Display off At stop mode f(XT) = 32.768 KHz	—	100	200	μA
Current Consumption		IDD	No load Display off f(osc) = 4.2 MHz f(XT) = 32.768 KHz	—	6	12	mA

*1 Applied to P0, P1, P2, and P4.
*2 Applied to $\overline{INTOUT}$, $\overline{RESET}$, and BZ.
*3 Applied to OSC0, XT, and $\overline{RESET}$.
*4 Applied to XT, $\overline{INT}$, and $\overline{RESET}$.

Note: "M" output voltage is intermediate voltage of the output from common port at dynamic display.

AC CHARACTERISTICS

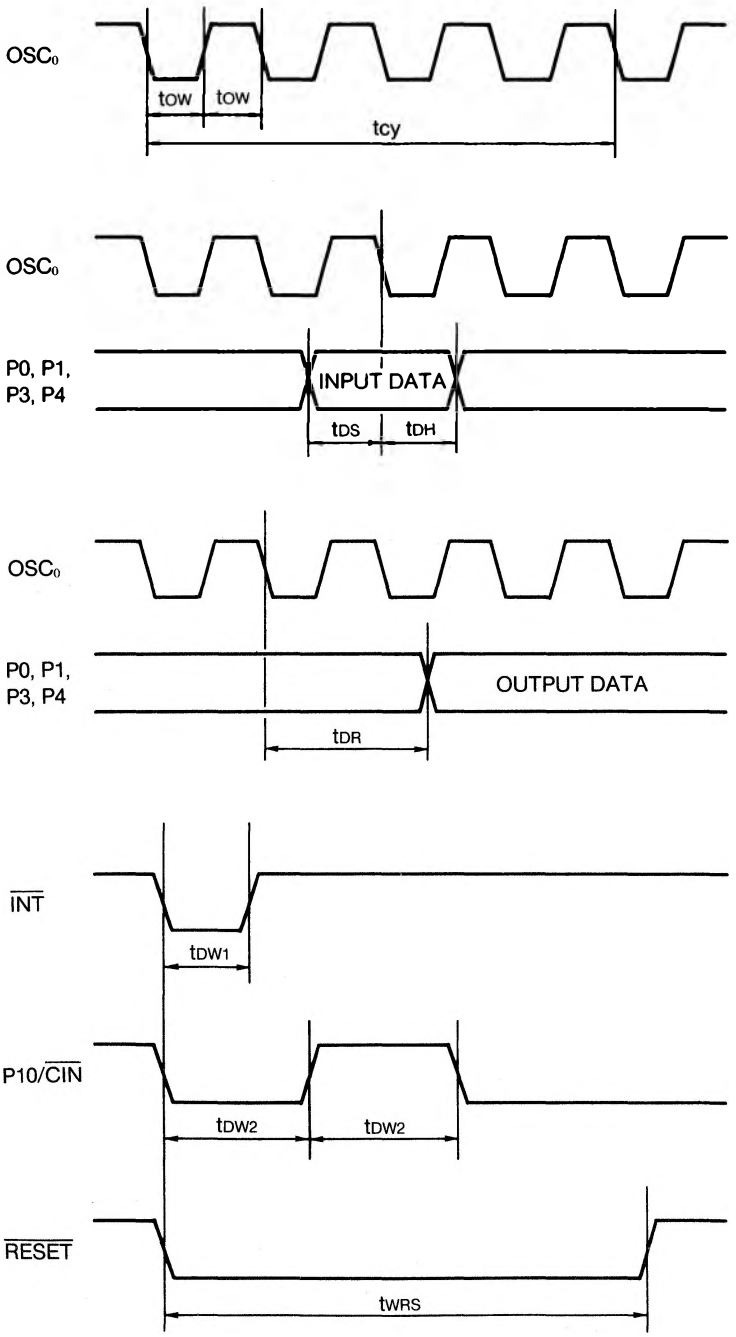
(VDD = 5V ±10%, Ta = −40 ~ +85°)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Clock (OSC_0) Pulse Width	t_{OW}	—	119	—	—	nS
Cycle Time	t_{CY}	—	952	—	—	nS
Input Data Set-up Time	t_{DS}	—	120	—	—	nS
Input Data Hold Time	t_{DH}	Note 1	120	—	—	nS
INT Input Data Pulse Width	t_{DW1}	—	120	—	—	nS
CT Clock Pulse Width	t_{DW2}	—	2/8tcy÷120	—	—	nS
Data Delay Time	t_{DR}	C_L = 15pF	—	—	300	nS
Reset Input Pulse Width	t_{WRS}	Note 2	2tcy	—	—	nS

Note 1* To release powerdown by inputting "L" level into INT Port, pulse width should be longer than the time for the oscillation stabilization at OSC_0.

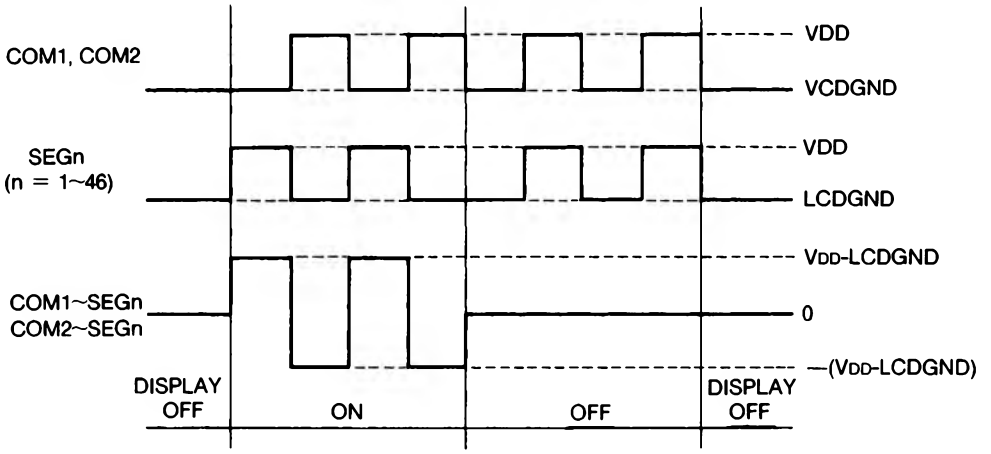
Note 2* The condition of stable oscillation. To release powerdown by reset, pulse width should be longer than the time for oscillation stabilization at OSC_0.

TIMING CHART

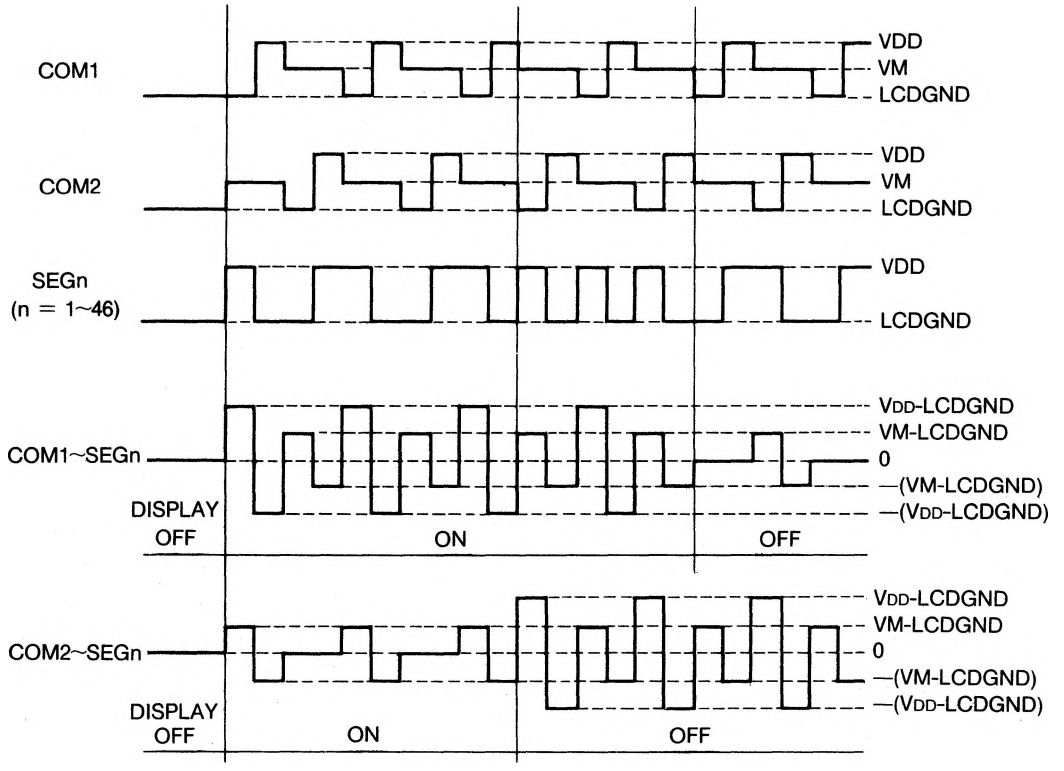


OUTPUT WAVE FORM OF LCD RIVER

STATIC MODE



DYNAMIC MODE



FUNCTIONAL DESCRIPTION

ROM

Organized into 2048 words by 8 bits, ROM is used to store developed application programs (instructions). It is addressed by the program counter (PC).

PROGRAM COUNTER (PC)

The program counter consists of a 11-bit binary counter. It is used to address ROM.

STACK

An interrupt or CAL instruction causes the contents of the PC to be saved in the stack. Also, the PUSH instruction causes the contents of accumulator, carry-flag, H- and L-register to be saved in it. These are allowed to be restored by the RT instruction or POP instruction.

RAM

Organized into 128 words of 4 bits, RAM is addressed by the H- and L-register or the contents of the second byte of an instruction.

L-REGISTER

A 4-bit register which specifies the row address of RAM and the port-address in the port operation instructions. It is also used as a working register.

H-REGISTER

A 4-bit register which specifies the column address of RAM and is used as a working register.

ALU

A 4-bit logic circuit which provides arithmetic and logical operations.

ACCUMULATOR (ACL)

Consisting of a 4-bit register, the accumulator holds the result of operations or the date present on ports.

C-FLAG

The flag that holds a carry generated from the result of operations.

INPUT/OUTPUT Ports (16 bits)

16 input/output ports are provided for effecting and controlling data transfer to and from an external source. The ports are selected by codes included in the instructions.

12-bit TIME-BASE COUNTER

The time base counter consists of a 12-bit binary counter. It is used to devide the frequency of the OSC_0 input by 2^{12} and generate the interrupt request at every over-flow signal.

8-bit TIMER EVENT COUNTER

The timer event counter consists of a 8-bit counter (8-bit) register, comparing and controlling circuits. It is used to count pulses of an internal or external source. Coincidently, if value between the counter and the register causes interrupt request occur.

LCD DRIVER

The LCD driver is used to effect LCD display by transferring data in a program to the register assigned as port 5 and 6. It is available to select driving in static or dynamic operation (1/2 duty cycle) and frame frequency (128 Hz/64 Hz) and to drive up to 92 segments at 1/2 duty. Also, 16 outputs(SEG1~SEG16)of the segment terminals can be used as normal data outputs.

A standard LCD clock is produced by the oscillation dividing a crystal oscillator (32.768 kHz) connected to XT and $\overline{XT}$ terminals. This is also used as standard clock of displaying, clock interrupting and watch dog timer. (This clock can be also produced by dividing a frequency of 4.194304 MHz. Note the selection of the frame frequency, when the crystal oscillator is used without a frequency of 4.194304 MHz.)

INTERRUPT

As shown below, 1 ~ 4 is available to interrupt;

1. External interrupt at the falling edge of INT signal input
2. Clock interrupt at every second (32.768 kHz crystal oscillator)
3. Time base counter interrupt at the occurance of an overflow of the timer base counter.
4. Timer event counter interrupt coinciding between the signals of the 8-bit counter and register.

Interrupts 1 and 2 are also used to release the power down mode.

WATCH DOG TIMER (WDT)

A timer for detecting the overrunning of the program. This timer produces the overflow signal by dividing the 64 Hz frequency by 4 generated from the oscillation of a frequency of 32.768 kHz. It can be also halted, when unused.

TIMING CONTROL (T.C)

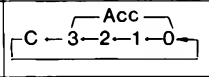
A 0 level on the $\overline{RESET}$ pin for longer than predetermined period initializes the internal circuitry and ports.

Clock pulses are supplied to the OSC_0 pin from an external source. A crystal or ceramic oscillator may be connected to OSC_0 and $\overline{OSC_1}$ to form an oscillator circuit to produce clock pulses.

INSTRUCTION SET

	Mnemonic		Hex op code	Byte	Cycle	Description
Load	LAI	n	90 – 9F	1	1	Acc ← n
	LLI	n	80 – 8F	1	1	L ← n
	LAL		21	1	1	Acc ← L
	LLA		2D	1	1	L ← Acc
	LAH		22	1	1	Acc ← H
	LHA		2E	1	1	H ← Acc
	LAM		38	1	1	Acc ← M
	LMA		2F	1	1	M ← Acc
	X		28	1	1	Acc ⟷ M
	LMI	nn	14 · nn	2	2	M(W) ← nn
	LHLI	nn	15 · nn	2	2	HL ← nn
	LAMD	mm	10 · mm	2	2	Acc ← Md
	LMAD	mm	11 · mm	2	2	Md ← Acc
	LMCT		3E · 59	2	2	M(W) ← CT
	LCTM		3E · 51	2	2	CT ← M(W)
	IPD	p	3D · pD	2	2	Acc ← Pp
	OPD	p	3D · pC	2	2	Pp ← Acc
Control	MEI		3E · 60	2	2	MEIF ← "1"
	MDI		3E · 61	2	2	MEIF ← "0"
	EIEX		3D · C8	2	2	EIEXF ← "1"
	EICT		3D · CB	2	2	EICTF ← "1"
	DIEX		3D · C4	2	2	EIEXF ← "0"
	DICT		3D · C7	2	2	EICTF ← "0"
	TIEX		3D · C0	2	2	SKIP IF EIEXF="1"
	TICT		3D · C3	2	2	SKIP IF EICTF="1"
	TQEX		3D · 20	2	2	SKIP IF IRQEX="1"
	TQCT		3D · D2	2	2	SKIP IF IRQCT="1"
	RQEX		3D · 24	2	2	IRQEX ← "0"
	RQCT		3D · D6	2	2	IRQCT ← "0"
Increment/ decrement	INL		31	1	1	L ← L+1, SKIP IF L="0"
	INH		32	1	1	H ← H+1, SKIP IF H="0"
	INM		33	1	1	M ← M+1, SKIP IF M="0"
	DCL		35	1	1	L ← L−1, SKIP IF L="F"
	DCH		36	1	1	H ← H−1, SKIP IF H="F"
	DCM		37	1	1	M ← M−1, SKIP IF M="M"
	INMD	mm	12 · mm	2	2	Md ← Md+1, SKIP IF Md="0"

INSTRUCTION SET (CONT.)

	Mnemonic	Hex op code	Byte	Cycle	Description
Bit handling	TAB n2	54 - 57	1	1	SKIP IF (ACC−Bit n2) = "1"
	TPB n2	50 - 53	1	1	SKIP IF (P−Bit n2) = "1"
	RPB n2	60 - 63	1	1	(P−Bit n2) ← "0"
	SPB n2	70 - 73	1	1	(P−Bit n2) ← "1"
	TMB n2	58 -5B	1	1	SKIP IF (M−Bit n2) = "1"
	RMB n2	68 - 6B	1	1	(M−Bit n2) ← "0"
	SMB n2	78 - 7B	1	1	(M−Bit n2) ← "1"
	TPBD p n2	3D · p0∼3	2	2	SKIP IF (Pp−Bit n2) = "1"
	RPBD p n2	3D · p4∼7	2	2	(Pp−Bit n2) ← "0"
	SPBD p n2	3D · p8∼B	2	2	(Pp−Bit n2) ← "1"
	TC	09	1	1	SKIP IF C = "1"
	RC	08	1	1	C ← "0"
	SC	07	1	1	C ← "1"
Arithmetic	ADS	02	1	1	Acc ← Acc+M, SKIP IF Cy="1"
	ADC	03	1	1	C, Acc ← C+Acc+M
	AIS n	3E · 4n	2	2	Acc ← Acc+n, SKIP IF Cy="1"
	DAS	0A	1	1	Acc ← Acc+10
	AND	0D	1	1	Acc ← Acc∧M
	OR	05	1	1	Acc ← Acc∨M
	EOR	04	1	1	Acc ← Acc¥M
	CMA	0B	1	1	Acc ← Acc
	CAM	16	1	1	SKIP IF Acc=M
	CAI n	3E · 0n	2	2	SKIP IF Acc=n
	RAL	0E	1	1	
Branch	JCP a6	C0 - FF	1	1	PC ← a6
	JP a11	40 _ 47 00 ¯ FF	2	2	PC ← a11
	CAL a11	A0 _ A7 00 ¯ FF	2	4	STACK ← PC+2, PC←a11, SP←SP−1
	RT	1E	1	4	PC ← STACK, SP ← SP+1
Others	PUSH	1C	1	3	STACK ← C, Acc, H, L, SP←SP−1
	POP	1D	1	3	C, Acc, H, L ← STACK, SP←SP+1
	STOP	3D · B9	2	2	CLOCK STOP
	NOP	00	1	1	NO OPERATION
	ECT	3D·BB	2	2	CTF ← "1" (Counter Start)
	DCT	3D·B7	2	2	CTF ← "0" (Counter Stop)
	TCT	3D·B3	2	2	Skip if CTF = "1"