OKI semiconductor

MSM6422

CMOS 4-BIT SINGLE CHIP MICROCONTROLLER

GENERAL DESCRIPTION

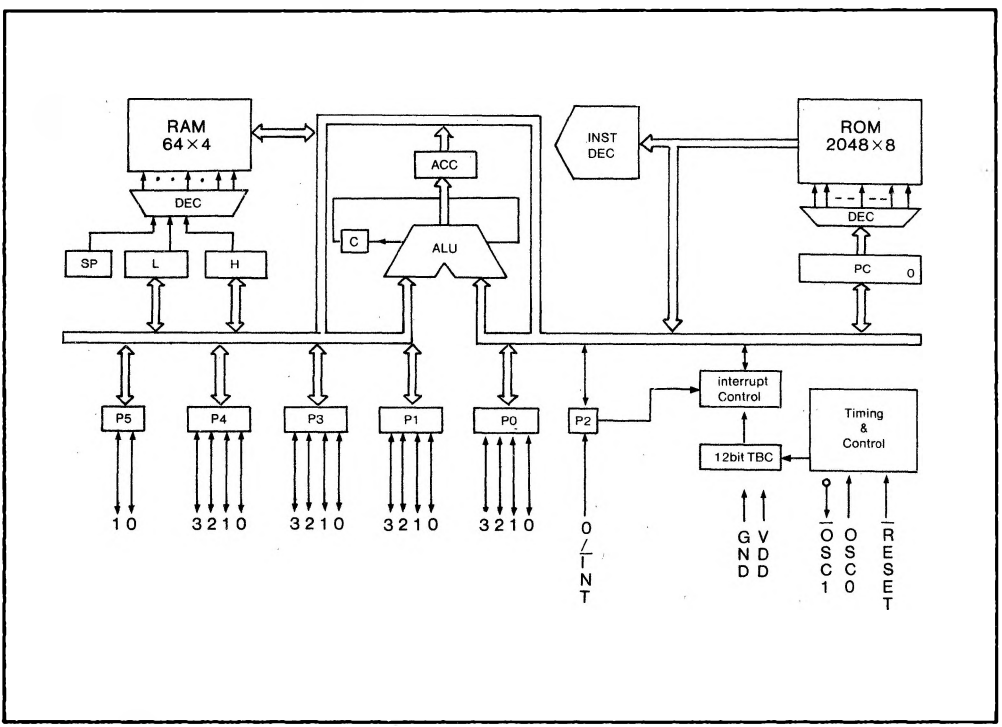
The OKI MSM6422 is a low power, high performance single-chip device implemented in complementary metal oxide semiconductor technology.

Integrated onto a single chip are 16K bits of mask program ROM; 256 bits of data RAM; 18 Input/Output lines and oscillator. Program memory is byte wide and data-paths are organized in 4 bit nibbles. RAM and I/O lines are bit addressable. 63 instructions include Binary, BCD operations; Bit set, Reset, Test; Subroutine call and return.

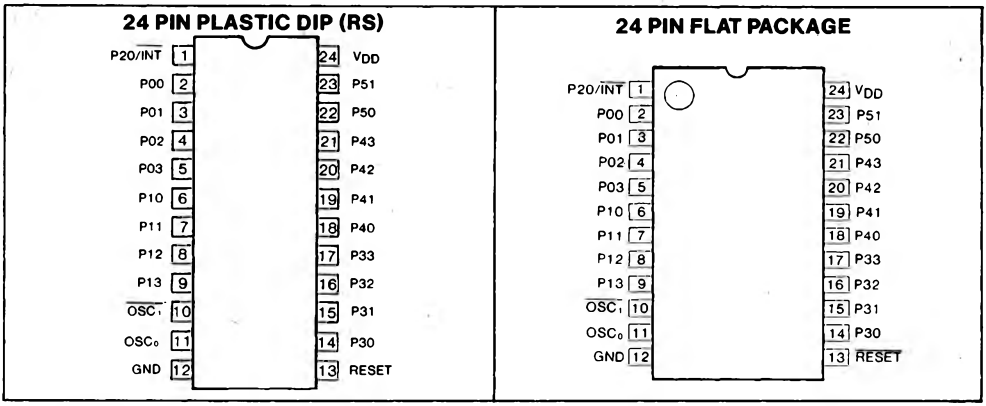
FEATURES

- Low power consumption – 30 mW Typical
- 2048 × 8 Internal ROM
- 64 × 4 Internal RAM
- 18 I/O Lines include 8 Bit Data Bus
- Self-contained Oscillator
- 63 Instructions
- 2 Interrupt Levels
- 16 Stack Levels
- −40 to +85°C Operating Temperature
- 4.5 to 5.5V Operating V_{DD} at 4.2 MHz
  3 to 6V Operating V_{DD} at 1MHz
- TTL Compatible
- 952ns Cycle Time @ 4.2MHz
  (V_{DD} 5V ±10%)

FUNCTIONAL BLOCK DIAGRAM



LOGIC SYMBOL (Top View)



PIN DESCRIPTION

Terminal symbol	Input/Output	Function	Reset
P00 P01 P02 P03	I/O	4-bit I/O ports (pseudo bidirectional configuration)	"1"
P10 P11 P12 P13	I/O	4-bit I/O ports (pseudo bidirectional configuration)	"1"
P30 P31 P32 P33	I/O	4-bit I/O ports (pseudo bidirectional configuration)	"1"
P40 P41 P42 P43	I/O	4-bit I/O ports (pseudo bidirectional configuration)	"0"
P50 P51	I/O	2-bit I/O ports (pseudo bidirectional configuration)	"0"
P20/$\overline{INT}$	Input	1-bit input port with a latch. Combined use with an interrupt input(falling edge trigger input)	The latch is reset to "0".
OSC_0	Input	System clock (SYSCLK) input terminal. This provides an oscillation circle with $\overline{OSC_1}$ terminal.	–
$\overline{OSC_1}$	Output	System clock output terminal. This provides an oscillation circle with OSC_0 terminal.	–
$\overline{RESET}$	Input	RESET input terminal.	–
V_{DD} GND	Input	Power Supply terminals.	–

FUNCTIONAL DESCRIPTION

Program ROM

Organized into as many as 2,048 words by 8 bits, ROM is used to store developed application programs (instructions). It is addressed by the program counter (PC).

Data RAM

RAM consists of up to 64 words 4 bits wide. It is addressed by the H- and L-registers or by the contents of the second byte of an instruction.

Input/Output Ports

18 input/output port lines are provided for effecting and controlling data transfer to and from an external source. The ports are selected by codes included in instructions.

P20/$\overline{INT}$ PIN (1 line)

A low on this interrupt input pin sets the interrupt request flag. The flag is automatically reset when an external interrupt occurs.
The line can be used as an input port when interrupt is not used.

12-BIT TIME BASE COUNTER (TBC)

The time base counter consists of a 12-bit binary counter. An interrupt request is generated each time an overflow occurs from the division of OSC_0 input signals by 2^{12}.

PROGRAM COUNTER (PC)

The program counter (PC) consists of a 11-bit binary up counter. It is used to address ROM.

STACK AND STACK POINTER (SP)

An interrupt or subroutine call (CAL) causes the contents of the program counter to be saved in the stack. The program counter is restored from the stack by the RT instruction.

All RAM locations (up to 16 levels) are available as the stack. Note that four words of RAM are used for each level.

The stack pointer is a 4-bit up-down counter that points to the address of the next stack to be used. It allows the RAM locations to be used as a push-down stack.

L-REGISTER

A 4-bit register which specifies RAM locations A3-A0.

H-REGISTER

A 4-bit register whose two low-order bits specify RAM locations A5-A4.

ALU

The 4-bit logic circuit that provides arithmetic and logical operations.

ACCUMULATOR (Acc)

Consisting of a 4-bit register, the accumulator holds the result of operations or the data present on ports.

C-FLAG

The flag that holds a carry generated from the result of operations.

TIMING CONTROL (TC)

A 0 level on the $\overline{RESET}$ pin for longer than a predetermined period initializes the internal circuitry and ports.

Clock pulses are supplied to the OSC_0 pin from an external source. A crystal or ceramic oscillator may be connected to OSC_0 and $\overline{OSC_1}$ to form an oscillator circuit to produce clock pulses.

ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Conditions	Limits	Unit
Supply Voltage	V_{DD}	Ta = 25°C	−0.3 ~ 7	V
Input Voltage	V_I		−0.3 ~ V_{DD}	V
Output Voltage	V_O		−0.3 ~ V_{DD}	V
Power Dissipation	P_D	Ta = 25°C per one package	200 max.	mW
		Ta = 25°C per one output	50 max.	mW
Storage Temperature	Tstg	—	−55 ~ +150	°C

OPERATING CONDITIONS

Parameter	Symbol	Condition	Limits	Unit
Supply Voltage	V_{DD}	f(OSC) $\leqq$ 1MHz	3 ~ 6	V
		f(OSC) $\leqq$ 4.2MHz	4.5 ~ 5.5	V
Memory-Hold Voltage	V_{DDH}	–	2 ~ 6	V
Operating Temperature	T_{OP}	–	−40 ~ +85	°C
Fan Out	N	MOS Load	15	–
		TTL Load	1	–

DC CHARACTERISTICS

(V_{DD} = 5V±10%, Ta = −40 ~ +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage *1, *2	V_{IH}	–	2.4	–	V_{DD}	V
"H" Input Voltage *3, *4	V_{IH}	–	4.2	–	V_{DD}	V
"L" Input Voltage	V_{IL}	–	−0.3	–	0.8	V
"H" Output Voltage *1, *5	V_{OH}	I_O = −15μA	4.2	–	–	V
"L" Output Voltage *1	V_{OL}	I_O = 1.6mA	–	–	0.4	V
"L" Output Voltage *5	V_{OL}	I_O = 15μA	–	–	0.4	V
Input Current *3	I_{IH}/I_{IL}	$V_I = V_{DD}/0V$	–	–	15/−15	μA
Input Current *2, *4	I_{IH}/I_{IL}	$V_I = V_{DD}/0V$	–	–	1/−30	μA
"H" Output Current *1	I_{OH}	V_O = 2.4V	−0.1	–	–	mA
"H" Output Current *1	I_{OH}	V_O = 0.4V	–	–	−1.2	mA
Input Capacity	C_I	f = 1MHz, Ta = 25°C	–	5	–	pF
Output Capacity	C_O		–	7	–	
Current Consumption (STOP)	I_{DDS}	V_{DD} = 2V, no load Ta = 25°C	–	0.2	5	μA
		No load	–	1	100	μA
Current Consumption	I_{DD}	Crystal oscillation, No load, 4.194304MHz	–	6	12	mA

*1 Applied to P0, P1, P3, P4, and P5

*2 Applied to P2

*3 Applied to OSC_0

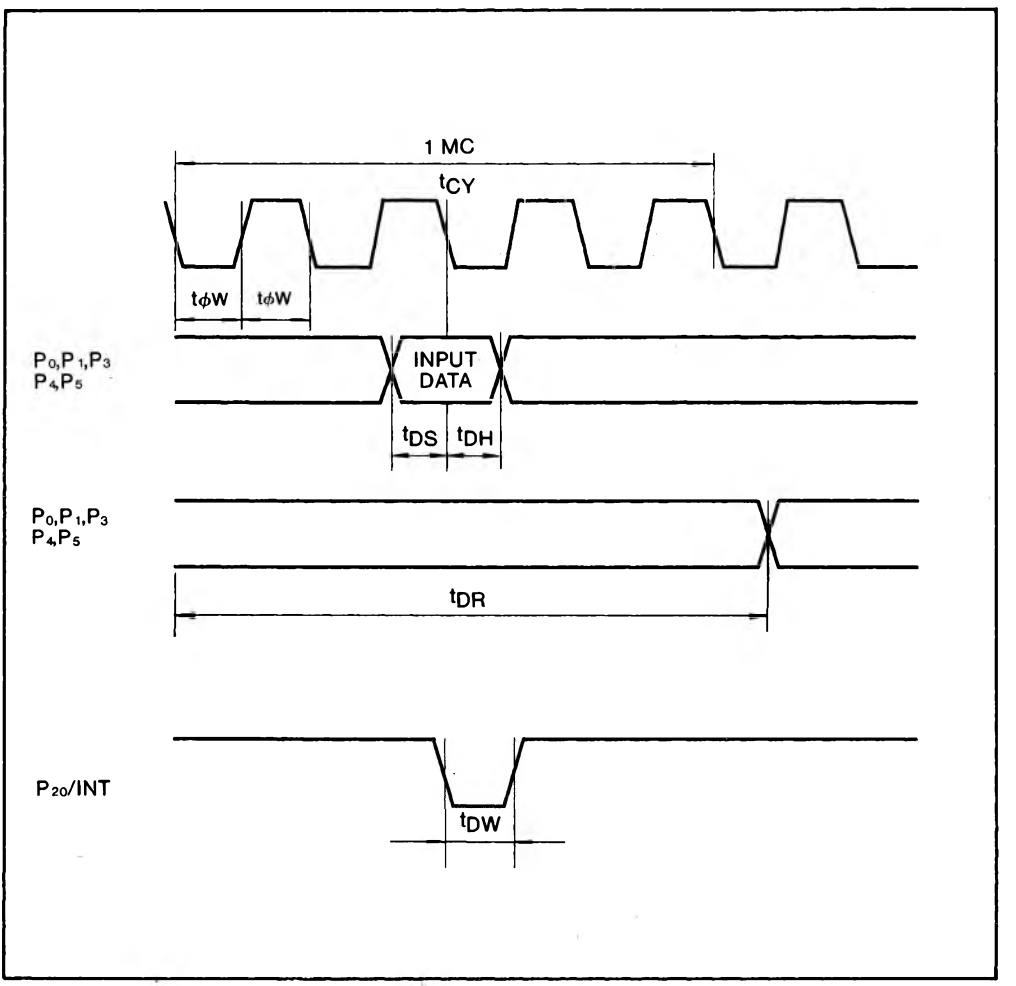
*4 Applied to $\overline{RESET}$

*5 Applied to $\overline{OSC_1}$

AC CHARACTERISTICS

(V_{DD} = 5V±10%, Ta = −40 ~ +85°C)

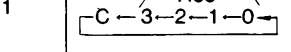
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock (OSC_0) Pulse Width	$t_{\phi W}$	–	119	–	–	ns
Cycle Time	t_{CY}	–	952	–	–	ns
Input Data Setup Time	t_{DS}	–	120	–	–	ns
Input Data Hold Time	t_{DH}	–	120	–	–	ns
Input Data/Input Clock Pulse Width	t_{DW}	–	120	–	–	ns
Data Delay Time	t_{DR}	C_L=15pF	–	–	t_{CY} +300	ns



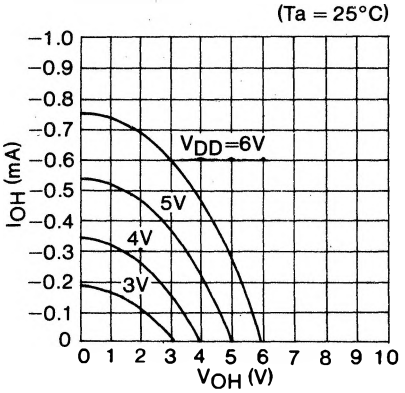
INSTRUCTION SET

	Mnemonic	Hex op code	Byte	Cycle	Description
Load	LAI n	90 – 9F	1	1	Acc ← n
	LLI n	80 – 8F	1	1	L ← n
	LAL	21	1	1	Acc ← L
	LLA	2D	1	1	L ← Acc
	LAH	22	1	1	Acc ← H
	LHA	2E	1	1	H ← Acc
	LAM	38	1	1	Acc ← M
	LMA	2F	1	1	M ← Acc
	X	28	1	1	Acc ← M
	LMI nn	14 · nn	2	2	M(W) ← nn
	LHLI nn	15 · nn	2	2	HL ← nn
	LAMD mm	10 · mm	2	2	Acc ← Md
	LMAD mm	11 · mm	2	2	Md ← Acc
	IPO p	3D · pD	2	2	Acc ← Pp
	OPD p	3D · pC	2	2	Pp ← Acc
Control	MEI	3E · 60	2	2	MEIF ← "1"
	MDI	3E · 61	2	2	MEIF ← "0"
	EIEX	3D · C8	2	2	EIEXF ← "1"
	EITB	3D · C9	2	2	EITBF ← "1"
	DIEX	3D · C4	2	2	EIEXF ← "0"
	DITB	3D · C5	2	2	EITBF ← "0"
	TIEX	3D · C0	2	2	SKIP IF EIEXF="1"
	TITB	3D · C1	2	2	SKIP IF EITBF="1"
	TQEX	3D · 20	2	2	SKIP IF IRQEX="1"
	TQTB	3D · D0	2	2	SKIP IF IRQTB="1"
	RQEX	3D · 24	2	2	IRQEX ← "0"
	RQTB	3D · D4	2	2	IRQTB ← "0"
Increment/ decrement	INL	31	1	1	L ← L+1, SKIP IF L="0"
	INH	32	1	1	H ← H+1, SKIP IF H="0"
	INM	33	1	1	M ← M+1, SKIP IF M="0"
	DCL	35	1	1	L ← L-1, SKIP LF L="F"
	DCH	36	1	1	H ← H-1, SKIP IF H="F"
	DCM	37	1	1	M ← M-1, SKIP IF M="F"
	INMD mm	12 · mm	2	2	Md ← Md+1, SKIP IF Md="0"

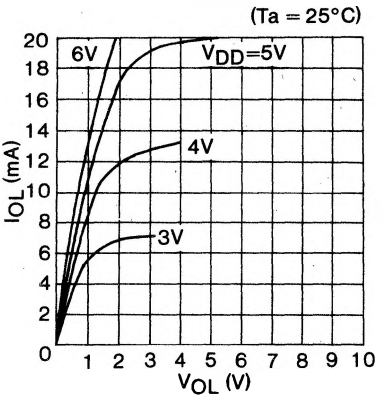
INSTRUCTION SET (CONT.)

	Mnemonic	Hex op code	Byte	Cycle	Description
Bit handling	TAB n2	54 - 57	1	1	SKIP IF (Acc-Bit n2) = "1"
	TMB n2	58 -5B	1	1	SKIP IF (M-Bit n2) = "1"
	RMB n2	68 - 6B	1	1	(M-Bit n2) ← "0"
	SMB n2	78 - 7B	1	1	(M-Bit n2) ← "1"
	TPBD p n2	3D · p0~3	2	2	SKIP IF (Pp-Bit n2) = "1"
	RPBD p n2	3D · p4~7	2	2	(Pp-Bit n2) ← "0"
	SPBD p n2	3D · p8~B	2	2	(Pp-Bit n2) ← "1"
	TC	09	1	1	SKIP IF C = "1"
	RC	08	1	1	C ← "0"
	SC	07	1	1	C ← "1"
Arithmetic	ADS	02	1	1	Acc ← Acc+M, SKIP IF Cy="1"
	ADC	03	1	1	C, Acc ← C+Acc+M
	AIS n	3E · 4n	2	2	Acc ← Acc+n, SKIP IF Cy="1"
	DAS	0A	1	1	Acc ← Acc+10
	AND	0D	1	1	Acc ← Acc∧M
	OR	05	1	1	Acc ← Acc∨M
	EOR	04	1	1	Acc ← Acc∀M
	CMA	0B	1	1	Acc ← $\overline{\text{Acc}}$
	CAM	16	1	1	SKIP IF Acc=M
	CAI n	3E · 0n	2	2	SKIP IF Acc=n
	RAL	0E	1	1	
Branch	JCP a6	C0 - FF	1	1	PC ← a6
	JP a11	40 - 47 00 - FF	2	2	PC ← a11
	CAL a11	A0 - A7 00 - FF	2	4	STACK ← PC+2, PC←a11, SP←SP-1
	RT	1E	1	4	PC ← STACK, SP ← SP+1
Others	PUSH	1C	1	3	STACK ← PC+2, PC←a11, SP←SP-1
	POP	1D	1	3	C, Acc, H, L ← STACK, SP←SP+1
	STOP	3D · B9	2	2	CLOCK STOP
	NOP	00	1	1	NO OPERATION

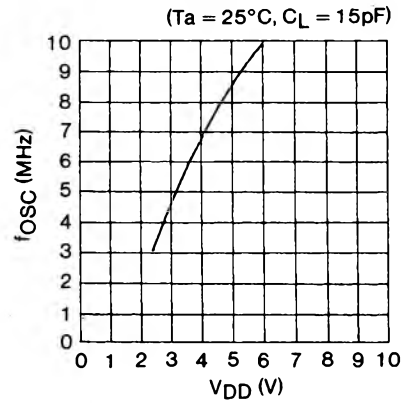
TYP. Current (I_{OH}) vs Voltage (V_{OH}) for High state Output



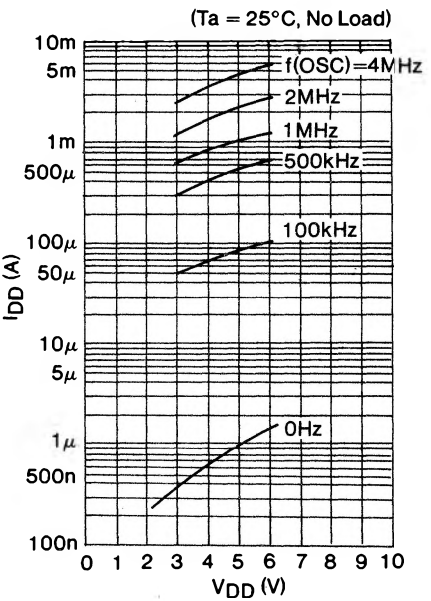
TYP. Current (I_{OL}) vs Voltage (V_{OL}) for Low state Output



TYP. Maximum Oscillator Frequency f(OSC) vs Supply Voltage (V_D)



TYP. Supply Current (I_{DD}) vs Supply Voltage (V_{DD})



TYP. Maximum Oscillator Frequency f(OSC) vs Temperature (Ta)