OKI semiconductor

MSM5842

CMOS 4-BIT SINGLE CHIP MICROCONTROLLER

GENERAL DESCRIPTION

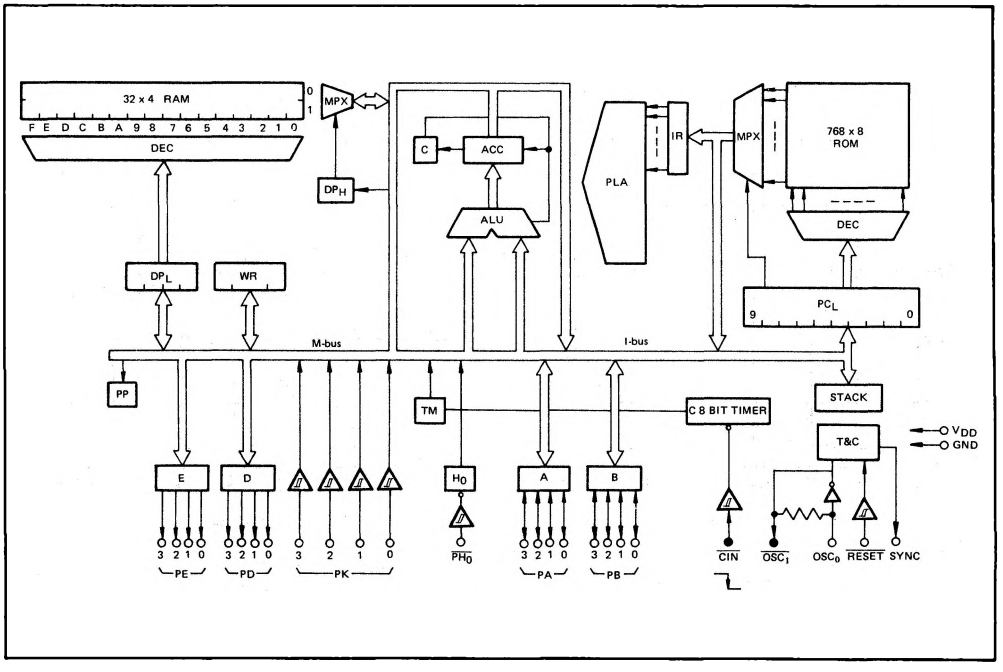
The OKI MSM5842 microcontroller is a low-power, high-performance single chip device implemented in complementary metal oxide semiconductor technology. Integrated with this one chip are 6K bits of mask program ROM, 128 bits of data RAM, 21 Input/Output lines, an 8-bit binary timer/counter, and oscillator. Program memory is byte wide and data paths are organized in 4 bit nibbles. RAM and I/O lines are bit addressable. 52 instructions include binary, BCD, operations; bit set, reset, test; 8-bit I/O; relative jumps; multifunctional instructions (increment, modify, skip); 8-bit wide table output; subroutine call and return. 94% of instructions are single byte, single cycle operations.

Available in plastic (RS) package.

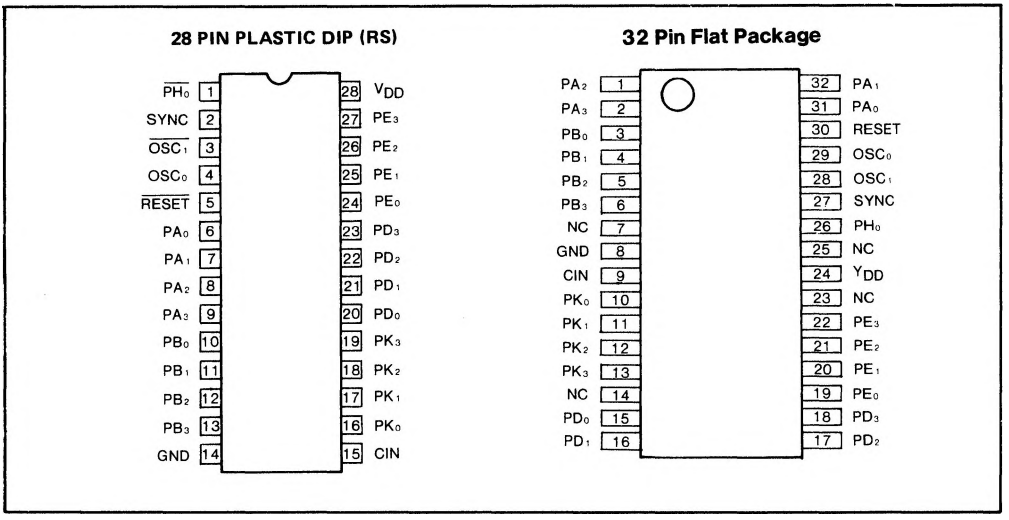
FEATURES

- Low Power Consumption – 7mW Typical
- 100% Static Logic – 100μW Standby
- 768 × 8 Internal ROM
- 32 × 4 Internal RAM
- 21 I/O Lines Incl. 8 Bit Data Bus
- 8 Bit Binary Timer/Counter
- Self-contained Oscillator
- 52 Instructions
- 1 Stack Level
- −20° to +70°C Operating Temperature
- 3V to 6V Operating V_{DD}
- Battery Powered or Battery Backup
- TTL Compatible (with pullups)
- 7.6μs Cycle Time @4.2MHz

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top View)



PIN DESCRIPTION

Designation	Pin No.	Function
GND	14	Circuit GND potential
V_{DD}	28	Main power source (+5V)
OSC_0	4	Crystal OSC input, external clock input
$\overline{OSC_1}$	3	Crystal OSC input, external clock output (not TTL compatible)
PA, PB	6 to 13	Quasi-bidirectional ports for 4 bit parallel I/O. Used as a pair for 8 bit I/O.
PD, PE	20 to 27	Output ports for 4 bit parallel output and bit set/reset. Specified by internal port pointer. Bit position specified by set/reset instruction.
PK	16 to 19	4 bit parallel or bit test input port (unlatched)
$\overline{PH}$	1	1 bit input port with latched memory (negative level sensitive)
$\overline{RESET}$	5	RESET must be low for more than one machine cycle and has priority over every other signal. (see MSM5842 user's manual for initialization sequence)
$\overline{CIN}$	15	Negative edge sensitive external input for timer/counter.
SYNC	2	General purpose synchronizing signal output at the beginning of each machine cycle.

FUNCTIONAL DESCRIPTION

Program ROM

The MSM5842 will address up to 768 bytes of program ROM. All instructions are byte wide. Only three of the 52 instructions require two bytes of program code. The instructions are routed to a programmed logic array which generates the necessary internal control signals.

Data RAM

Data is organized in 4 bit nibbles. Internal data RAM consists of 32 nibbles and one nibble which is a dedicated general purpose register, W, accessible directly under program control. DATA RAM must be addressed indirectly through the DP (data pointer) register, a five bit pointer (directly accessible by numerous instructions) consisting of a 4 bit DP_L register and a 1 bit DP_H register. Any nibble of internal data RAM can be accessed through the DP registers. Some instructions, automatically change the contents of the DP register allowing efficient array processing.

Input/Output Ports

PA, PB – These two ports are pseudo-bidirectional ports which can be used as simple I/O lines or used as either a 4 bit or 8 bit parallel bus.

PD, PE – These two output ports are addressed indirectly through the ONE BIT port pointer whose contents are changed through certain instructions. These ports are bit (set/reset) addressable.

PK is an input port without a Latch circuit, addressable as a nibble input.

PH is a one bit input port with a Latch circuit, which can be tested and reset under program control.

Timer/Counter

The timer/counter is an 8-bit counter whose input is an external signal ($\overline{CIN}$). The TM flag is set when the timer/counter generates a carry.

Stack

The stack is a single register for storing return-from-subroutine address information. It is ten bits wide.

Program Counter (PC)

The program counter is ten bits wide.

Accumulator

The accumulator register is the data path focal point of the CPU. Approximately one-half of the instructions involve the accumulator. Its contents are the source and destination for many ALU operations and port operations. CASE statements (computed GOTOs) are possible by using the Jump with Accumulator (JA) instruction.

Flags

The MSM5842 is endowed with the following set of flags.

Z – zero flag	: Indicates that the result of the previous operation was zero
C – carry	: Indicates a carry from the previous operation
TM – timer flag	: Indicates an overflow of the timer/counter register
H_0 – H_0 memory	: Indicates that an input has been detected on the H_0 input

INSTRUCTION SET

	Mnemonic	Description	Instruction Code								Byte	Cycle
			7	6	5	4	3	2	1	0		
Load, Store, Read, Clear	CLA	Clear Accumulator	0	0	0	1	0	0	0	0	1	1
	CCL	Clear DP_L	0	0	1	0	0	0	0	0	1	1
	CLH	Clear DP_H	0	1	1	0	0	0	0	0	1	1
	LAI	Load Accumulator with Immediate	0	0	0	1	I_3	I_2	I_1	I_0	1	1
	LLI	Load DP_L with Immediate	0	0	1	0	I_3	I_2	I_1	I_0	1	1
	LHI	Load DP_H with Immediate	0	1	1	0	0	0	0	I_0	1	1
	L	Load Accumulator with Memory	1	0	0	1	0	1	0	0	1	1
	LAL	Load Accumulator with DP_L	0	1	0	1	0	1	0	1	1	1
	LLA	Load DP_L with Accumulator	0	1	0	1	0	1	0	0	1	1
	LAW	Load Accumulator with W Register	1	0	0	0	0	1	0	0	1	1
	SI	Store Accumulator to Memory then Increment DP_L	1	0	0	1	0	0	0	0	1	1
	LWA	Load W Register with Accumulator	1	0	0	0	0	0	0	0	1	1
	LPA	Load Port Pointer with Accumulator	0	1	0	1	1	0	0	0	1	1
	LTI	Load Timer with All Zeros	0	1	1	0	1	0	0	0	1	1

INSTRUCTION SET (CONT.)

	Mnemonic	Description	Instruction Code 7	6	5	4	3	2	1	0	Byte	Cycle
Exchange	X	Exchange Accumulator with Memory	1	0	0	1	1	0	0	0	1	1
Increment/Decrement	INA	Increment Accumulator (Skip if Zero)	0	0	0	0	0	0	0	1	1	1
	INL	Increment DP_L (Skip if Zero)	0	1	0	1	0	1	1	1	1	1
	INM	Increment Memory (Skip if Zero)	0	1	0	1	1	1	0	1	1	1
	INW	Increment W Register (Skip if Zero)	1	0	0	0	1	0	0	0	1	1
	DCA	Decrement Accumulator – Skip if Not All Ones	0	0	0	0	1	1	1	1	1	1
	DCL	Decrement DP_L (Skip if All Ones)	0	1	0	1	0	1	1	0	1	1
	DCM	Decrement Memory (Skip if All Ones)	0	1	0	1	1	1	0	0	1	1
Logical	CAO	Complement Accumulator of One	0	1	0	1	0	0	0	0	1	1
	RAL	Rotate Accumulator Left through Carry	0	1	0	0	0	1	1	1	1	1
Arithmetic	AC	Add Memory to Accumulator with Carry	0	1	0	0	1	1	0	0	1	1
	AS	Add Memory to Accumulator, Skip if Carry	0	1	0	0	1	1	1	0	1	1
	AIS	Add Immediate to Accumulator, Skip if Carry	0	0	0	0	I_3	I_2	I_1	I_0	1	1
	DAS	Decimal adjust Accumulator in Subtraction	0	1	0	1	1	0	1	0	1	1
	CM	Compare Accumulator with Memory, Skip if Equal	0	1	0	1	1	1	1	0	1	1
Bit Set/Reset/Test	SMB	Set Memory Bit	1	0	1	1	1	0	I_1	I_0	1	1
	RMB	Reset Memory Bit	1	0	1	1	1	1	I_1	I_0	1	1
	TAB	Test Accumulator Bit	1	0	1	0	0	0	I_1	I_0	1	1
	TMB	Test Memory Bit	1	0	1	0	0	1	I_1	I_0	1	1
	THB	Test H Port Bit	1	0	1	0	1	1	0	I_0	1	1
	TTM	Test Timer flag	1	0	1	0	1	1	1	0	1	1
	TC	Test Carry flag	0	1	0	0	0	0	1	0	1	1
	SC	Set Carry flag	0	1	0	0	0	0	0	0	1	1
	RC	Reset Carry flag	0	1	0	0	0	0	0	1	1	1
Branch/Subroutine	J	Jump	0 I_7	0 I_6	1 I_5	1 I_4	0 I_3	0 I_2	I_9 I_1	I_8 I_0	2	2
	JC	Jump in Current Page	1	1	I_5	I_4	I_3	I_2	I_1	I_0	1	1
	JA	Jump with Accumulator	0	1	0	0	0	0	1	1	1	1
	CAL	Call Subroutine	0 I_7	0 I_6	1 I_5	1 I_4	1 I_3	0 I_2	I_9 I_1	8 I_0	2	2
	RT	Return from Subroutine	0	1	0	1	1	0	0	1	1	2
Input/Output	OTD	Output Table Data	0	1	1	1	0	0	0	1	1	2
	OA	Output Accumulator to Port A	0	1	1	1	0	0	1	0	1	1
	OB	Output Accumulator to Port B	0	1	1	1	0	0	1	1	1	1
	OP	Output Accumulator to Port P designated Port Pointer	0	1	1	1	0	1	0	0	1	1
	OPM	Output Memory to Port P designated Port Pointer	0	1	1	1	0	1	1	0	1	1
	IA	Input Port A in Accumulator	0	1	1	1	1	0	1	0	1	1
	IB	Input Port B in Accumulator	0	1	1	1	1	0	1	1	1	1
	IK	Input Port K in Accumulator	0	1	1	1	1	1	0	0	1	1
Control	NOP	No Operation	0	0	0	0	0	0	0	0	1	1

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Limits	Unit
Supply Voltage	V_{DD}	Ta = 25°C	−0.3 to 7	V
Input Voltage	V_I	Ta = 25°C	−0.3 to VDD	V
Storage Temperature	T_{stg}		−55 to +150	°C

Note: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Symbol	Conditions	Limits	Unit
Supply Voltage	V_{DD}	1MHz	3 to 6	V
		4.2MHz	4.5 to 5.5	V
Operating Temperature	Top		−40 to 85	°C
Fan Out		MOS Load	40	
		TTL Load	1	

D.C. CHARACTERISTICS

(V_{DD} = 5V±10%, Ta = −40° to +85°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
High Input Voltage	V_{IH}	–	3.6			V
Low Input Voltage	V_{IL}	–			0.8	V
High Output Voltage (1)	V_{OH}	I_O = −40μA	4.2			V
Low Output Voltage	V_{OL}	I_O = 1.6mA			0.45	V
OSC_O Input Leak Current	I_{IH}	$V_I = V_{DD/0V}$			25	μA
	I_{IL}				−25	
$\overline{RESET}$ Leak Current	I_{IH}	$V_I = V_{DD/0V}$			1	μA
	I_{IL}				−20	
Input Leak Current(2)	I_{IH}	$V_I = V_{DD/0V}$			1	μA
	I_{IL}				−1	
PA, PB High Output Current	I_{OH}	V_{OH} = 0.4V			−1	mA
High Output Current(1)	I_{OH}	V_{OH} = 2.5V	−0.25			mA
Low Output Current	I_{OL}	V_{OL} = 0.45V	1.6			mA
Input Capacitance	C_I	f = 1MHz Ta = 25°C		5		pF
Output Capacitance	C_O	f = 1MHz Ta = 25°C		7		pF
Current Consumption(3)	I_{DD}	$V_I = V_{DD/0V}$		20	200	μA
	I_{DD}	$V_I = V_{DD/0V}$ f=4.2MHz		1.5	4	mA

Notes: (1) Except PA, PB (see graphs)
(2) Except OSC_O, $\overline{RESET}$
(3) Typical Value of V_{DD} is 5V

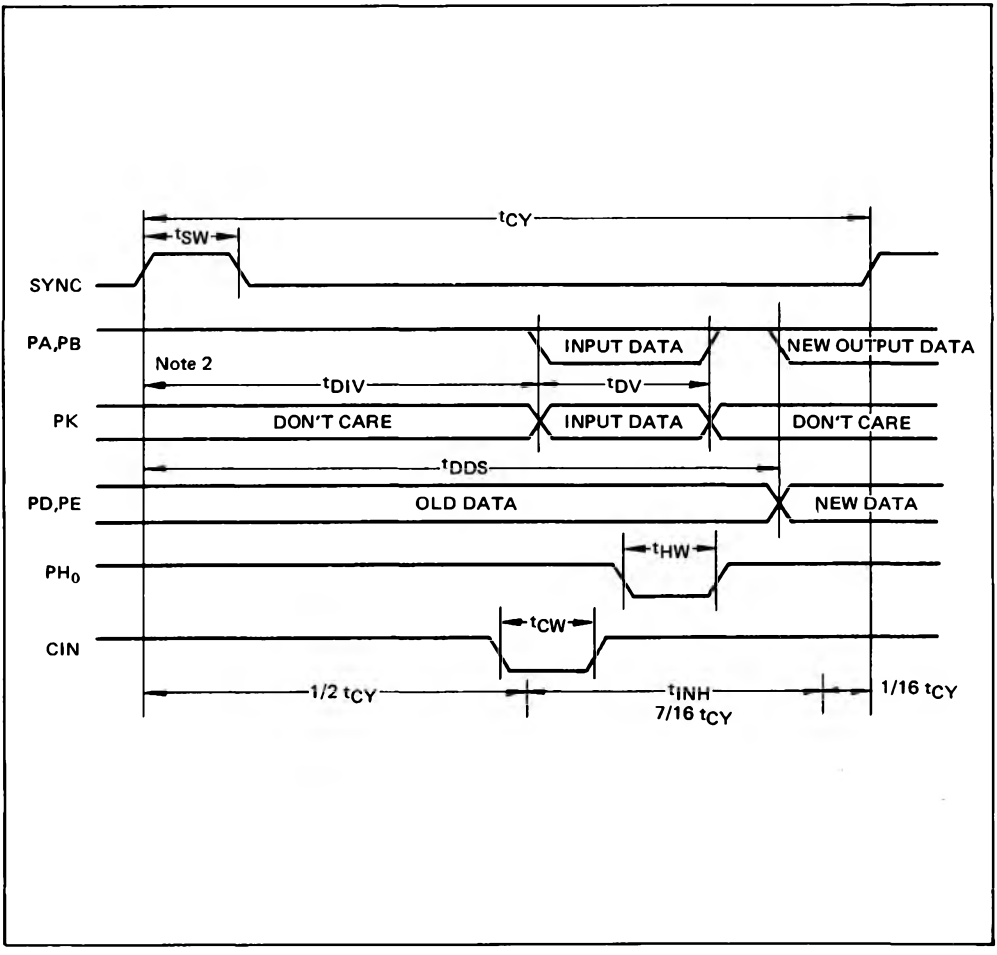
A.C. CHARACTERISTICS

(V_{DD} = 5V±10%, Ta = −40° to +85°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Cycle Time	t_{CY}	O_{SC} = 4MHz	7.6			μS
Sync Pulse Width	t_{SW}		0.95			μS
Port Input Invalid Time	t_{DIV}				1/2 t_{CY} + 0.5	μS
Port Input Valid Time	t_{DV}		2			μS
Sync ↑ to New Data Valid	t_{DDS}	PD, PE C_L = 50pF			13/16 t_{CY} + 0.5	μS
PH_0 Input Pulse Width	t_{HW}	(1)	250			nS
$\overline{CIN}$ Input Pulse Width	t_{CW}		250			nS

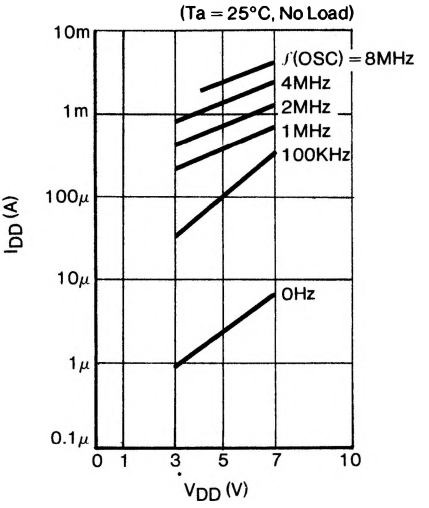
Notes: (1) The processor logic may ignore the following event:
A PH_0 low level occurring only during T_{INH} of a THB instruction.
(2) All 'ONES' must be output before reading port A or B.

TIMING CHARTS

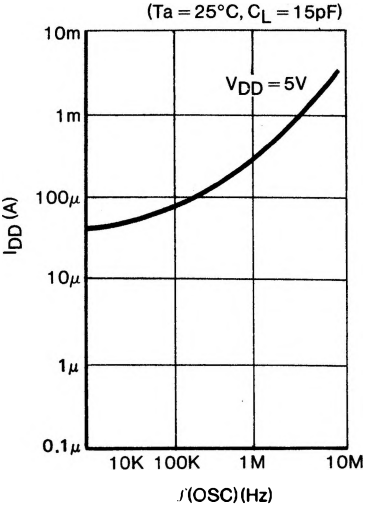


TYPICAL PERFORMANCE CURVES

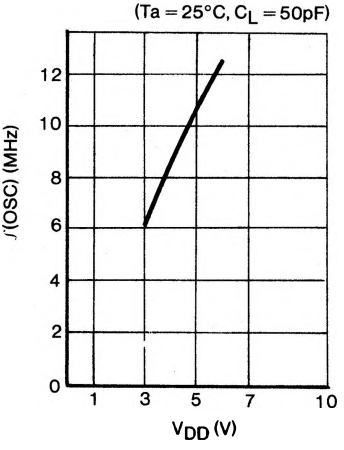
Supply Current vs Supply Voltage



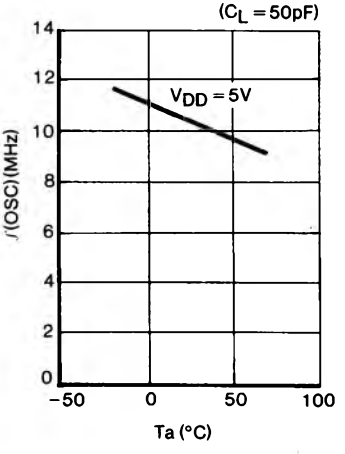
Supply Current vs Oscillator Frequency



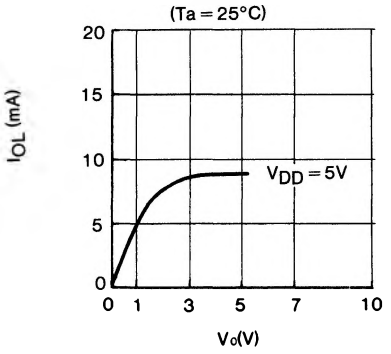
Oscillator Frequency vs Supply Voltage



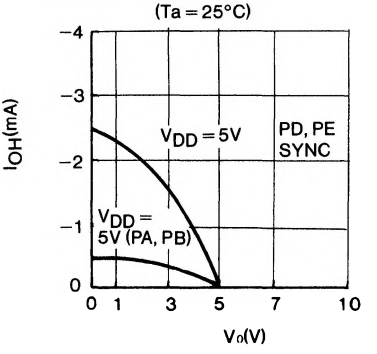
Oscillator Frequency vs Temperature



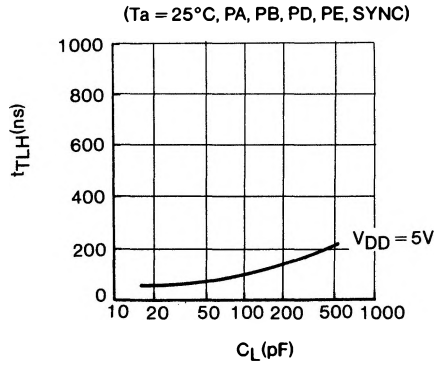
Low Current Out vs Voltage



High Current Out vs Voltage



Fall Time vs Load



Rise Time vs Load