OKI semiconductor

MSM5114RS

4096-BIT (1024 x 4) CMOS STATIC RAM

GENERAL DESCRIPTION

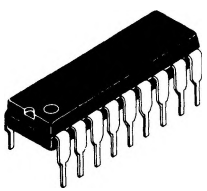
The Oki MSM5114 is a 4096-bit static Random Access Memory organized as 1024 words by 4 bits using Oki's reliable Silicon Gate CMOS technology. It uses fully static circuitry and therefore requires no clocks or refreshing to operate. Microwatt power dissipation typical of all CMOS is exhibited in all static states. Directly TTL compatible inputs, outputs and operation from a single +5V supply simplify system designs. Common data input/output pins using three-state outputs are provided.

The MSM5114 series is offered in an 18-pin plastic (RS suffix) package. The series is guaranteed for operation from 0°C to 70°C and over a 4V to 6V power supply range.

FEATURES

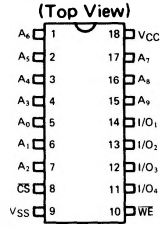
- Fully Static Operation
- Low Power Dissipation
  40μW Max. Standby Power
  192 mW/MHz Max. Operating Power
- Data Retention to V_{CC}=2V
- Single 4 ~ 6V Power Supply
- High Density 300-mil 18-Pin Package
- Common I/O Capability using Three-State Outputs
- Directly TTL/CMOS Compatible
- Silicon Gate CMOS Technology
- Interchangeable with Intel 2114L Devices

	5114-2	5114-3	5114
Max. Access Time (NS)	200	300	450
Max. Operating Power (MW/MHz)	192	192	192
Max. Standby Power (μW)	40	40	40



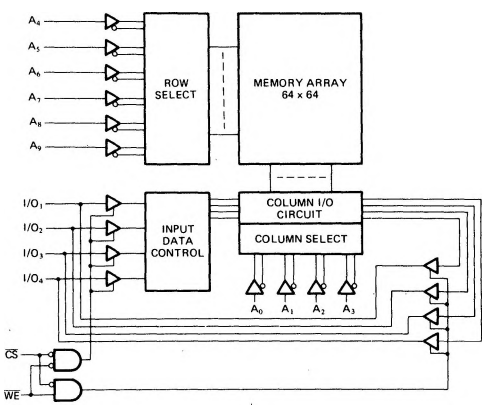
PIN CONFIGURATION

(Top View)



A_0 To A_9: Address Inputs
$\overline{WE}$: Write Enable
$\overline{CS}$: Chip Select
$I/O_1 \sim I/O_4$: Data Input/Output
V_{CC}: +5V Supply
VSS : Ground

FUNCTIONAL BLOCK DIAGRAM



$\overline{CS}$	$\overline{WE}$	I/O	Mode
H	X	Hi-Z	Not Selected
L	L	H	Write 1
L	L	L	Write 0
L	H	D-out	Read

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit	Conditions
Supply Voltage	V_{CC}	−0.3 to 7.0	V	Respect to VSS
Input Voltage	V_{IN}	−0.3 to V_{CC} + 0.3	V	
Data I/O Voltage	V_D	−0.3 to V_{CC} + 0.3	V	
Storage Temperature	T_{stg}	−55 to 150	°C	

Note: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operations of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	V_{CC}	4	5	6	V	
Input Signal Level	V_{IH}	2.4	5	V_{CC}	V	5V ±10%
	V_{IL}	−0.3	0	0.8	V	
Operating Temperature	T_{opr}	0		70	°C	

DC CHARACTERISTICS

(V_{CC} = 5V ± 10%; Ta = 0°C to +70°C, unless otherwise noted.)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input Load Current	I_{LI}	−1		1	μA	V_{IN} = 0 to V_{CC}
Data I/O Leakage Current	I_{LO}	−1		1	μA	$V_{I/O}$ = 0 to V_{CC}
Output High Voltage	V_{OH}	2.4			V	I_{OUT} = −1.0 mA
Output Low Voltage	V_{OL}			0.4	V	I_{OUT} = 1.6 mA
Standby Supply Current	I_{CCS}		0.2	50	μA	V_{IN} = 0 or V_{CC}, $V\overline{CS}$ = V_{CC}
Operating Supply Current	I_{CC}		19	35	mA	V_{IN} = 0 or V_{CC}, t_{RC} = 1 μs

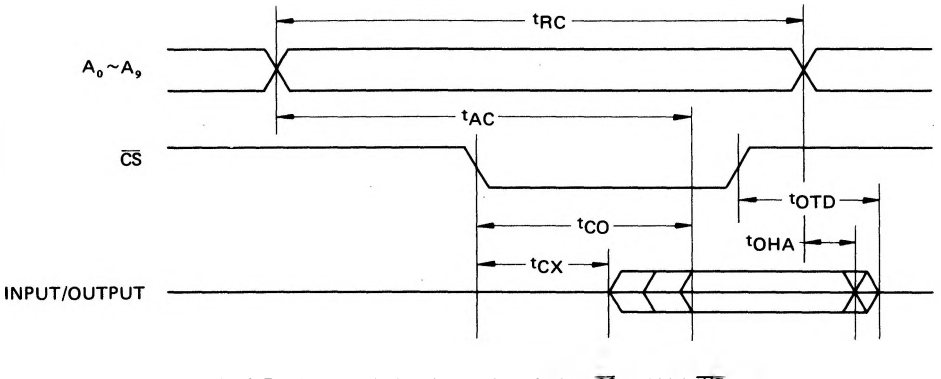
AC CHARACTERISTICS

READ CYCLE

(V_{CC} = 5V ±10%, T_a = 0°C to +70°C)

Parameter	Symbol	5114-2		5114-3		5114		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	200		300		450		ns
Access Time	t_{AC}		200		300		450	ns
Chip Selection to Output Valid	t_{CO}		200		300		450	ns
Chip Selection to Output Active	t_{CX}	20		20		20		ns
Output 3-state from Deselection	t_{OTD}		60		80		100	ns
Output Hold from Address Change	t_{OHA}	10		10		10		ns

READ CYCLE



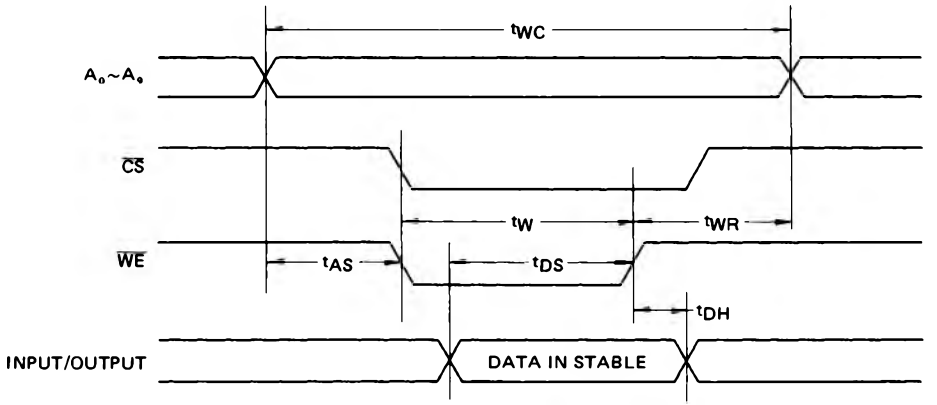
Notes:
1. A Read occurs during the overlap of a low $\overline{CS}$ and high $\overline{WE}$.
2. Input Pulse levels: 0.8V to +2.4V
3. Input Rise and Fail Time: 10 ns
4. Timing Measurement Reference Levels: 1.5V
5. Output Load: 1 TTL Gate and C_L = 50 pF

WRITE CYCLE

(V_{CC} = 5V ±10%, T_a = 0°C to +70°C)

Parameter	Symbol	5114-2		5114-3		5114		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	200		300		450		ns
Write Time	t_W	150		190		250		ns
Write Release Time	t_{WR}	20		30		50		ns
Address Setup Time	t_{AS}	20		20		20		ns
Data Setup Time	t_{DS}	120		150		200		ns
Data Hold From Write Time	t_{DH}	10		10		10		ns

WRITE CYCLE



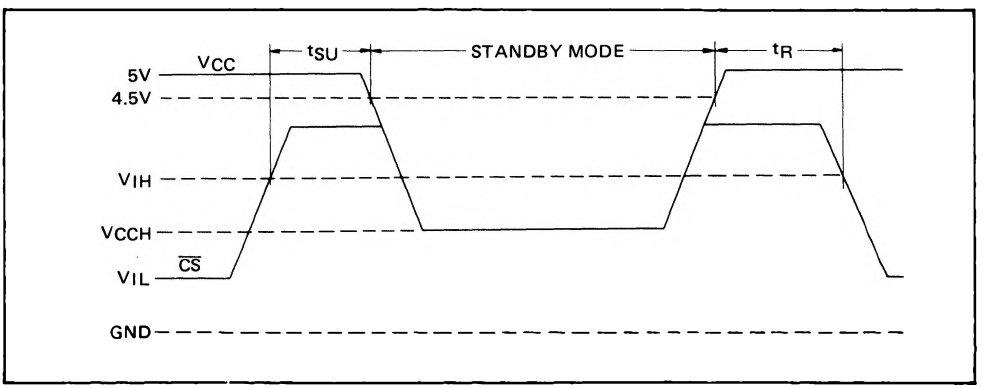
Notes:
1. A Write occurs during the overlap of a low $\overline{CS}$ and low $\overline{WE}$.
2. Input Pulse Levels: 0.8V to +2.4V
3. Input Rise and Fall Time: 10 ns
4. Timing Measurement Reference Levels: 1.5V
5. t_W: Overlap time of a low $\overline{CS}$ and low $\overline{WE}$.
6. t_{AS}: Low $\overline{WE}$ from address or low $\overline{CS}$ from address
7. t_{WR}, t_{DS} and t_{DH} are defined from High CS or High $\overline{WE}$, whichever occurs first.

LOW V_{CC} DATA RETENTION CHARACTERISTICS

(T_a = 0°C to +70°C, unless otherwise noted.)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
V_{CC} for Data Retention	V_{CCH}	2			V	V_{IN} = 0 or V_{CC}, $V_{\overline{CS}} = V_{CC}$
Data Retention Current	I_{CCH}		0.1	20	μA	V_{CC} = 2V $V_{CS} = V_{CC}$ V_{IN} = 0V or V_{CC}
$\overline{CS}$ to Data Retention Time	t_{SU}	0			ns	
Operation Recovery Time	t_R	t_{RC}			ns	

LOW V_{CC} DATA RETENTION WAVEFORM



CAPACITANCE

($T_a = 25°C$, f = 1 MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input/Output Capacitance	$C_{I/O}$			10	pF
Input Capacitance	C_{IN}			8	pF

Note: This parameter is periodically sampled and not 100% tested.